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Subject: Microprocessor Architectures/(EEC 201)
Term: Feb / May 2019

ANSWER THE FOLLOWING QUESTIONS:

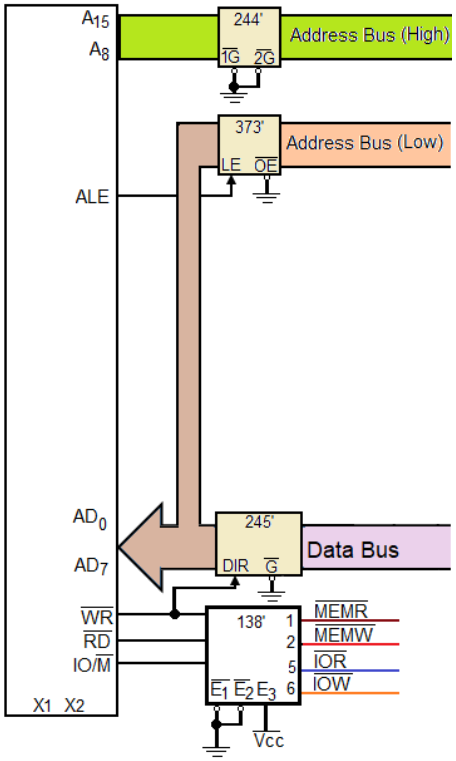
1. Consider the next specifications:

Component	Size	Start address	Description
Rom:2764	8K	continuous	Read only memory
IO_in	-	3300h	input port
RAM:6264	8K	6000h	Random access memory
RAM:6264	16K	continuous	Random access memory
IO_in_out	-	20h	bidirectional Peripheral I/O

(a) Design a 8085 microcomputer board system that meet the given specifications.

Solution: 8085 architecture:

1. Draw the 8085 kit includes:



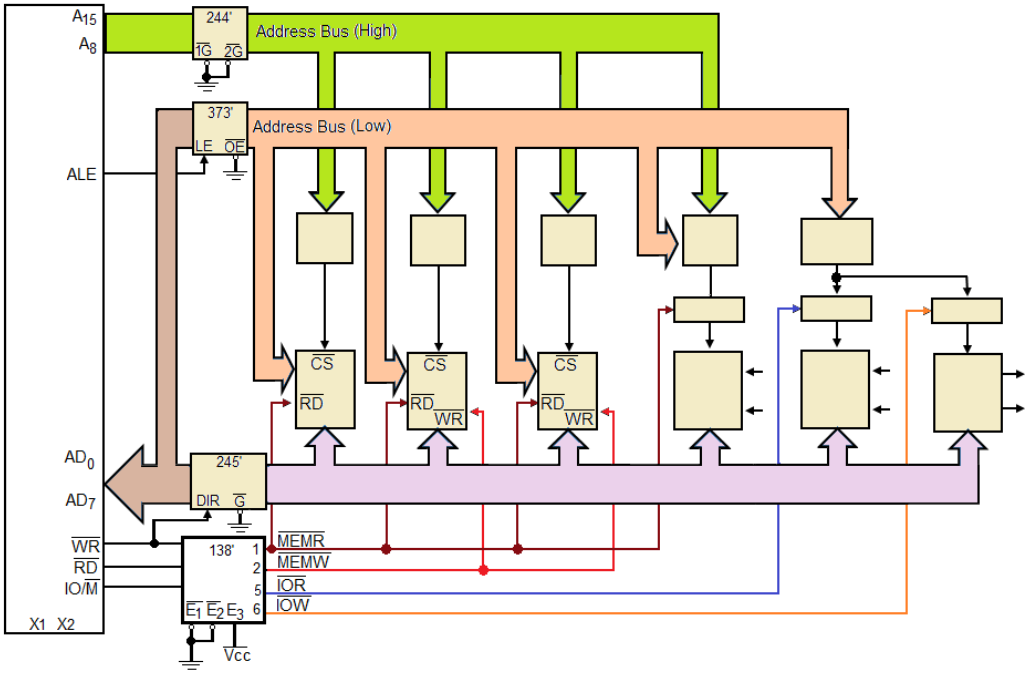
(a) 244 unidirectional buffer for high address bus.

(b) 373 latch for low address bus(note: ALE connected with enabling signal).

(c) 245 bidirectional buffer for data bus (note: direction and enabling signal).

(d) 138 decoder for controlling signals ($\overline{MEMWR}$, $\overline{MEMRD}$, $\overline{IOWR}$, and $\overline{IOWR}$).

2. Draw the required memories and I/O ports includes.



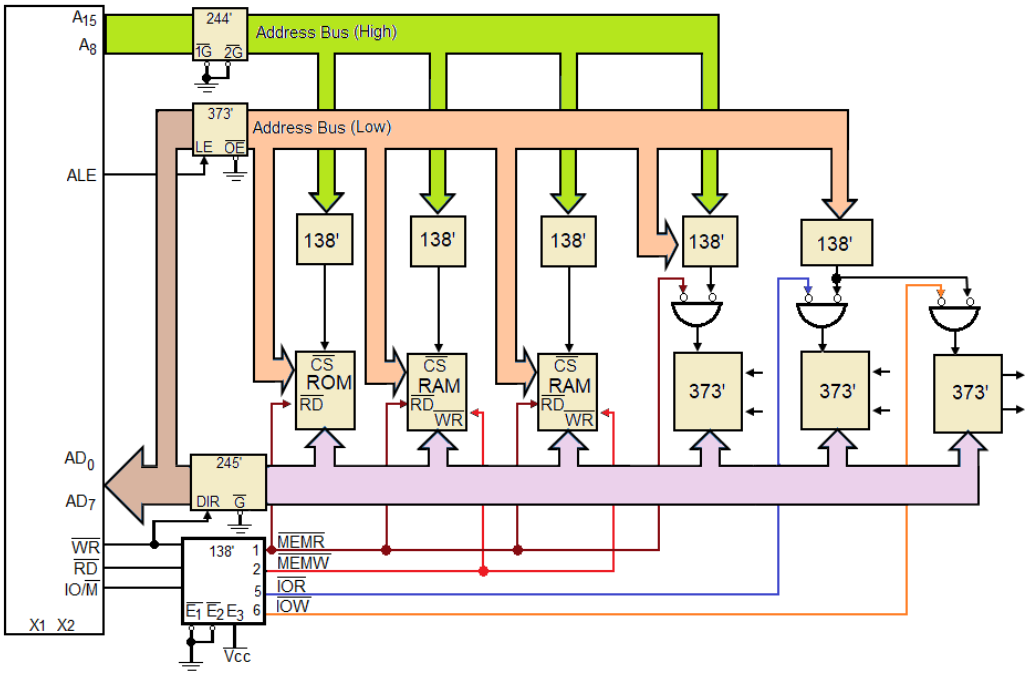
(a) ROM required read signal ($\overline{MEMRD}$), chip select signal ($\overline{CS}$) from 138 decoder, data bus, and required number of address bus.

(b) RAM required read signal($\overline{MEMRD}$), write signal($\overline{MEMWR}$) , and chip select signal ($\overline{CS}$) from 138 decoder, data bus, and required number of address bus.

(c) Memory-mapped I/O (I/O in memory address domain) required read signal($\overline{MEMRD}$) or write signal($\overline{MEMWR}$) according is it (in or out port) , and chip select signal ($\overline{CS}$) from 138 decoder, data bus, and required number of address bus.

(d) Peripheral I/O (I/O in Peripheral address domain) required read signal($\overline{IORD}$) or write signal($\overline{IOWR}$) according is it (in or out port) , and chip select signal ($\overline{CS}$) from 138 decoder, data bus, and required number of address bus.

3. Replace ports with 373' and controlling circuits.



4. calculate the and draw the memory map addresses.

Component	Size	Start address	size	end address
Rom:2732	4K	0000h	0FFF	0FFFh
Rom:2764	8K	1000h	1FFF	2FFFh
IO_in	-	3200h	input port	
RAM	8K	4000h	1FFF	5FFFh
RAM	16K	6000h	3FFF	9FFF
IO_in_out	-	20h	bidirectional port	

5. Draw memory map.red color highlight dynamic bits

0000h	0000 0000 0000 0000	ROM4K
0FFF	0000 1111 1111 1111	
1000	0001 0000 0000 0000	ROM8K
2FFF	0010 1111 1111 1111	
3200	0011 0010 1111 1111	in port
4000	0100 0000 0000 0000	RAM8K
5FFF	0101 1111 1111 1111	
6000	0110 0000 0000 0000	RAM8K
9FFF	1001 1111 1111 1111	

6. It is clear that the last ram consume all address bus bits. Therefor, start from most significant bit (MSB).

7. Is MSB is enough to discriminate between memories sections. It is clear all of them share 0 except portion of last RAM. Therefore select the next bit.

8. Are two MSB is enough to discriminate between memories sections. It is clear two ROM and ports share the same bits 00 and two RAMs share 01. Therefore select the next bit.

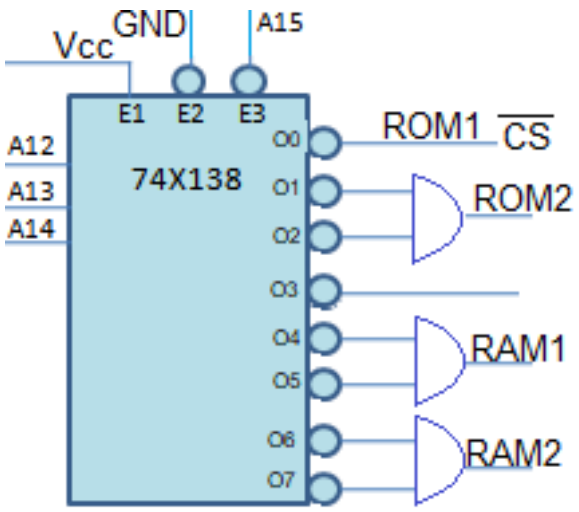
9. Are three MSB is enough to discriminate between memories sections. It is clear two ROM and ports share the same bits 001 . Therefore select the next bit.

10. Are four MSB is enough to discriminate between memories sections.

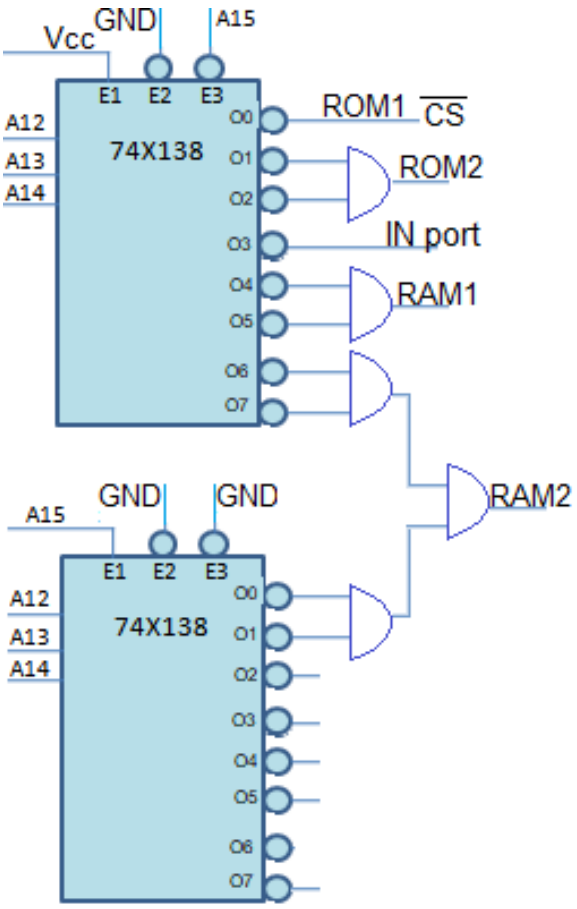
11. Redraw memory map with MSB 4 bit addresses. (Note: write all possible addreses range for each memory section)

0	0000h 0FFF	ROM4K
1 and 2	1000 2FFF	ROM8K
3	3200	in port
4 and 5	4000 5FFF	RAM8K
6, 7, 8 and 9	60FF 9FFF	RAM8K

12. As we know 138 has just 3 input bits plus 3 enable signals.

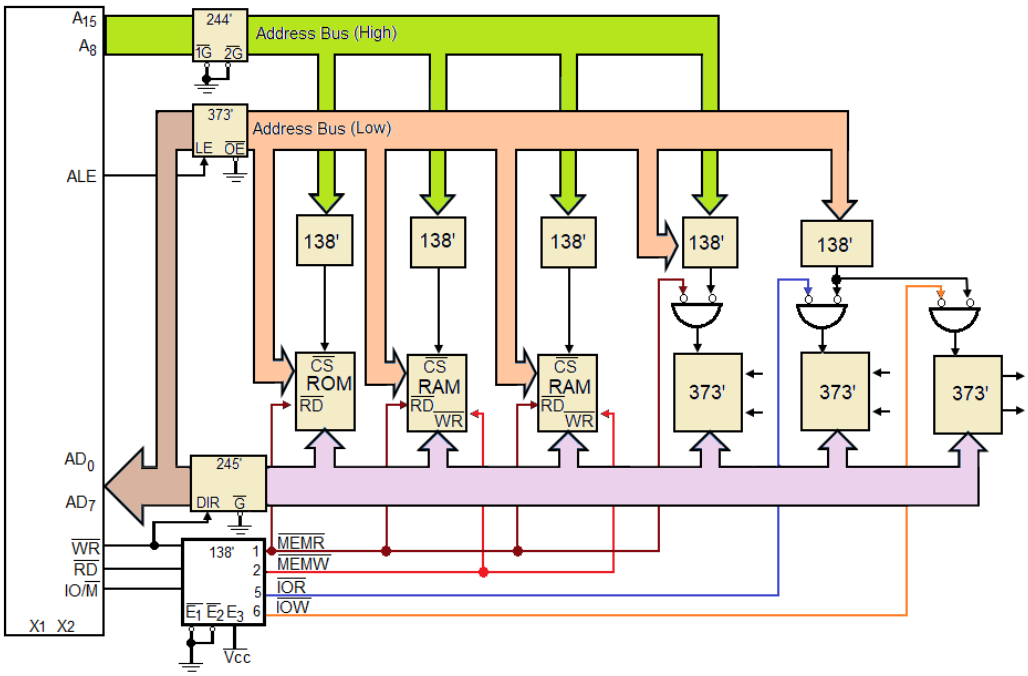


13. As we seen RAM 2 still not complete yet, for that another 138 is required.

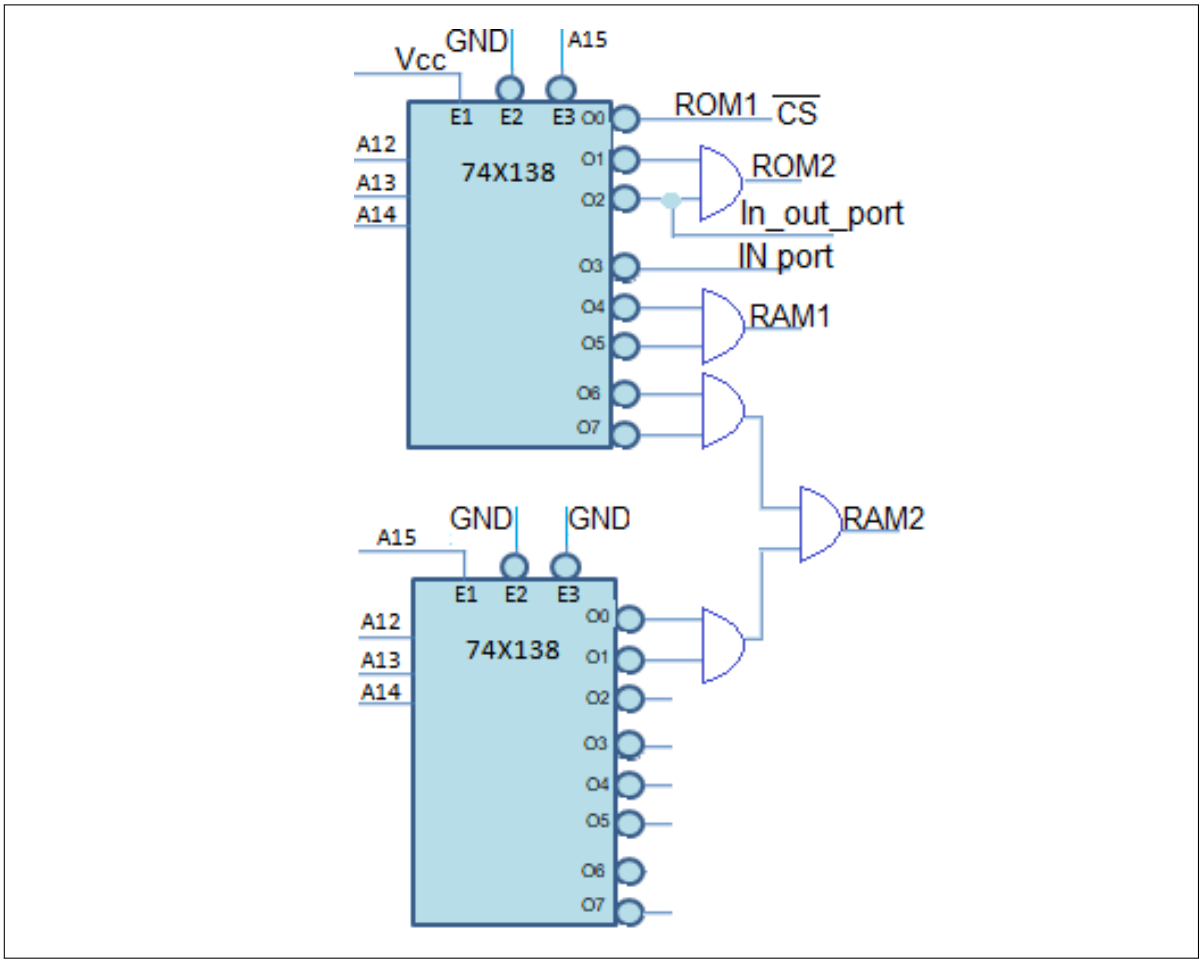


14. Note A15 signal and enabling signals of each 138'.

15. For IO_in_out (address = 20 h), as known for Peripheral I/O, the low and high address bus bytes are same. Therefore, the main kit could be changed to connect the High byte with Peripheral I/O not low as shown in next figure .



16. For the proposed design, we can benefit from the decoding circuit to be used also for Peripheral I/O.


Vcc
GND
A15
E1
E2
E3
O0
O1
O2
O3
O4
O5
O6
O7
A12
A13
A14
74X138
ROM1 CS
ROM2
In_out_port
IN port
RAM1
RAM2
GND
GND
A15
E1
E2
E3
O0
O1
O2
O3
O4
O5
O6
O7
A12
A13
A14
74X138