Introduction to communication protocols

By: Mustafa Shiple

Why Different Bus Types?

- **System Cost**
- Different bus data rates
- Single or multiple Microcontroller
- Unidirectional or Bi-Directional communication
- Simplex or Full Duplex

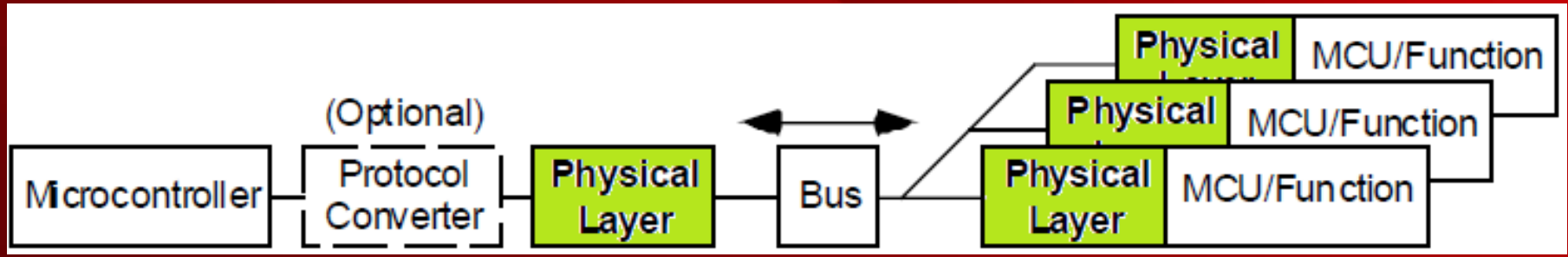
Why Different Bus Types?

- Number of devices on the bus
- Physical Layer requirements
- Message error detection
- Message “through-put”
- Bus bandwidth efficiency
- Differential or single-wire
- Radiated Electro-Magnetic Interference (EMI)
- Noise environment
- Noise immunity

Physical Layer

- A Physical Layer refers to circuitry that translates Microcontroller logic-level signals into bus-level voltage and current signals, and vice versa.
- Microcontroller defines the logic-level signals.
- Microcontrollers are designed for transmitting data short distances.
- Physical layers are designed for single-wire or two-wire bus systems.

Physical Layer Example



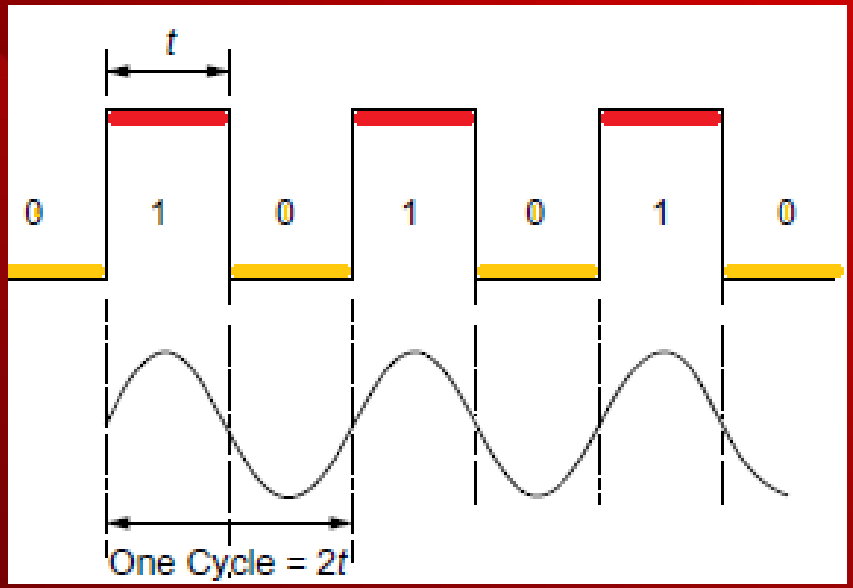
**Exchange between protocol and physical layer

Data Rate Vs. Bandwidth

- Data rate ($R=1/t_b$) b/s
- Channel bandwidth

  $B = 1/2R$ Hz
- Noisy Channel

  $R = B * \log_2(1+S/N)$
  - *S :signal* power
  - *N :noise power in watts.*



What is the difference between Bit Rate and Baud Rate?

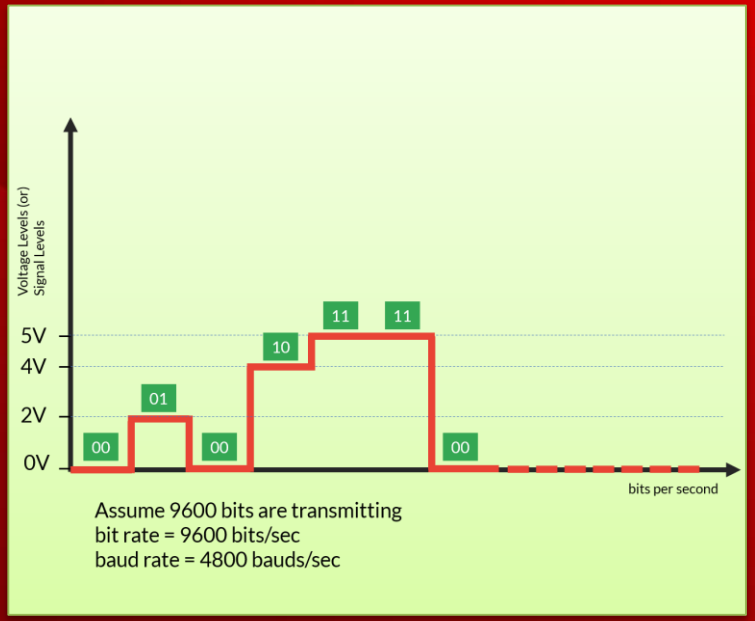
Bit Rate	Baud Rate
Bit rate is the number of bits per second.	Baud rate is the number of signal units per second.
It determines the number of bits traveled per second.	It determines how many times the state of a signal is changing.
Cannot determine the bandwidth.	It can determine how much bandwidth is required to send the signal.
This term generally used to describe the processor efficiency.	This term generally used to describe the data transmission over the channel.
Bit rate = baud rate x the number of bits per signal unit	Baud rate = bit rate / the number of bits per signal unit

Example 1

An analog signal carries 4 bits in each signal unit. If 1000 signal units are sent per second, find the baud rate and the bit rate

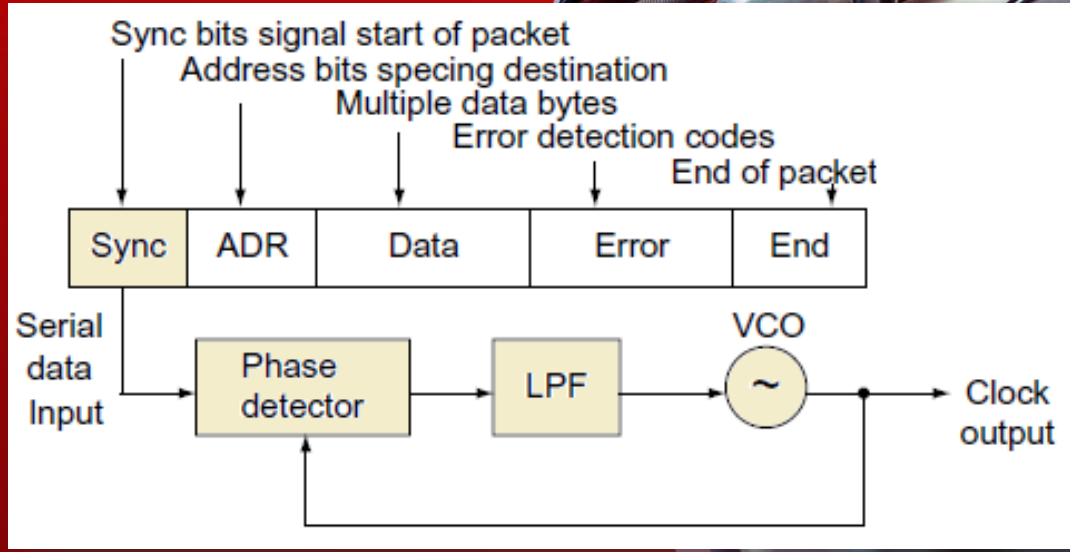
Solution

Baud rate = 1000 bauds per second (baud/s)
Bit rate = 1000 x 4 = 4000 bps



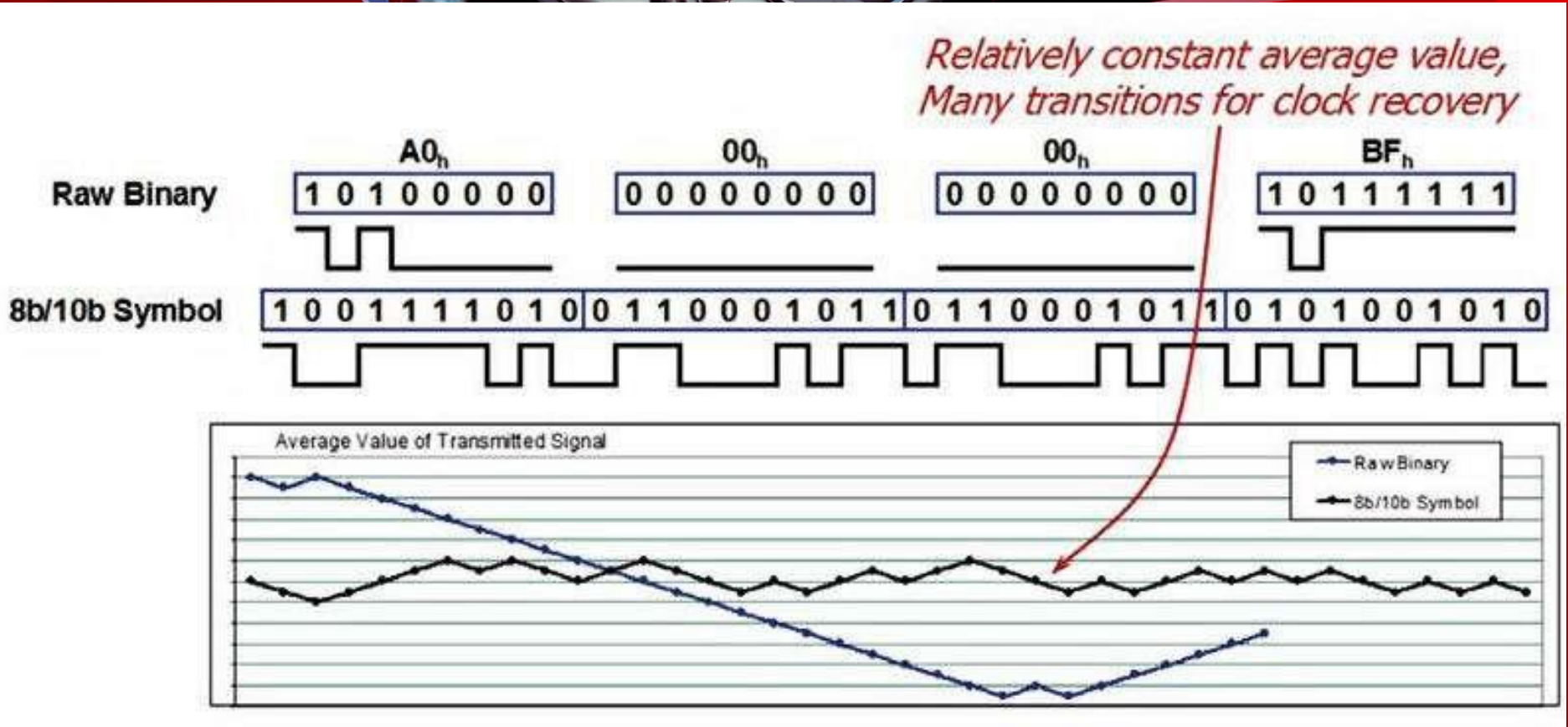
Clock and Data Recovery (CDR)

- One problem is a long sequence of binary 0s or 1s.
- To overcome 8b/10b conversion or coding. This provides a zero DC.
- High-speed systems a similar technique called 66b/64b. Overhead is only 3.125%



- Bit scrambling, It helps the DC balance problem

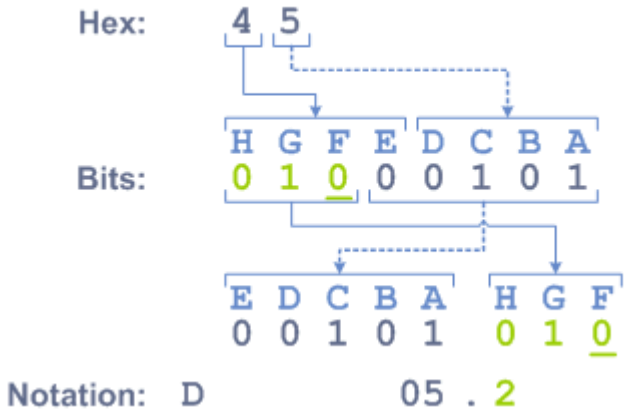
Zero Balance



8b/10b

Running disparity (RD)=#number 1-#number 0

Notation

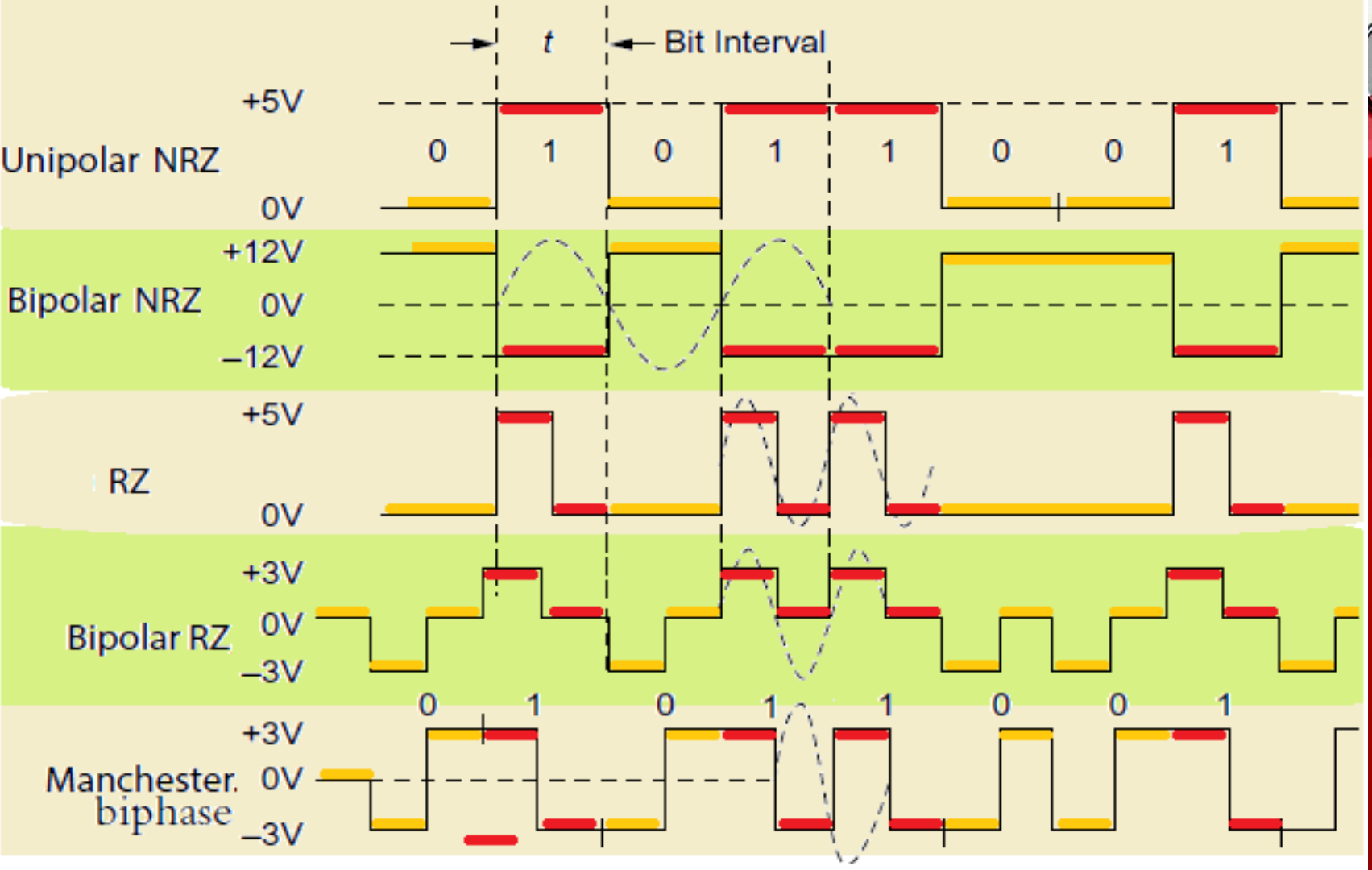


5b/6b code

Input		RD = −1	RD = +1
	EDCBA	abcdei	
D.00	00000	100111	011000
D.01	00001	011101	100010
D.02	00010	101101	010010
D.03	00011	110001	
D.04	00100	110101	001010
D.05	00101	101001	
D.06	00110	011001	
D.07	00111	111000	000111
D.08	01000	111001	000110
D.09	01001	100101	
D.10	01010	010101	
D.11	01011	110100	
D.12	01100	001101	
D.13	01101	101100	
D.14	01110	011100	
D.15	01111	010111	101000

3b/4b code

Input		RD = −1	RD = +1
	HGF	fghj	
D.x.0	000	1011	0100
D.x.1	001	1001	
D.x.2	010	0101	
D.x.3	011	1100	0011
D.x.4	100	1101	0010
D.x.5	101	1010	
D.x.6	110	0110	
D.x.P7 †	111	1110	0001
D.x.A7 †	111	0111	1000

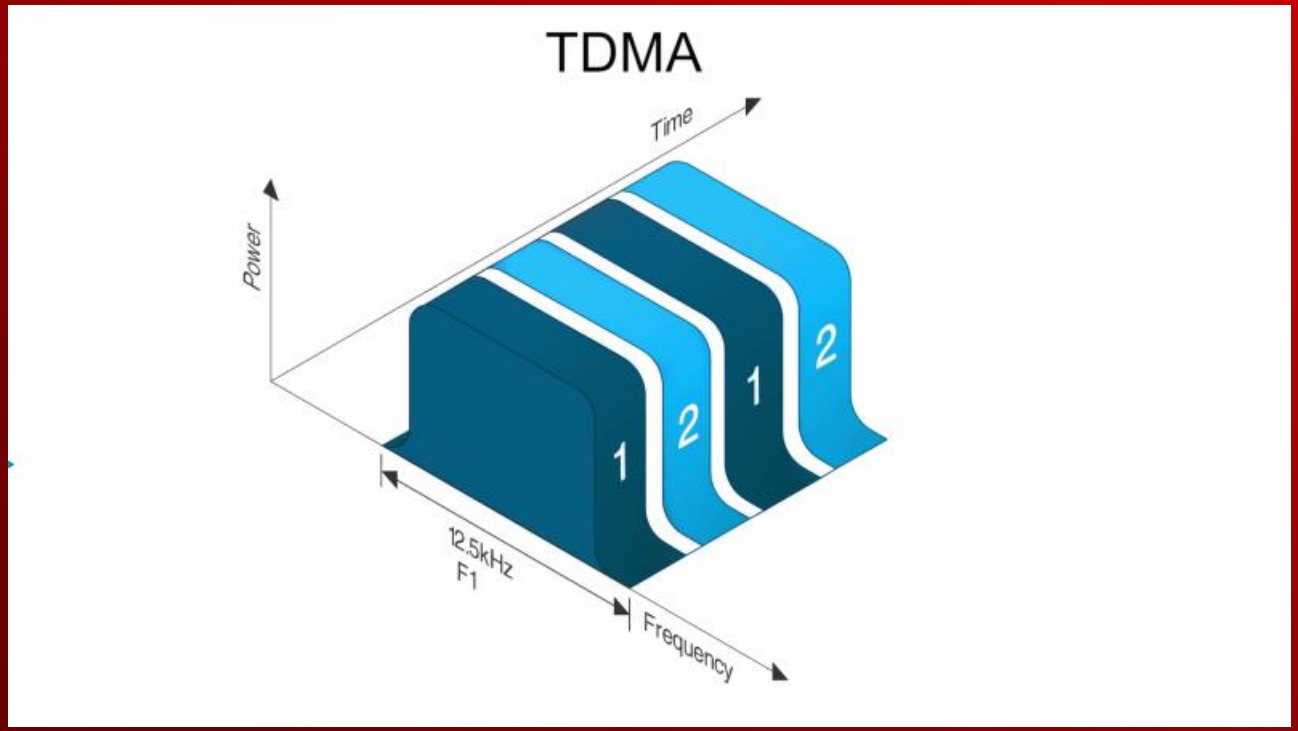

t
Bit Interval
+5V
Unipolar NRZ
0
1
0
1
1
0
0
1
0V
+12V
Bipolar NRZ
0V
–12V
+5V
RZ
0V
+3V
Bipolar RZ
0V
–3V
0
1
0
1
1
0
0
1
+3V
Manchester.
biphase
0V
–3V

Line Codes

Access Methods

- **Master-Slave**
  - **Master control the communication over media**
  - A common technique is polling of the slaves in sequence.
- Carrier sense multiple access (CSMA)
  - Listen before transmitting/collision or interference
  - CSMA/CD : CSMA incorporates a collision detection (CD) technique.
- Time division multiple access (TDMA)
  - This time is divided to slots, one for each node on the shared medium.

TDMA



Mastering

- Masters are used to manage bus operations.
- There are Single and Multi-Master bus systems.
  - Each Master in a bus system typically requires a microcontroller.
  - Only one Master is allowed to assume Mastership of the bus at any time to eliminate bus contentions.

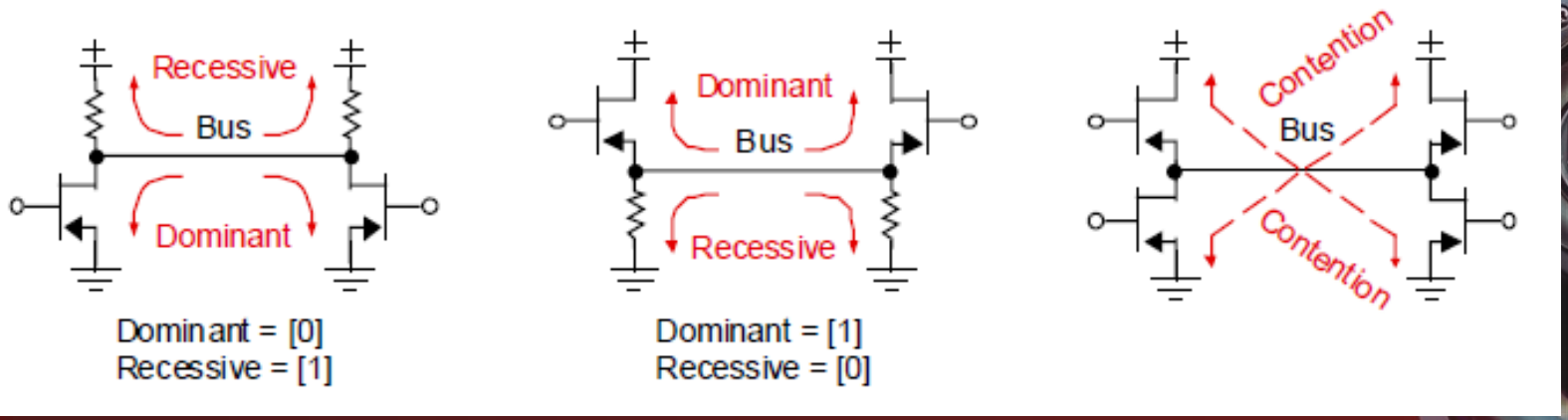
Multi-Master system

- Advantage
  - Ability to control the bus from more than one Node
- Disadvantages
  - Bus access availability is dependent on activity.
  - Time critical systems have to be designed for very high speeds to guarantee message delivery in worst case time.
  - Multiple Masters increases the complexity of the system.

Determinism

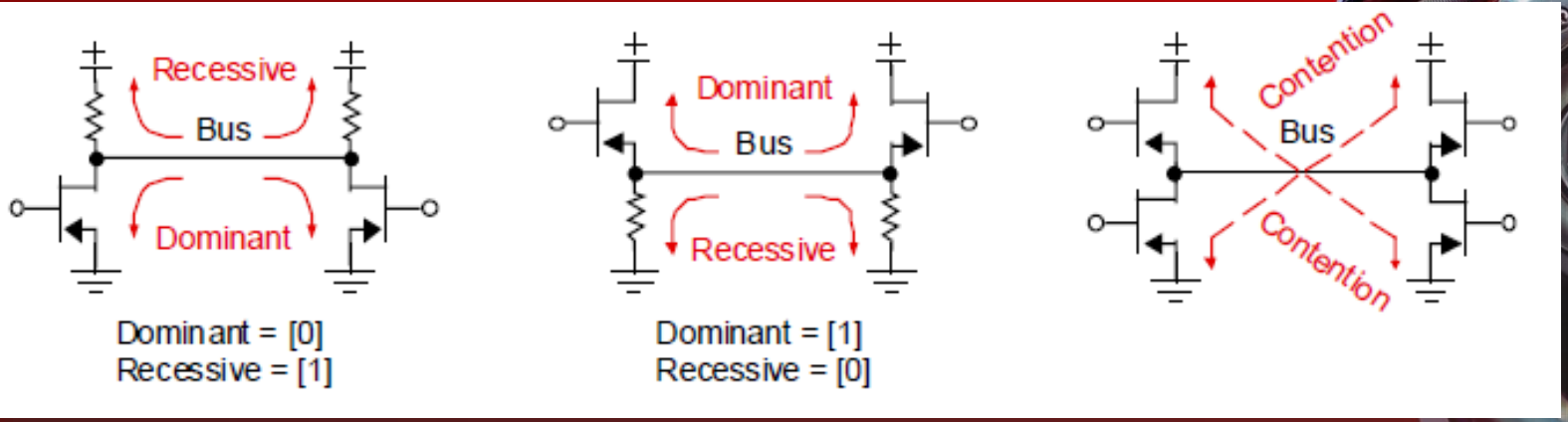
- Determinism describes the degree of access a Master has to the bus at any particular time.
- Collision Handling greatly impacts the degree another Master has to the bus.
- Full Determinism is where a Master has immediate access to the bus at any time.

Dominant vs. Recessive



1. Dominant and Recessive relate to voltage states of the bus.
2. Dominant state: Bus voltage is pulled high or low by means of an active switch element
3. Recessive state: Bus is pulled high or low by means of a passive element
4. Contention exists when two or more Nodes using their active switch elements.

Dominant vs. Recessive

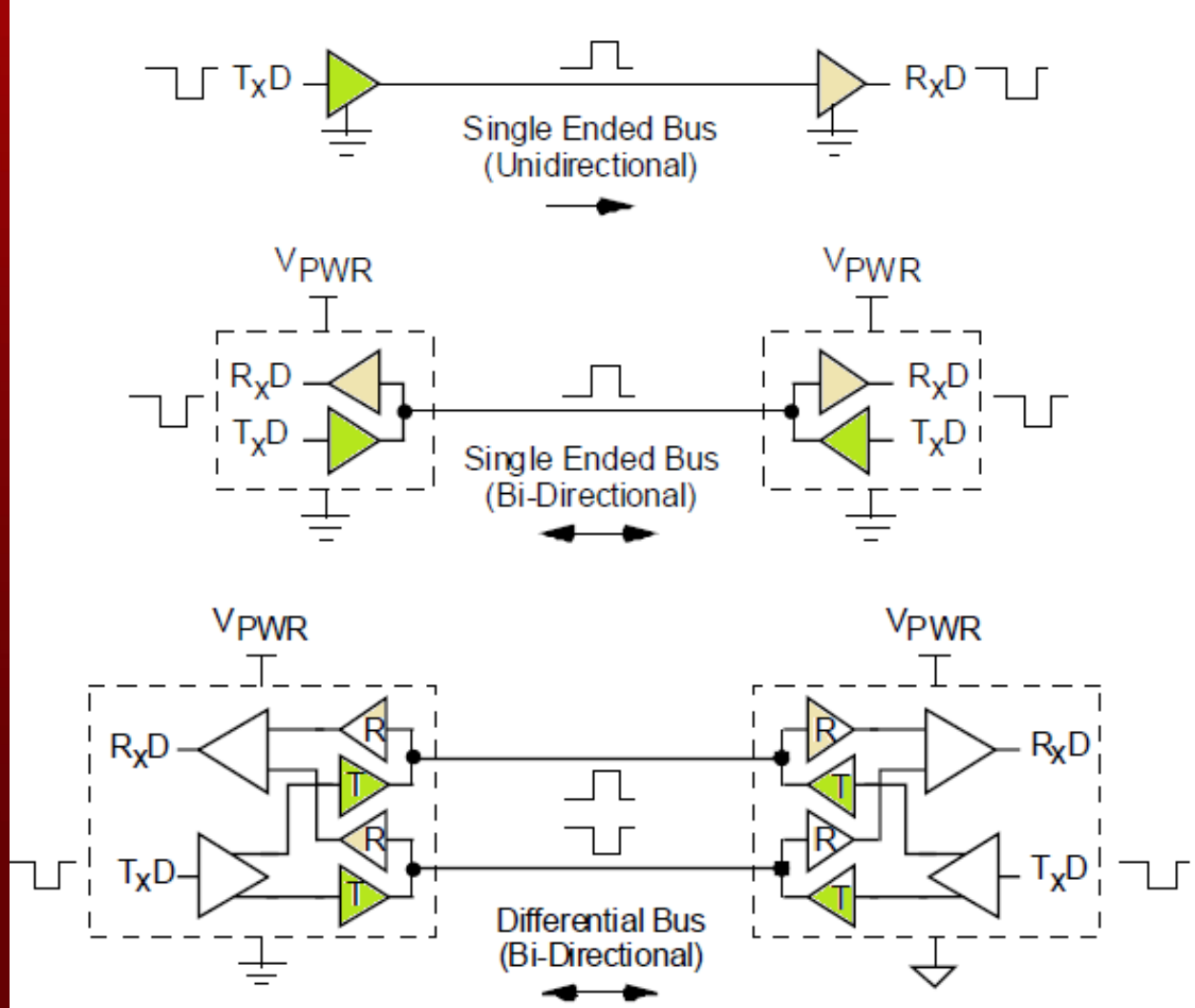


4. Contentions must be resolved before meaningful communication can occur.
5. Dominant / Recessive contentions are resolved by the Dominant “over-powering” the Recessive.
6. Simultaneous Dominant High / Dominant Low contentions are not allowed by bus design.

Collision Handling

- Ability to resolve simultaneous Dominant / Recessive signal collision conflicts
  - Advantages
    - Non-destructive collision
    - Allows prioritization of signals
  - No bus recovery time required
- Contention Back-Off: Advantages
  - Higher data speeds are possible by using higher drive power.

Single Ended and Differential Busses



Error Detection Types

- Cyclical Redundancy Check (CRC)
  - Error checking scheme capable of catching more than one bit in error
  - CRCs are more than one bit in length.
- Framing Error Check
  - Detects an incorrect number of bits in a frame (data field)
- Parity Error Check
  - Can not detect more than one error.

Safety and Fault Tolerance

Informational Redundancy

Adding useful information as meta-information, e.g. for error detection and error correction.

Communication system is extended by adding components unnecessary for basic operation

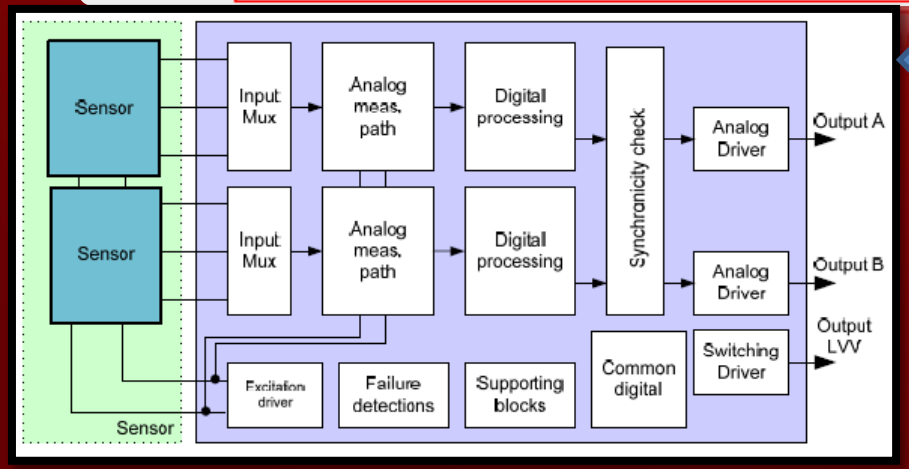
Structural Redundancy

Failure Modes and Effects Analysis (FMEA)

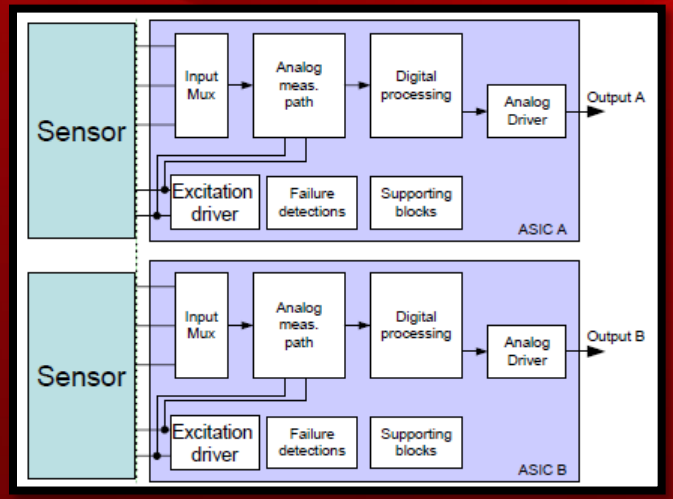
Failsafe logic: System FMEA

In case something goes wrong then **disable** ABS functions but "normal" braking can still be performed by driver.

Partial Redundant



Full Redundant



Static Redundancy

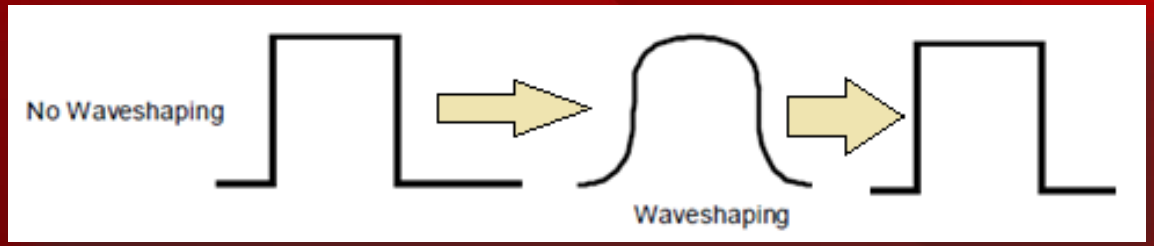
Continually active

Informational Redundancy

Not activated until errors occur.

Dynamic Redundancy

Equalization



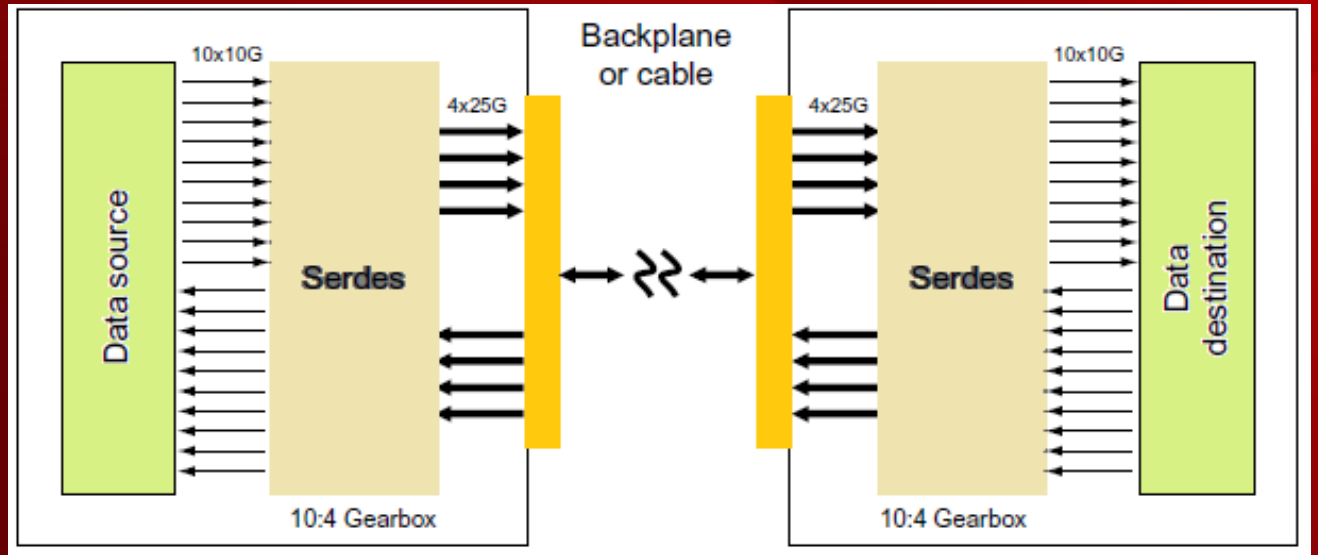
- The cables act as LPFs that effectively attenuate the high frequency. content of the signal producing a rounding effect.
- This effect can be eliminated by using equalization

Bit Banging

- The process of implementing serial I/O procedures in software in an embedded microcontroller.
- The term can apply to any other serial protocol implemented in software rather than in a specific interface IC.

Gearbox Operations

- Translate serial data to a serial stream at a higher or lower data rate.



Composability

- is a System design principle that deals with the inter-relationships of components.

Composable Communication Architectures

- Changing the functionality of one ECU not affect the functionality of other ECUs.

Compare between Asynchronous and Synchronous

Asynchronous Communication	Synchronous Communication
There is no common clock signal between the sender and receivers.	Communication is done by a shared clock.
Sends 1 byte or character at a time.	Sends data in the form of blocks or frames.
Slow as compare to synchronous communication.	Fast as compare to asynchronous communication.
Overhead due to start and stop bit.	Less overhead.
Ability to communicate long distance.	Less as compared to asynchronous communication.
A start and stop bit used for the data synchronization.	A shared clock is used for the data synchronization.
Economical	Costly
RS232, RS485	I2C, SPI.