Serial Communication basics

الدكتور مصطفى شيل

INTER-INTEGRATED CIRCUIT PROTOCOL

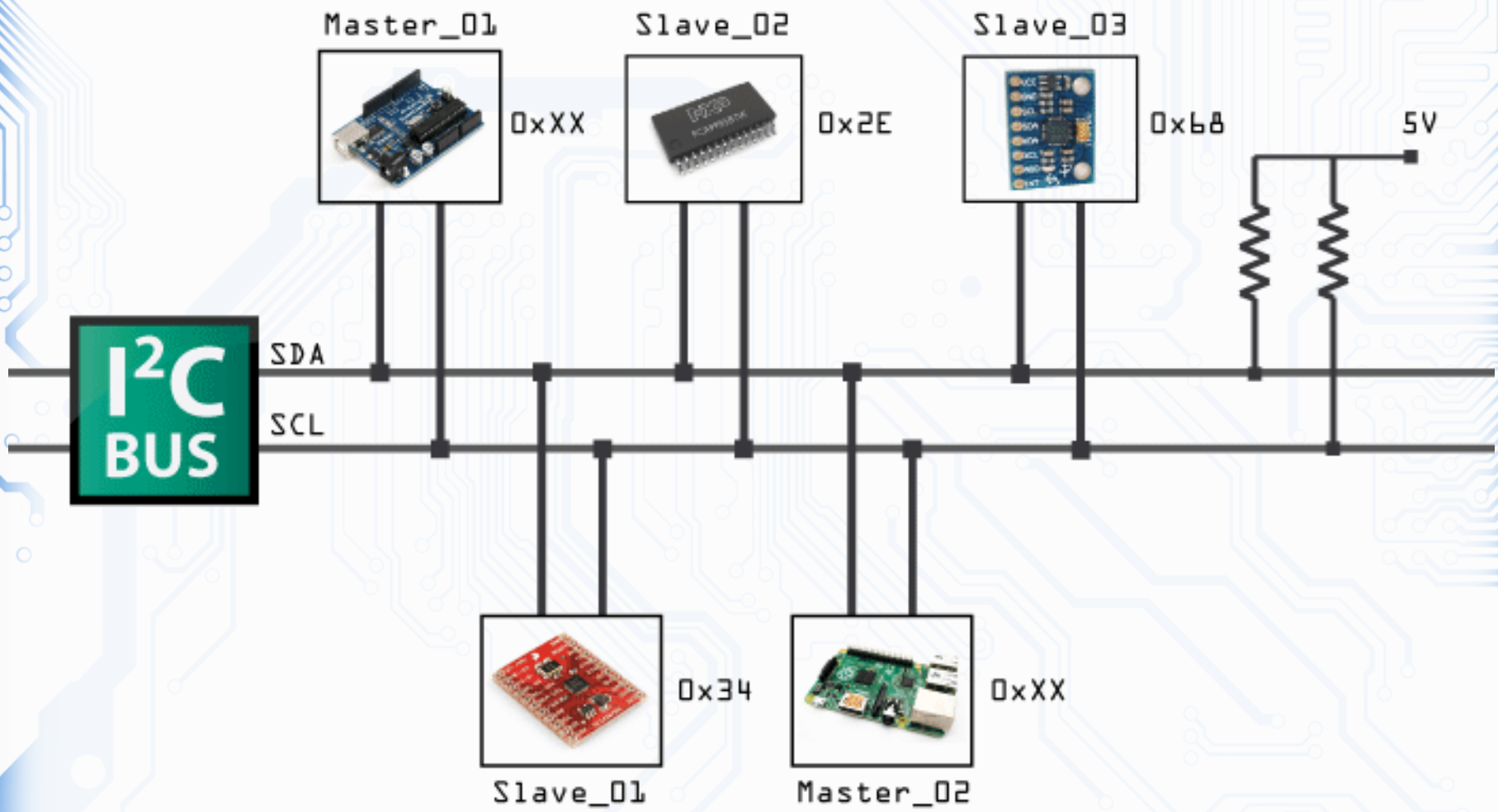
Eye on History

- 1982 by Philips Semiconductor (now NXP Semiconductors).
- 2006, no licensing fees are required to implement the I²C protocol.

I2C Features

- Two bus lines are required (SCL, SDA)
- No strict baud rate, the master generates a bus clock
- Simple master/slave relationships exist between all components
- Each device connected to the bus is software-addressable by a unique address
- I2C is a true multi-master bus providing arbitration and collision detection

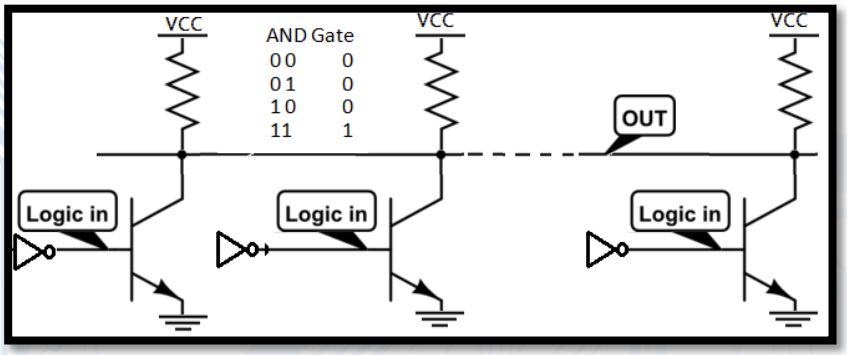
I2C Configuration

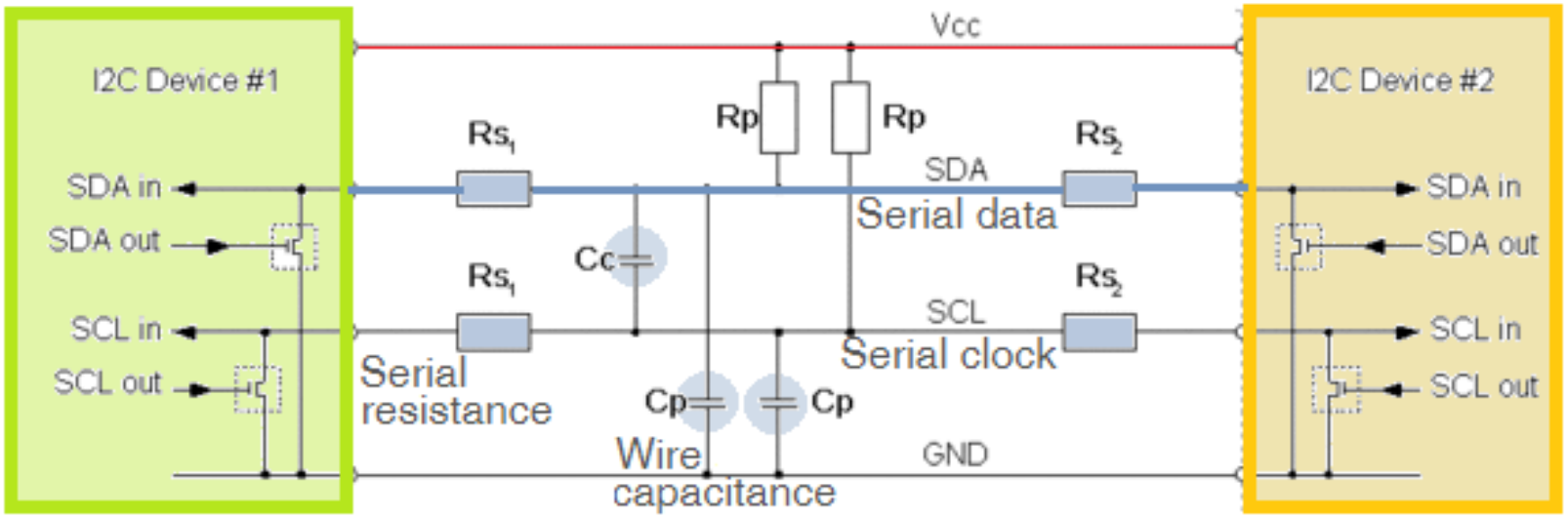


PHYSICAL LAYER

Physical Layer:

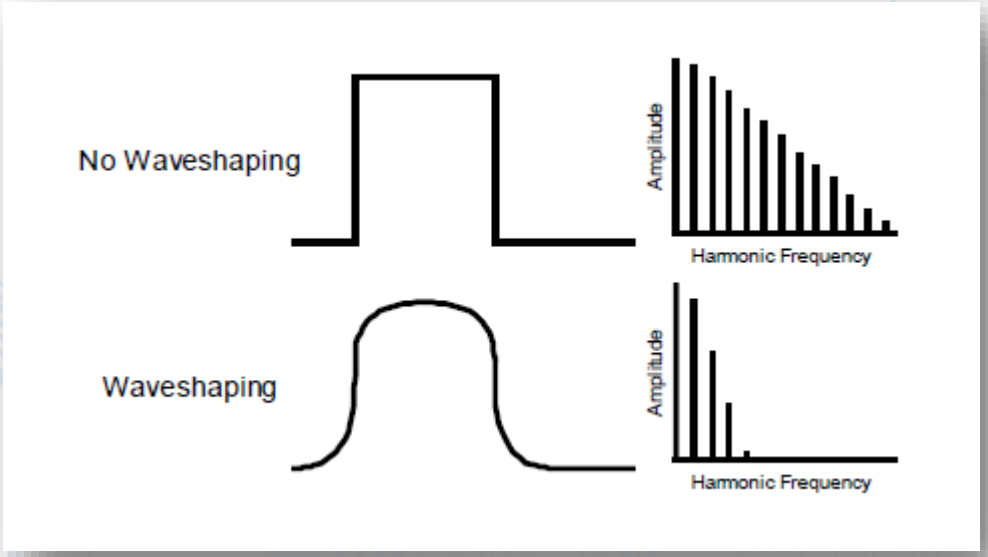
Open-Collector/Drain



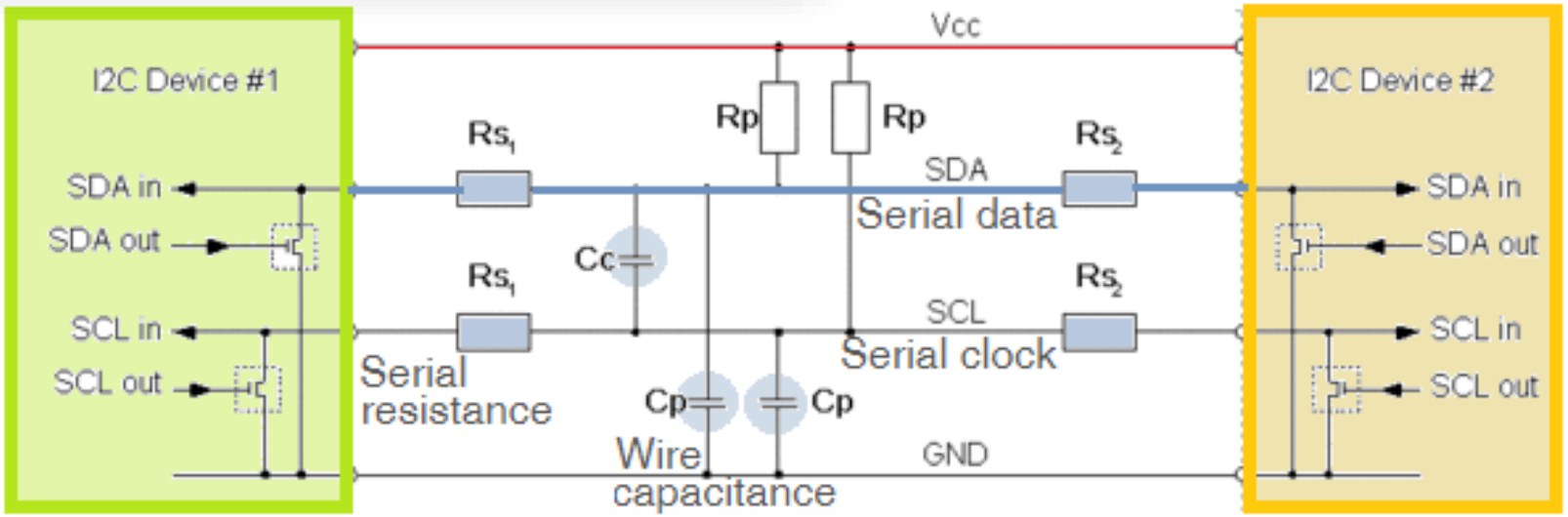


Cc	Cross channel capacitance
Rp	Pull-up resistance

Physical Layer:
Wave shaping



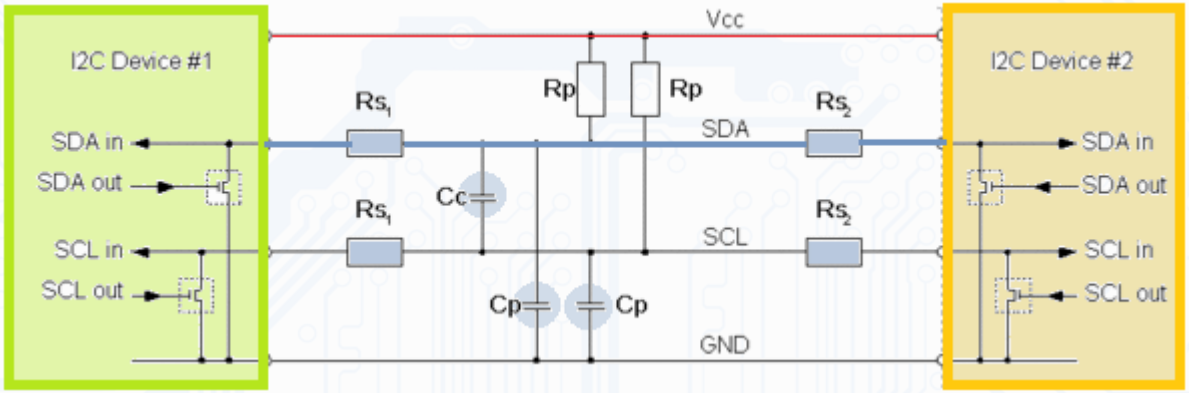
** Spreading pulse

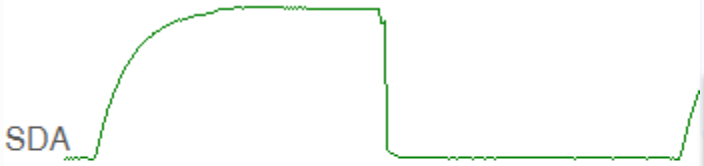


Cc	Cross channel capacitance
Rp	Pull-up resistance

Effect of cable length

Rp = 10 kΩ and Cp = 300 pF. The SCL clock runs with 100 kHz.

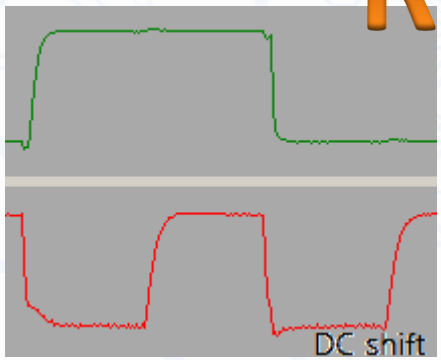




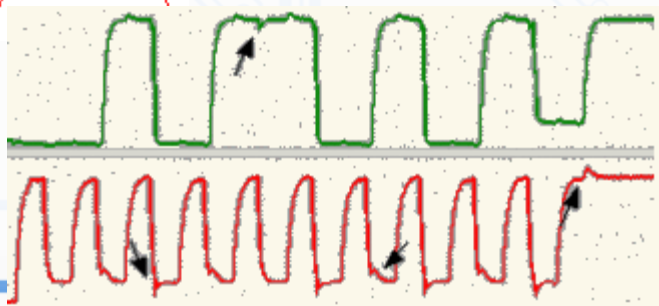
Cp

$$\text{low level}\Big|_{\text{slave}} = Vcc\,\frac{Rs}{Rs + Rp}$$

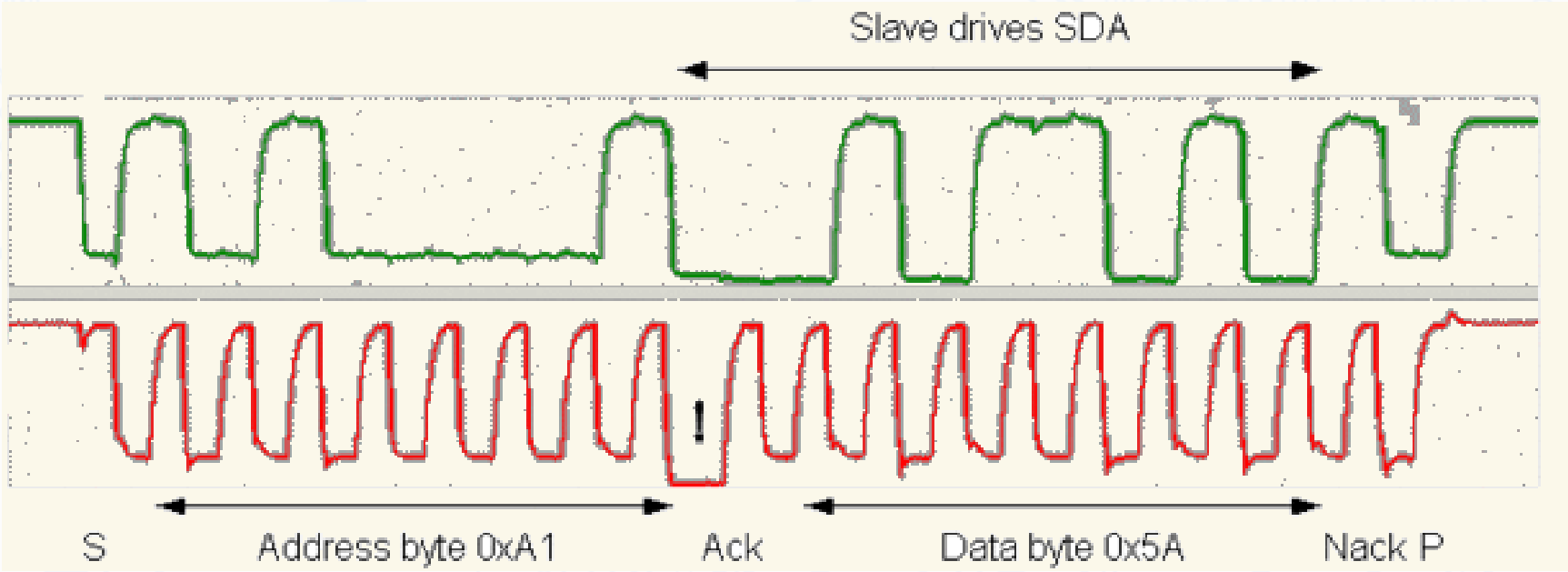
Rs



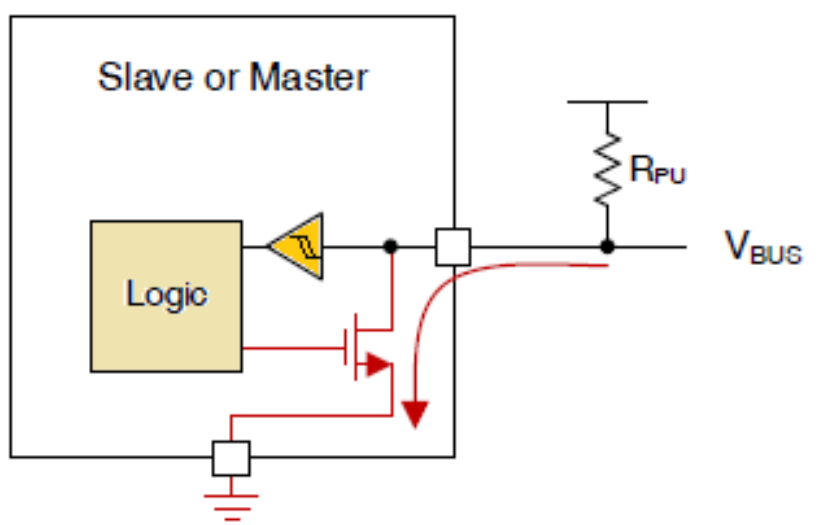
Cc

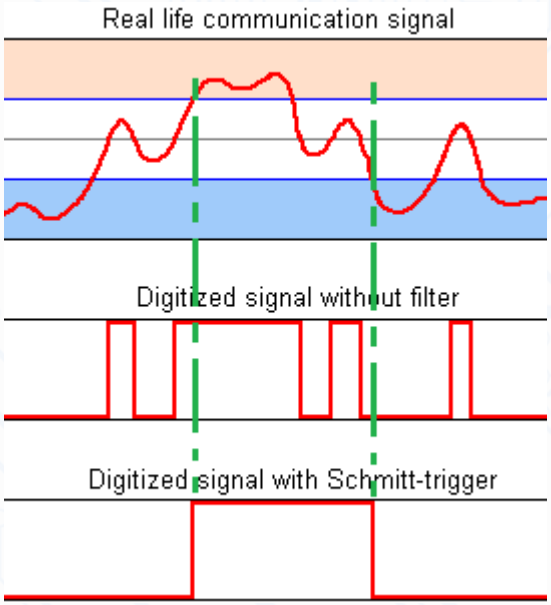


Rs as Debugging



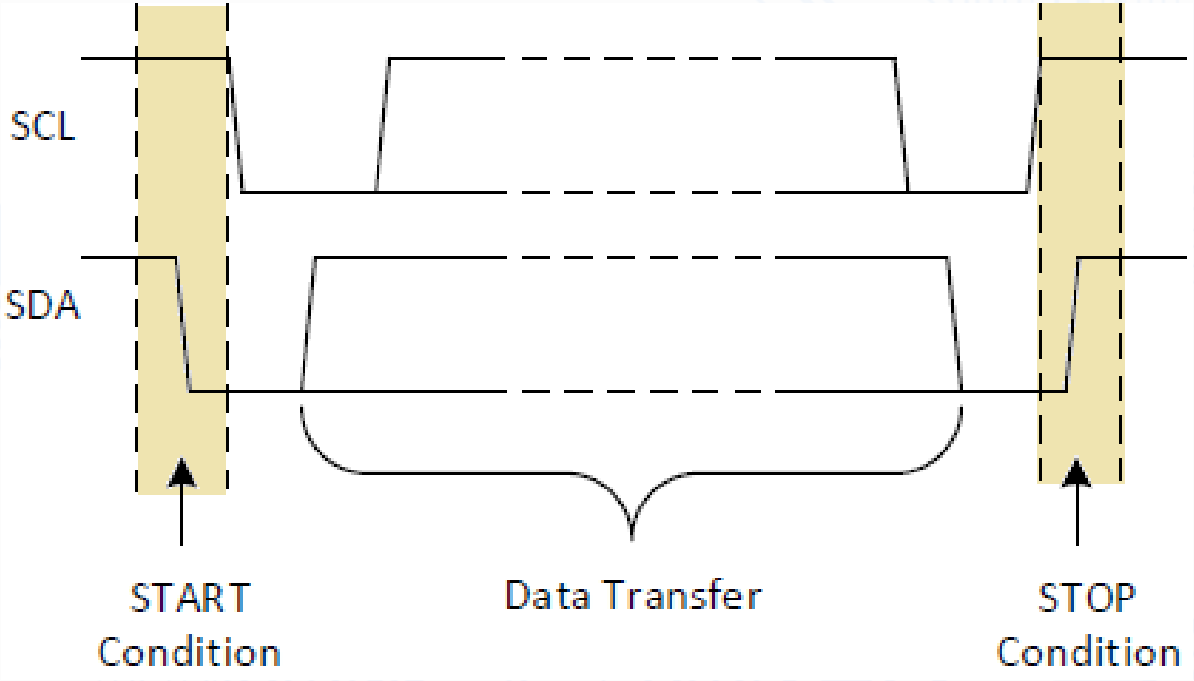
Physical Layer:
Schmitt Gates



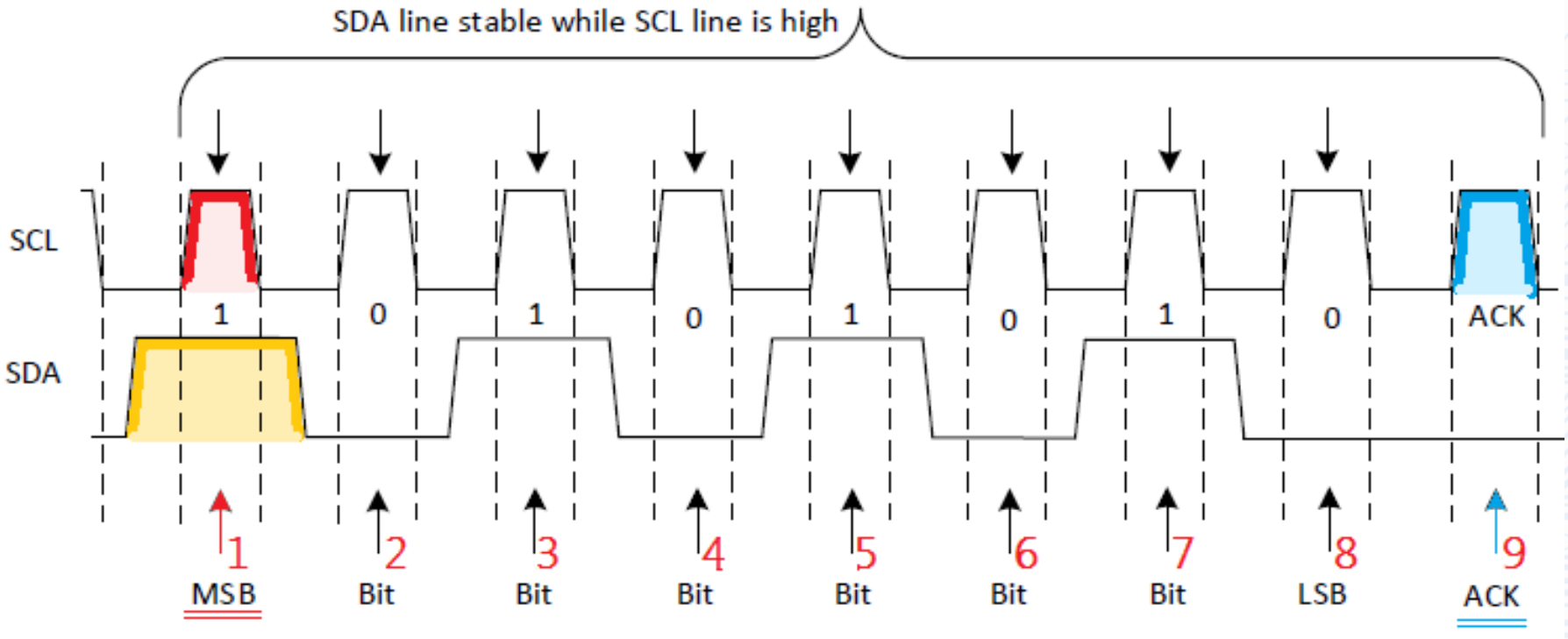


- ***Bit Timing: Non Return to Zero (NRZ)*** 1= “recessive” and 0=“dominant”

Start/Stop bits



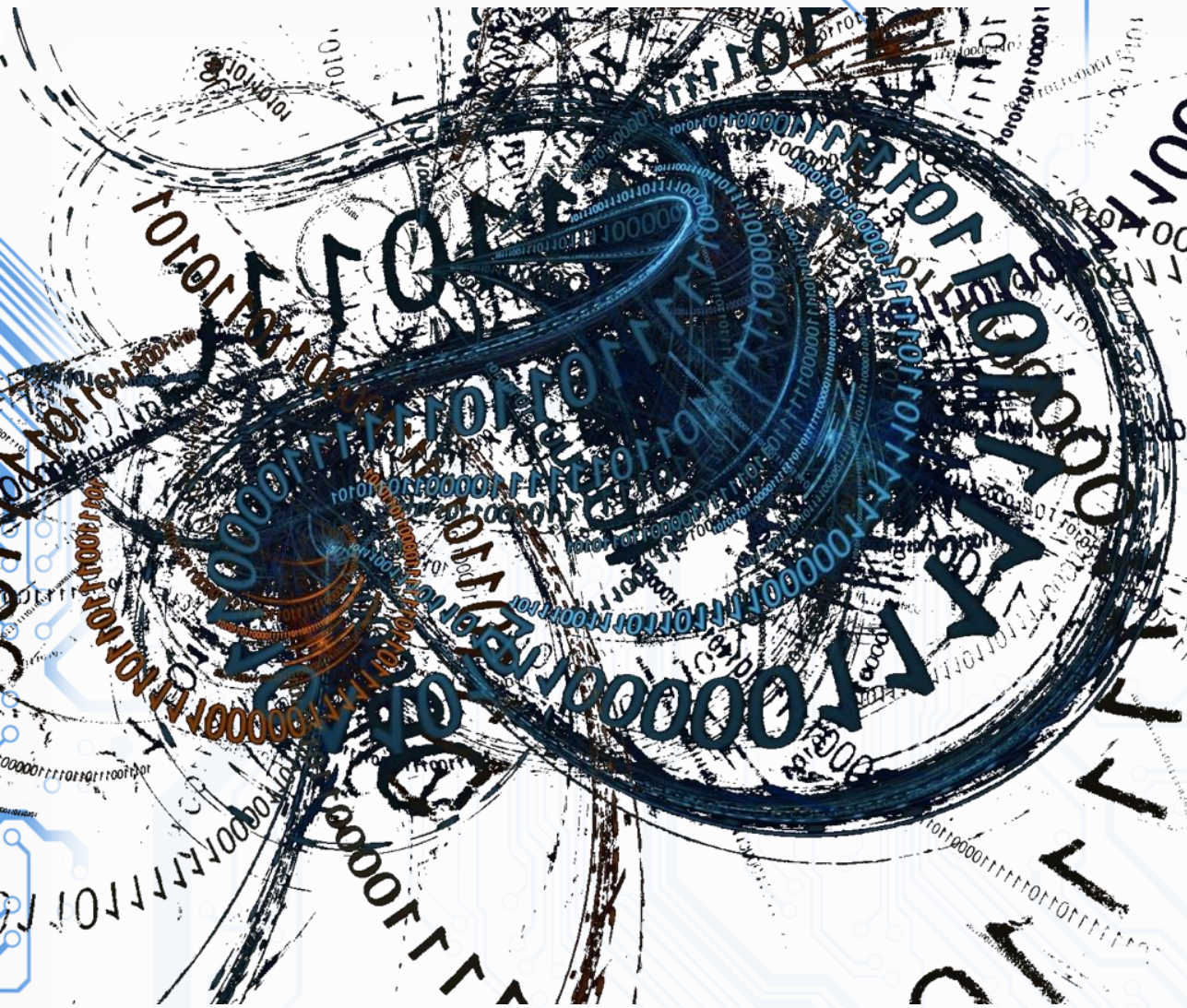
Data Byte



Each byte of data (including the address byte) is followed by one ACK/NACK bit from the receiver

Requirements For Devices

1. Both, SDA and SCL, must be open drain.
2. In most I2C buses, the low and high input voltage level thresholds of SDA and SCL must depend on Vcc.
3. The SCL and SDA signals must be sampled by Schmitt Trigger inputs, i.e. with a certain hysteresis.
4. Spikes in SCL and SDA signals must be filtered .
5. Setup and hold times; this includes a specified maximum SCL clock rate (100 kHz for normal speed, 400 kHz for full speed).

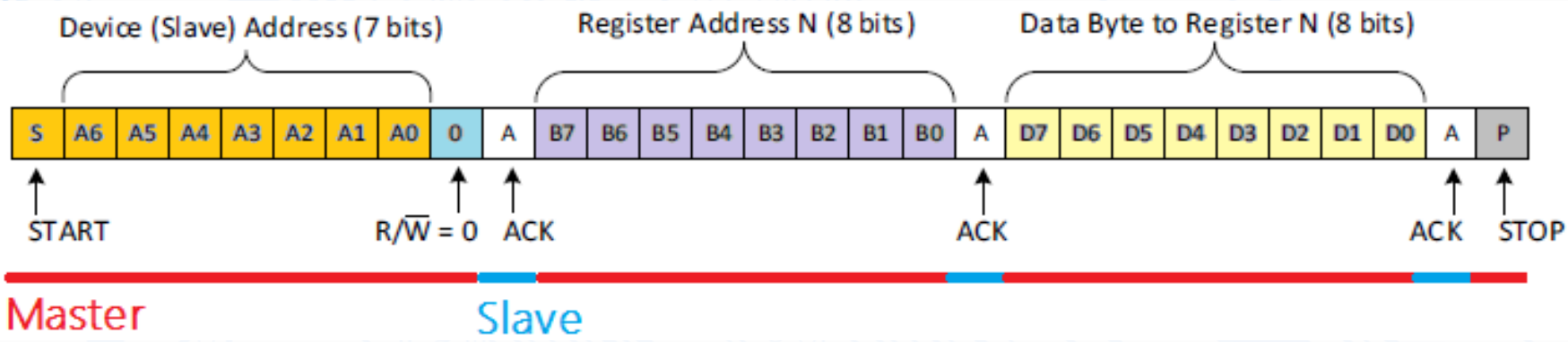


DATA LINK LAYER

Data Frame:

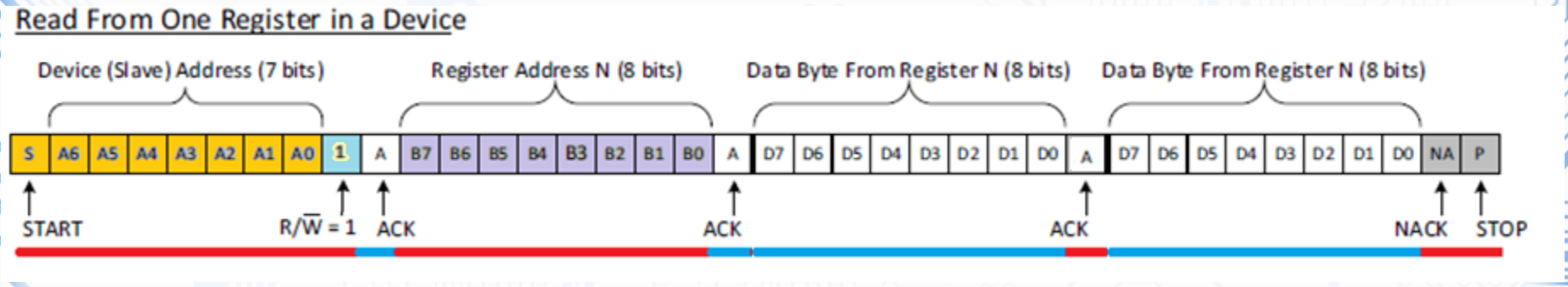
Write to One Register in a Device

- Data byte field could be more thane one byte



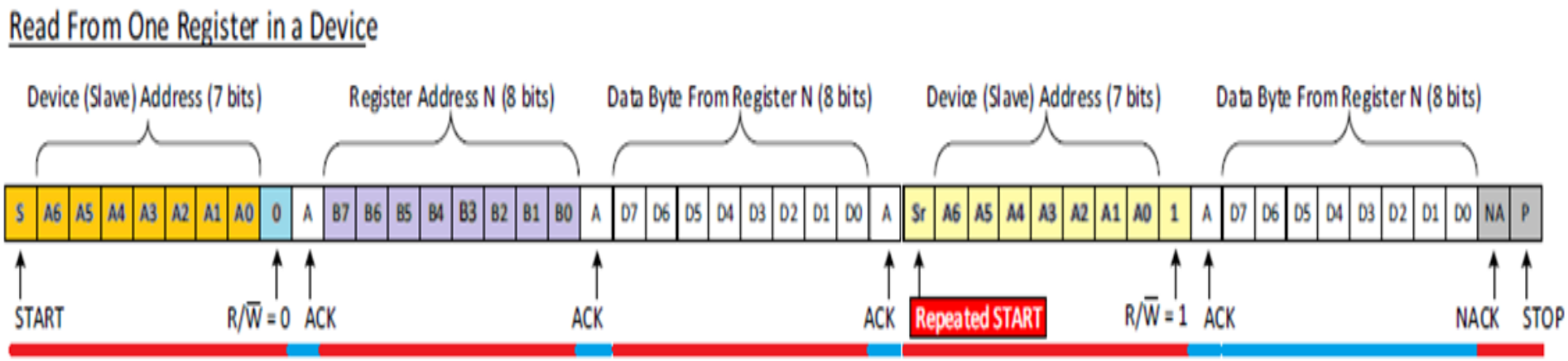
Data Frame:

Read From One Register in a Device



Data Frame:

Multiple frames From One Master

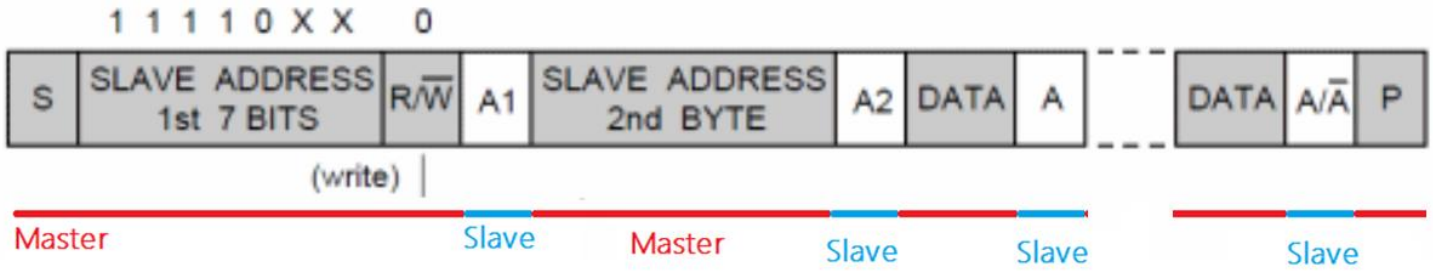


Not Acknowledge

1. The receiver is unable to receive or transmit because it is not ready to start communication with the master.
2. During the transfer, the receiver gets data or commands that it does not understand.
3. During the transfer, the receiver cannot receive any more data bytes.
4. A master-receiver is done reading data and indicates this to the slave through a NACK.

Extension of the I2C Specifications

Read/write 10 bit Address



SPI

Serial Peripheral Interface
PROTOCOL

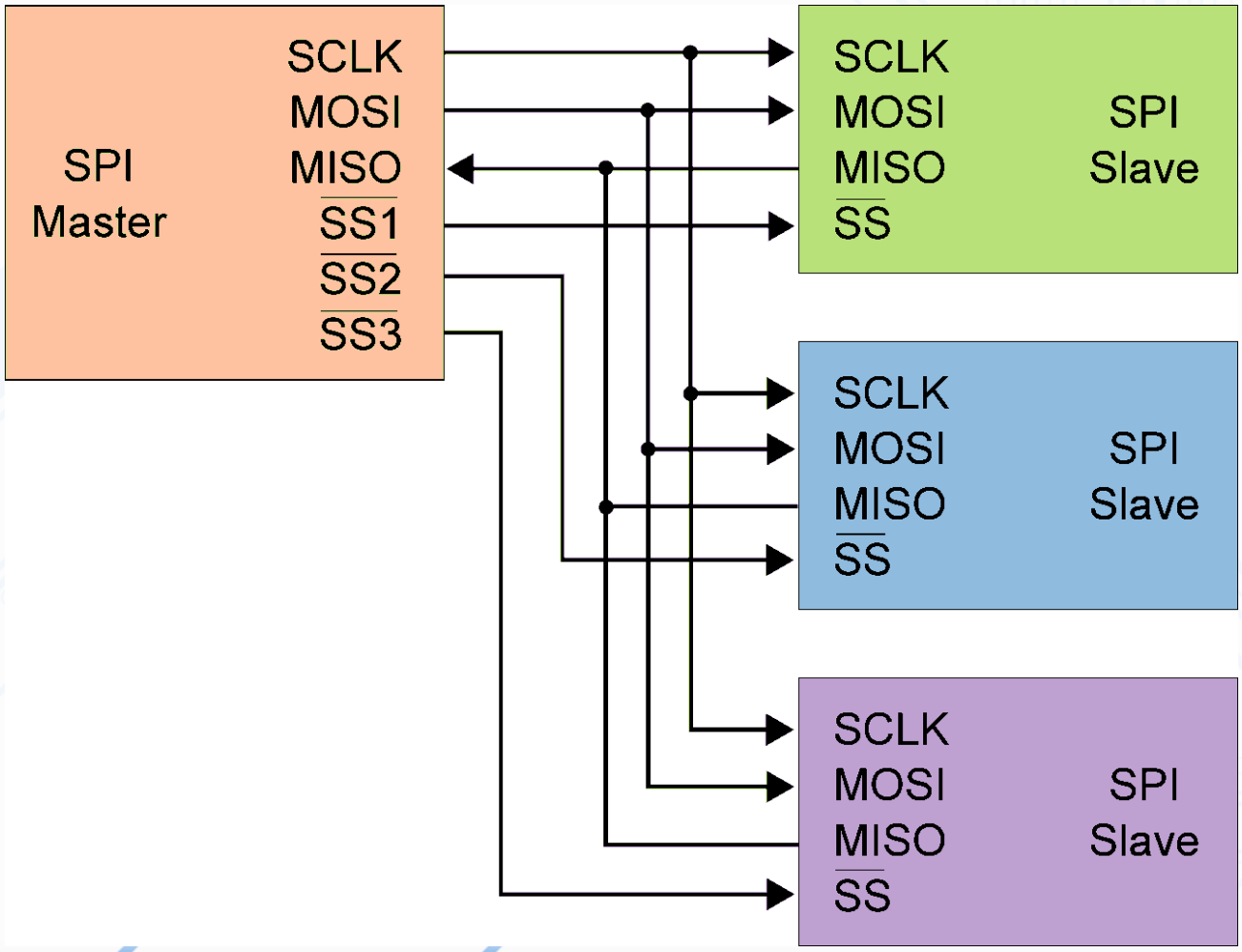
Eye on History

1. By Motorola company (now Freescale), in the Mid 1980.

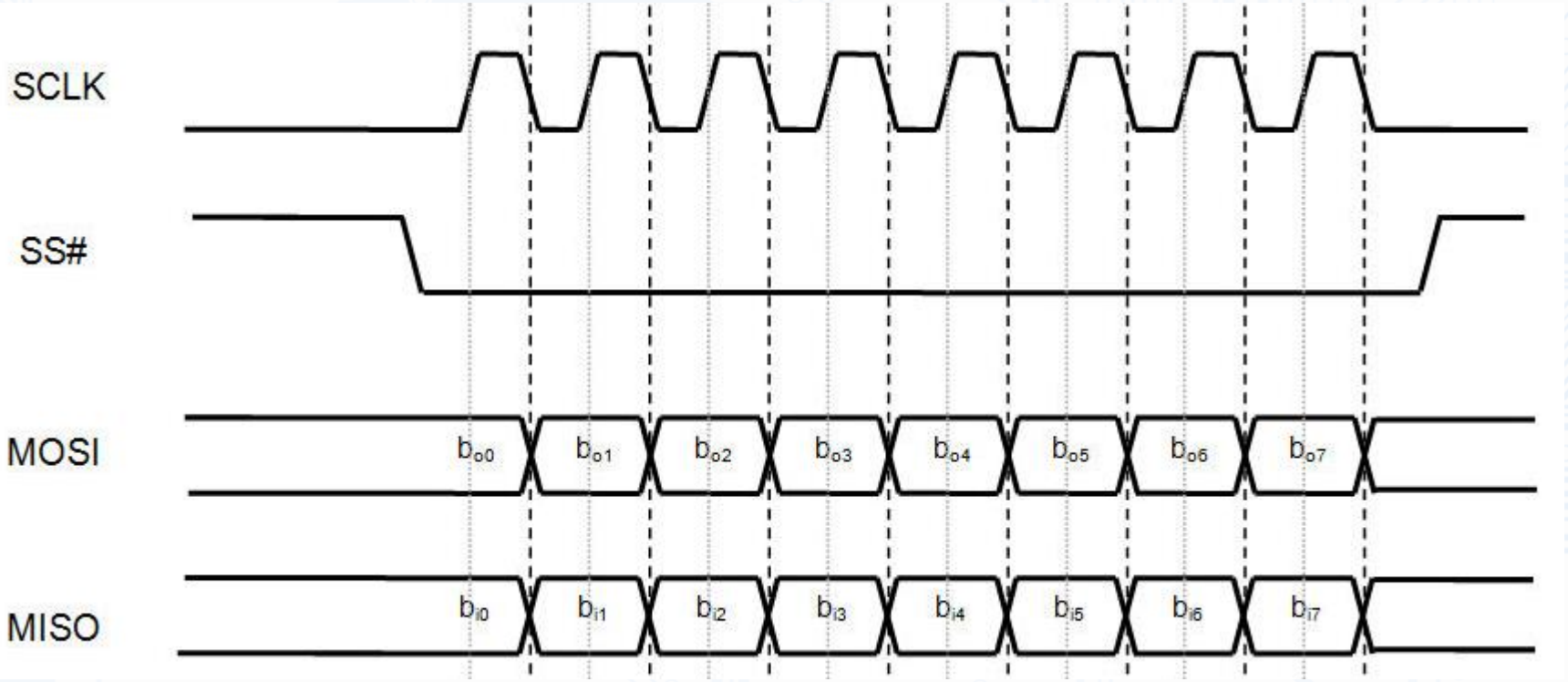
SPI communication

- Synchronous serial communication interface
- Complete protocol flexibility for the bits transferred, not limited to 8-bit words
- Requires 2 or 3 wires for the communication +1 wire for each device in the bus
- Slaves send data to master at the same time when master is sending data to them.

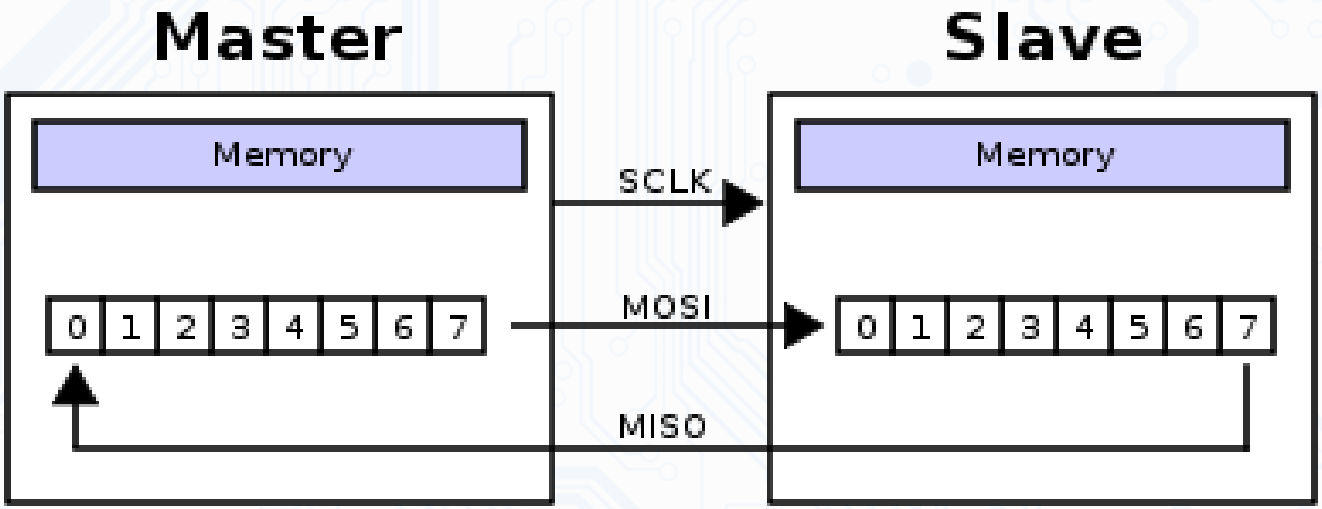
SPI wiring


SPI
Master
SCLK
MOSI
MISO
SS1
SS2
SS3
SCLK
MOSI
MISO
SS
SPI
Slave
SCLK
MOSI
MISO
SS
SPI
Slave
SCLK
MOSI
MISO
SS
SPI
Slave

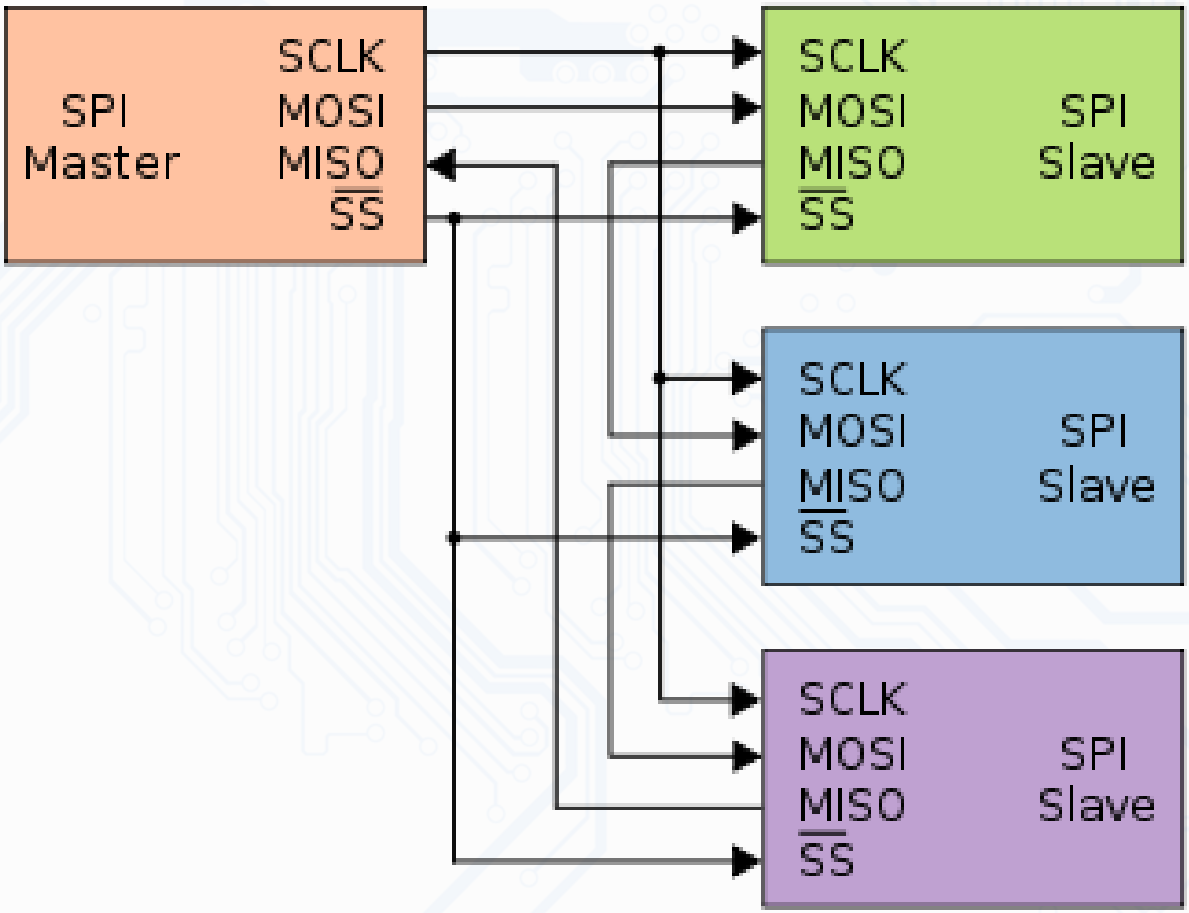
Time Diagram



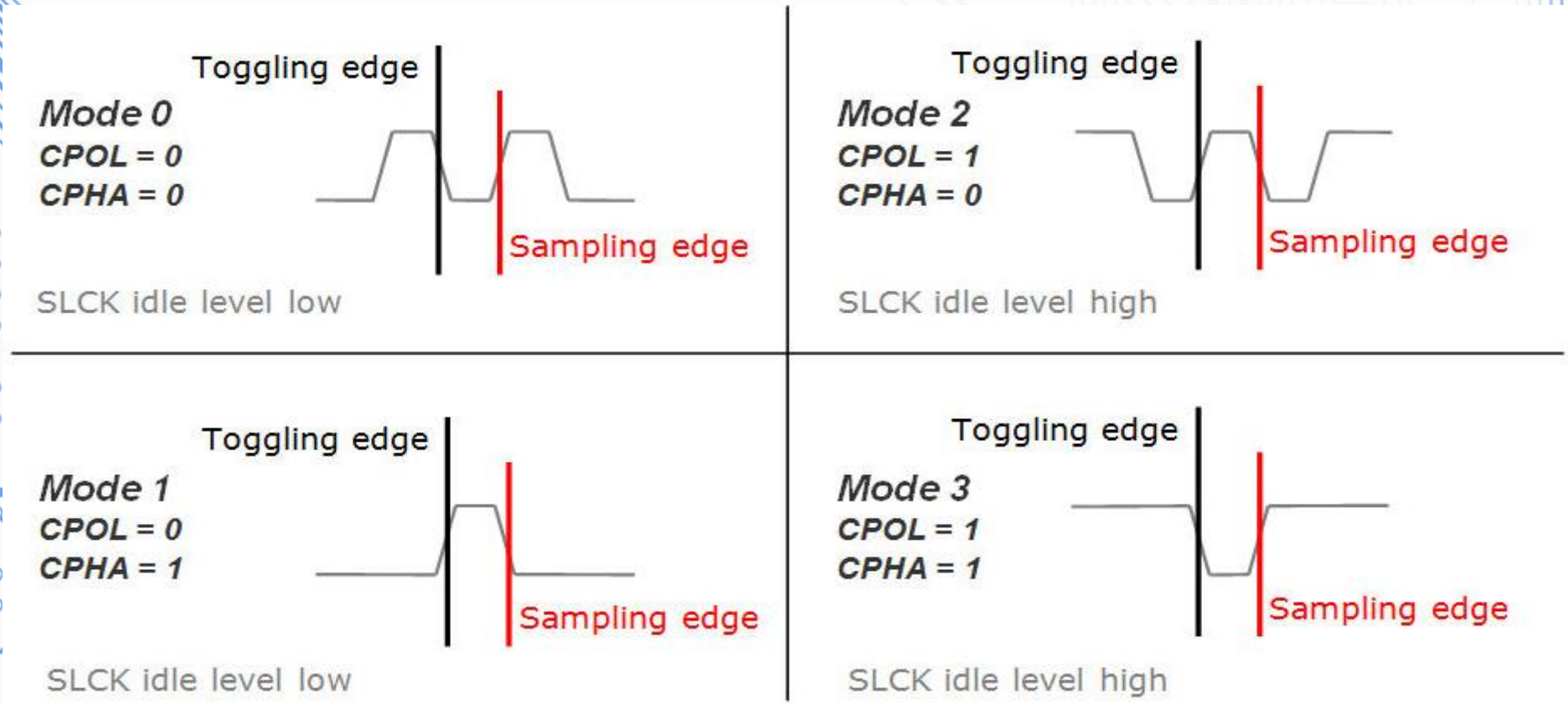
Circular Buffer



Daisy Chain Configuration



SPI Modes



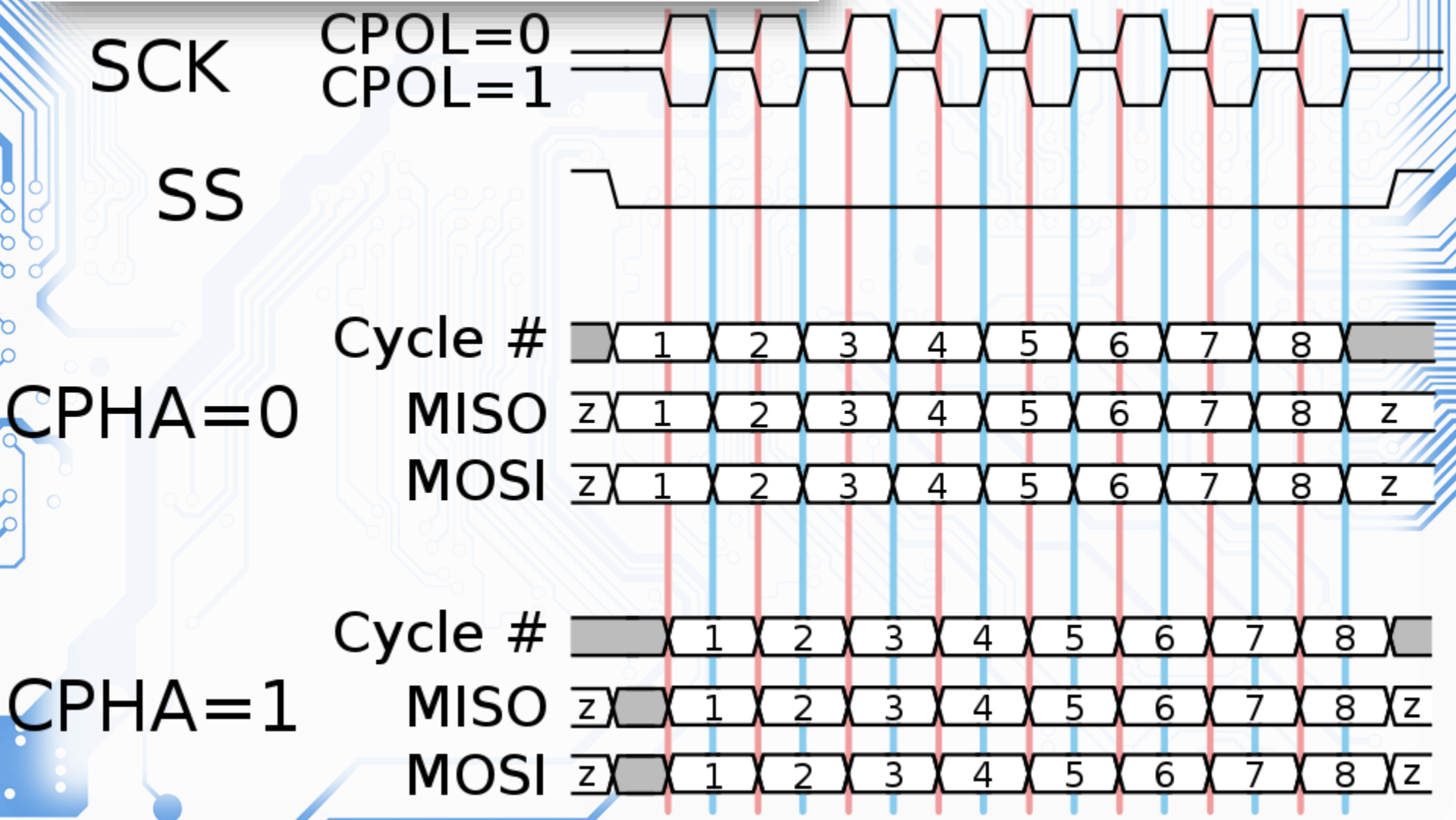
Where:

CPOL: clock polarity

CPHA : clock phase

SPI Modes

PHASE	CLKPOL	SCK Transmit Edge	SCK Receive Edge	SCK Idle State
0	0	Falling	Rising	Low
0	1	Rising	Falling	High
1	0	Rising	Falling	Low
1	1	Falling	Rising	High



End