National Telecommunication Institute

(NTI)

Electronics Department

PCB Design Using OrCad Software

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1-1. Starting a New Schematic

1-1-1. Before You Begin

It is helpful to be very organized when you are designing. OrCAD will create many files and if you keep all of them in the same directory, it can quickly become very confusing. I like to make a directory hierarchy and put associated files into subdirectories. Before beginning, navigate to the directory in which you will keep your project and create the following subdirectories:

- sch - for your schematics.
- lib - for symbol and footprint libraries.
- board - for your board files.
- comps - for component datasheets.
- assy - for assembly related documents.

For larger designs, more subdirectories would be desirable, but these will be sufficient for this project.

1-1-2. Starting a New Schematic Entry

To create a new project, first start OrCAD Capture and click File_>New_>Project. You will see the following dialog box. Browse to the schematic directory that you created and name the project.

You now have an empty project workspace. You should see an empty schematic page and a project window like the following.

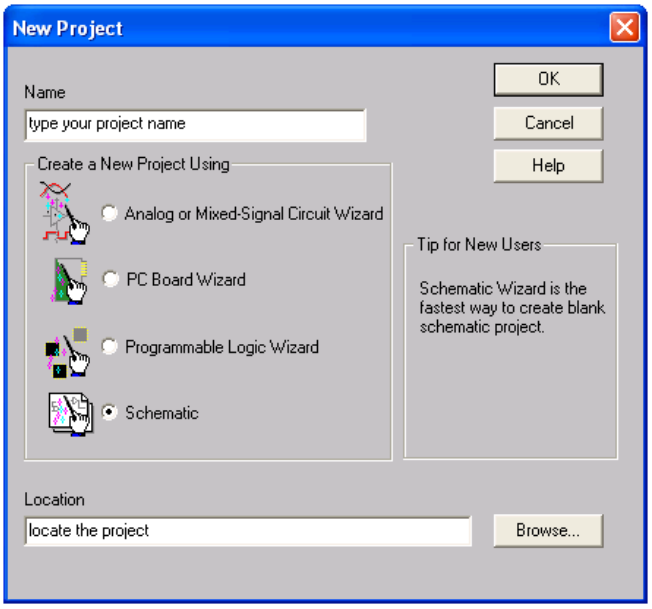


Figure 1: New project dialog

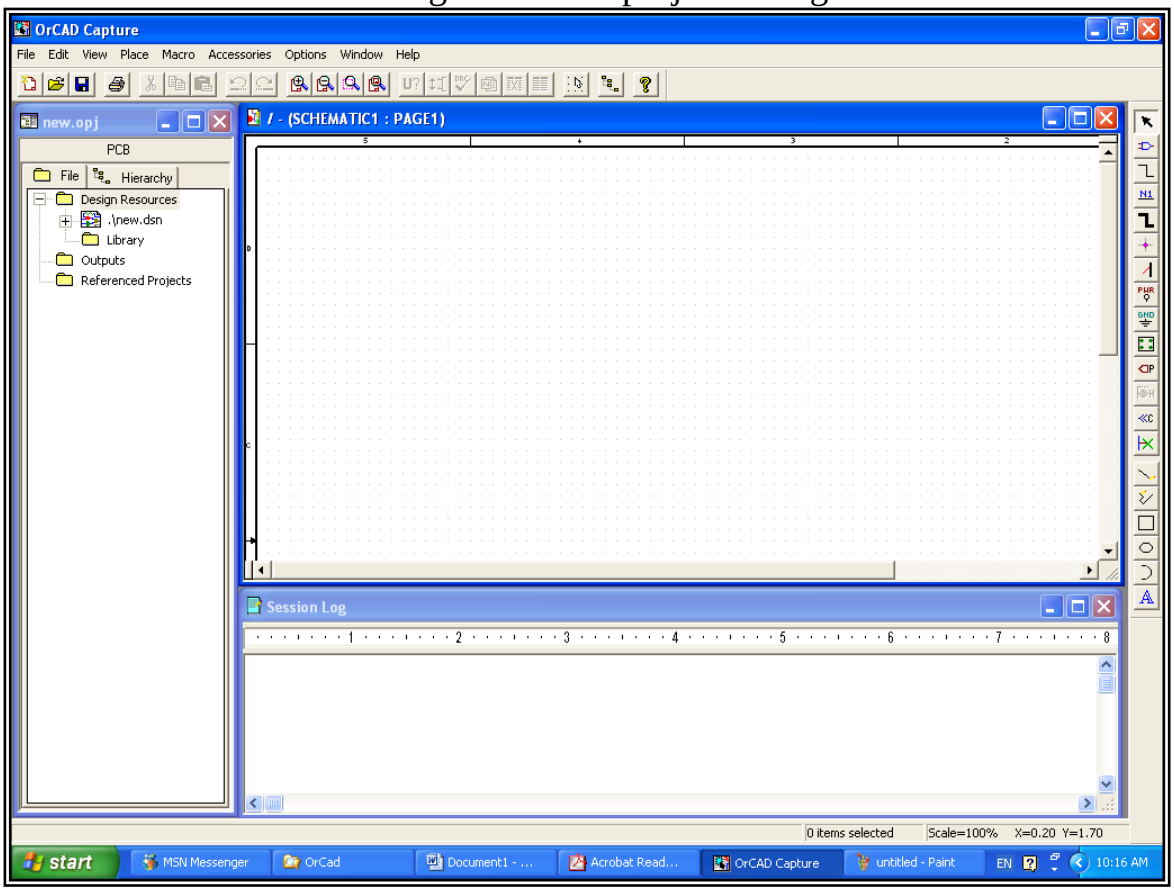


Figure 2: New project workspace

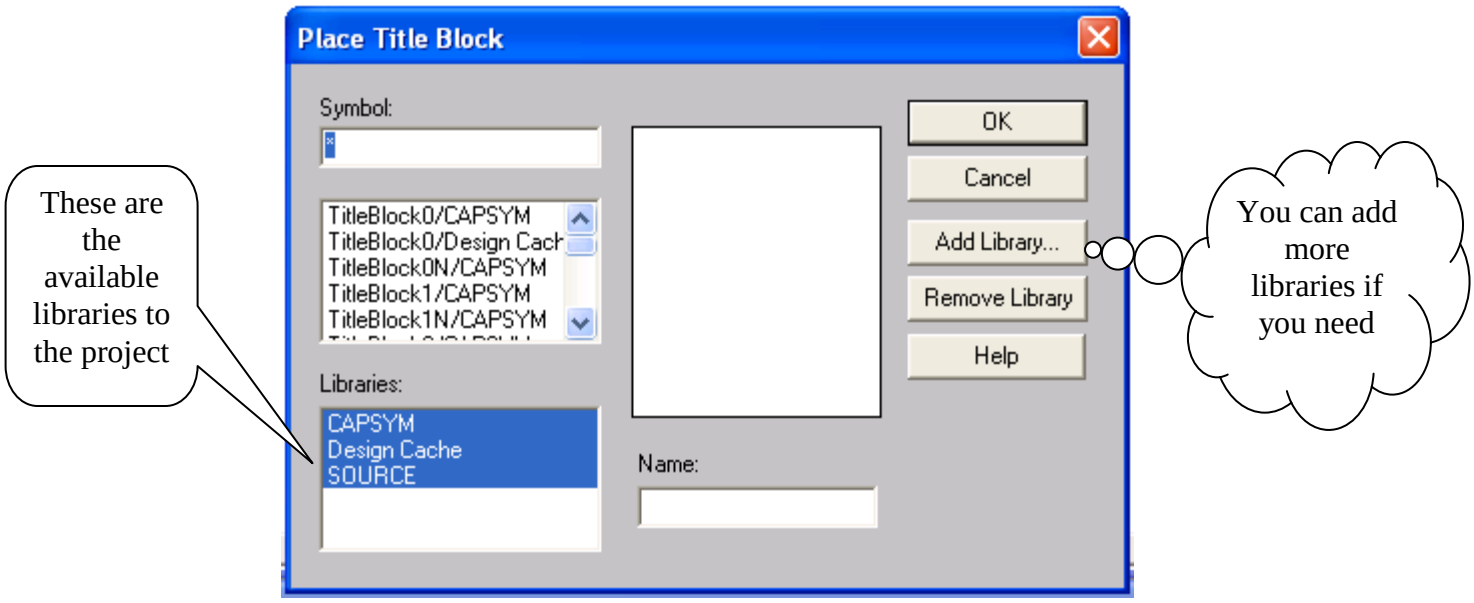
1-1-3. Schematic Entry in OrCAD

1-1-3-1. Setting Up the Environment

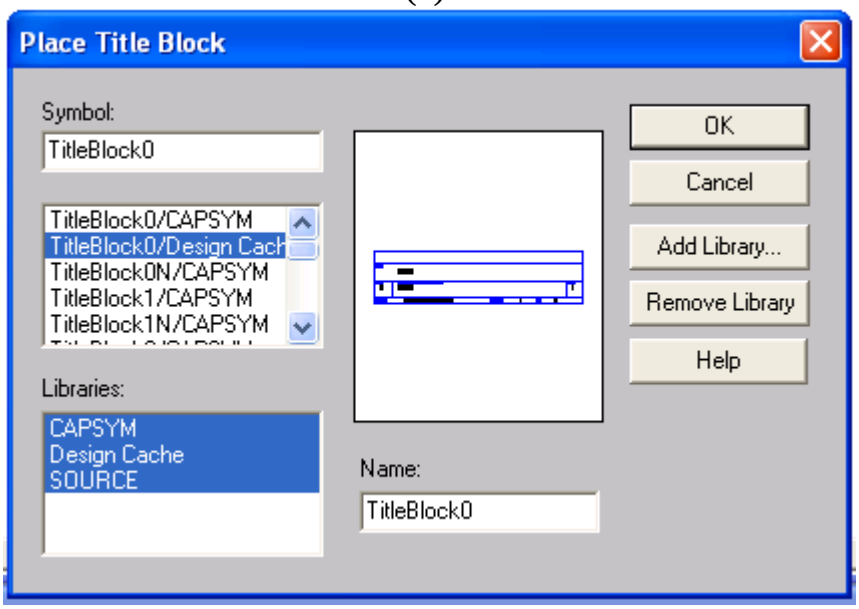
Now that you have your parts library set up, you are ready to begin entering schematics. You can see from the project window that you already have one page of schematics called PAGE1 in a folder called SCHEMATIC1. If you can't see this, click on the `+' next to the dsn file to expand the view. Even though our circuit is small enough to fit on one page, we will use two pages to demonstrate a schematic with multiple pages. First add a new schematic page by right-clicking the schematic ***root*** folder and selecting New Page. You will be prompted to provide a name for this page. Call it power and Connectors. Now rename the original page by right-clicking and selecting Rename. Call this Xilinx PLD. It is always nice to give your schematic pages useful names. While you are at it, rename the schematic folder in the same manner, calling it FPGA test.

Open power and Connectors page of your schematics by double-clicking it in the project window. This will bring up a blank page. Before we place parts, let's do a couple of things.

First, I like to make the page size a bit bigger than the default. You can fit a lot more onto the page and it will still look nice when printed. To do this select Options_>Schematic Page Properties. Click the Custom radio button and use the following values (width=15.2, height=11.5). Second, there is a title block in the lower right corner. We are going to replace this with our own, so highlight the title block and delete it. We add a new title block by selecting Place_>Title Block. . . You will see the following dialog box.



(a)



(b)

Figure 3 block title dialogue

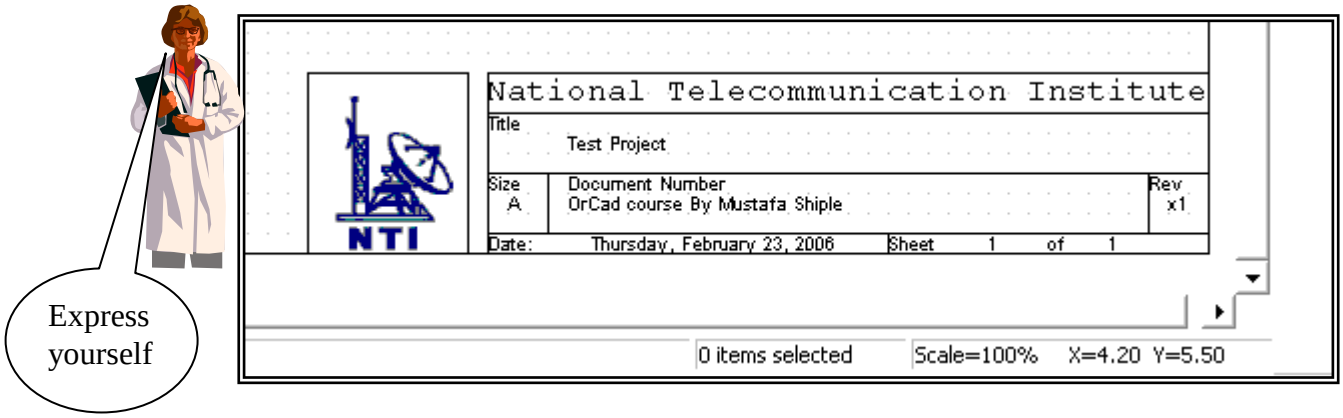


Figure 4 final presentation of Block title

The title block is in your library, so we need to add that to the list of libraries. Click the Add Library button to browse to and select the library you created for the tutorial. Once you have added the library, you will be able to choose the "TitleBlock0" to add it to your design. Place the title block in the lower right corner of your schematic page. The title block has fields to put information for each page of schematics. Double-click the text to edit each field and change the information on each page so that it looks something like this.

1-1-3-2. Placing Parts and Making Connections

You are now ready to start placing the electrical components for your design. Open the first page of your schematics and click the Place Part icon on the toolbar on the right side of the screen. You will then get a dialog for choosing which part you want to place on your schematics.

Select the part CONN JACK PWR and click OK. Place the part on the left side of your schematic page. Now place the remaining parts on both pages using the attached completed schematics as a guide

A small hint for moving around in OrCAD: use `I' and `O' to zoom in and out, respectively.

Figure 3: Place Part Icon

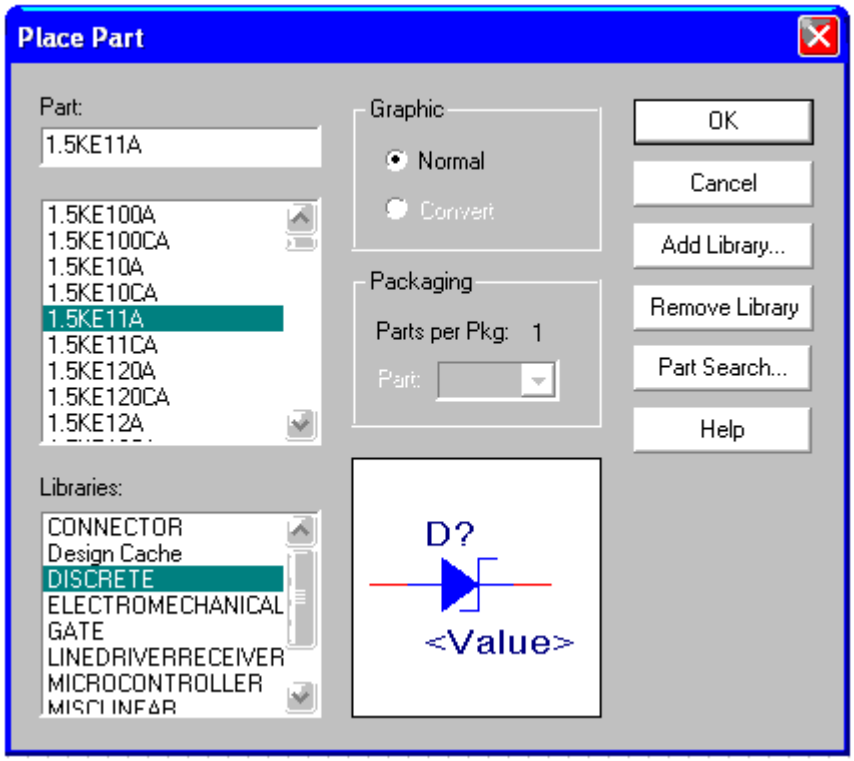


Figure 5: Place Part Dialog

`C' will center the design at your cursor. `R' will rotate a part. You can do these actions while in the middle of another action (e.g. while placing a part). You will also notice that each part has a value associated with it. You can change this by double-clicking the current value. In this manner you can give all your capacitors, resistors, etc. the appropriate values. When you are done, the first page of your schematics should look something like attached appendix.

Now we need to draw nets to make electrical connections between components. To do this, click the Place Wire icon and connect the components as shown in the attached schematics. Use the Place Bus and Place Bus Entry icons to place busses and bus connections.

Now you need to add power and ground connections to some of the parts. OrCAD has several built-in symbols for power and ground. I like to use a symbol that explicitly names the nets, as shown in the picture below. I do this because many designs will have multiple power and ground nets. Explicitly naming them helps prevent shorts and other errors. It also makes your schematics easier to read. Add power and ground to your schematics now.

The procedures you done are:

1- Create new project.
2- Customize schematic view.
3- Document your project.
4- Place the component you need.
5- Wire the interconnection.

1-1-3-3. Connecting Pages and Naming Nets

Since some of these connections go to the PLD, we need to a way to connect the two schematic pages together. We can do this by using off-page connectors (flat design). To place these click the Place Off-Page Connector icon. Then select the connector called OFFPAGELEFT-L or OFFPAGELEFT-R, it doesn't really matter which one, they are functionally the same. You can place this on your schematic just like a part and then connect to it with a net. Off-page connectors are linked by a common name. For example, two off-page connectors on separate pages with the name CLK will be considered by OrCAD to be one net. To name a connector, just double click it to get a naming dialog box. Name your connectors now using the attached completed schematics as a guide.

Note: For reasons that will become clear later, I like to place my off-page connectors as close to the edge of the page (right or left) as possible. This makes clear which nets go off page and which don't. It will also help you find mistakes on naming nets across pages.

Normal nets can also be named. This is extremely useful and can help tremendously in the layout process. I encourage you to use the Place Net Alias icon to name any important nets such as clocks, address and data bus lines, and other specific signals you are interested in. To name a net, first highlight the net you want to name and then click the icon, you will be given a dialog box to enter the name of the net. You can position the text anywhere you like. If you have already attached an off-page connector to a net, then that net already has the same name as the connector. You don't need to give the net an alias unless it will make your schematics more readable.

If you have any pins on parts that are left unconnected, use the Place No Connect icon to mark it in your schematics.

Now complete your schematics as shown in the attached reference.

(a) (b) (c)

Figure 6: (a) Place Wire Icon (b) Place Bus Icon (c) Place Bus Entry Icon

Figure 7: Place Off-Page Connector, Net Alias Icon and No Connect Icon

1-1-4. Creating a Schematic Parts in OrCAD Library

OrCAD allows you to create a library of part symbols for use in schematic entry. These libraries are kept in separate files that are included in the project workspace. This allows you to reuse libraries in other designs. In this experiment, A new version of nand and XC9538 will be created.

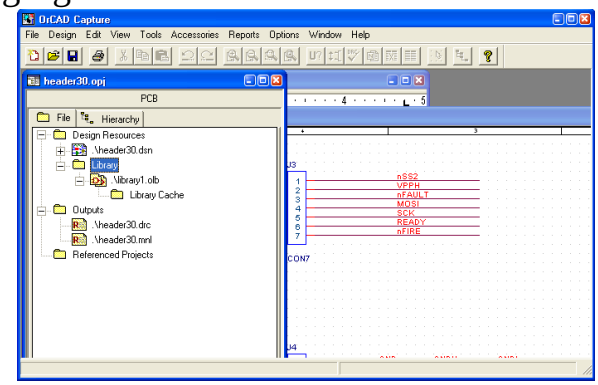
Experiment flow:

- The part definition.
- The part outline drawing
- Pin placing.

Experiment procedure

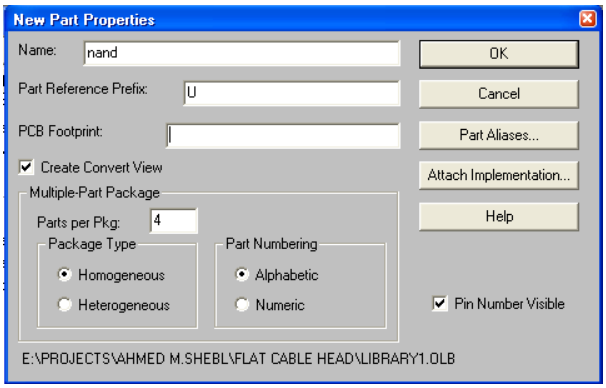
Define a new part (NAND)

1. .Add a new library to our design. To do this, click File_>New_>Library. Your project window will now look like the following figure.

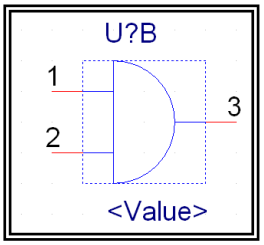


Note: When you place a part in a design, OrCAD creates a cached copy of the part symbol in the design file. This makes schematic projects portable but can also introduce some problems later in the design cycle.

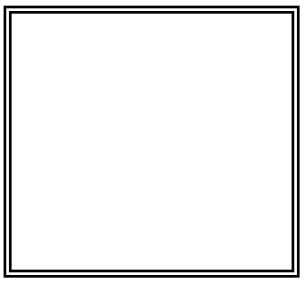
2. Right-click the library file and select Save As... Name the file MyLib and place it in the lib directory that you created earlier. You are now ready to add parts to your library.
3. Right-click the library file and select New Part. This will bring up a dialog box for New Part Properties.



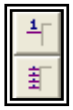
4. Type the part name, part reference and select the other options as shown. Note: Part Reference Prefixes (also known as Reference Designators) help categorize parts in your schematics and PCB layouts. There is a pseudo-standard reference for most types of parts. For example, C is used for capacitors, R for resistors, L for inductors, U for ICs, and X for crystals.
5. Convert view means a DeMorgan equivalent view. A part with this option specified will have two views (a normal and a convert) you can switch between once the part is placed.
   Homogenous means the package with multiple parts are graphically identical.
6. Now you have to draw the normal view and convert view. For normal view select View→Normal.
7. Draw the Nand symbol as shown do not forget the circle at the output (the next figure for ……..gate type) using Place menu.



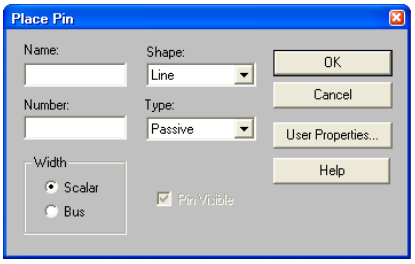
8. Tune the diameter of the circle in delicate manner by setting the grids from options→preferences (Grid display) uncheck pointer snap to grid.
9. After finishing reactivate pointer snapping. All graphics that make up the part must fit within the boundaries of the part body border.
10. DeMorgan equation is $\overline{A.B} = \overline{A} \oplus \overline{B}$
11. Draw the convert view according to DeMorgan equation in the next hallow rectangle.
12. From View menu select convert.
13. Draw the convert view using your graphical skills.



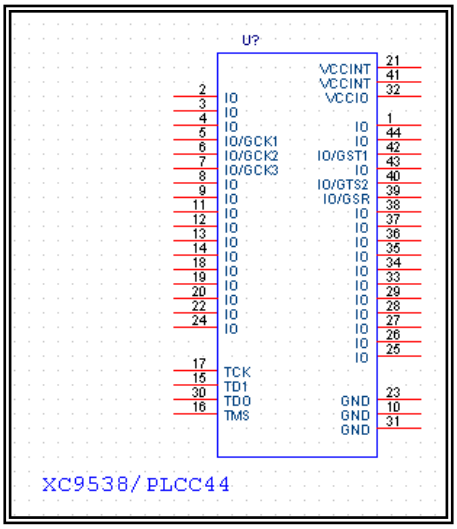
Placing Part pins:



14. Add pins to the part using the pin tool or the pin array tool.
15. The default pin Shape (Line) and Type (Passive) are OK for most pin types. For clocks and active low signals you may want to use some of the other shapes. Use the type Power for power pins. When you do this, make sure that the Pin Visible check box is checked. Place power pins near the top of the part and ground pins near the bottom.



16. State the three states of (3 state types) …… , …….., and ……
17. From View menu Select package then alternate among the parts to place power pins for each part.
18. Make up the design.
19. When you are done creating the part, you must save it. From the File menu, choose Save from file menu then Select close.
20. Update Cache commands to change the part in schematics (Design menu).
21. Now start to Create new part called (XC9538/LCC).



1-1-4-1. Creating Schematic Symbols in OrCAD Capture

To add a new part to your library, right-click the library file and select New Part. This will bring up a dialog box for New Part Properties, which looks like this.

We will be making a symbol for the Xilinx XC9536 PLD. This part comes in a 44-pin PLCC package. Name the part XC9536-PLCC44. Leave the Part Reference Prefix as U . You can leave the default values for all the other settings. Click OK to bring up the workspace for part creation. It should look like the picture below. Tools for working with the part are located on the toolbar on the right-hand side of the screen.

.

To get started, drag the dashed line on the workspace to make it a little larger. You won't be able to fit too many pins on the part with its current size. When it is large enough, use the Place Rectangle tool to draw a solid outline in the same place as the dashed line.

Use the Place Pin tool to place pins on the part. You will see a dialog that looks like this. Refer to the part datasheet for the correct pin numbers for the PC44 package. You can either download the datasheet from the Xilinx web site or from here

The default pin Shape (Line) and Type (Passive) are OK for most pin types. For clocks and active low signals you may want to use some of the other shapes. You will also want to use the type Power for power pins. When you do this, make sure that the Pin Visible check box is checked. place power pins near the top of the part and ground pins near the bottom. As a last touch, double-click the text that reads <value> and change it to read XC9536-PLCC44. When you are all done, your part should look something like the following symbol.

Save your part and close the window. You may get a warning about duplicate pin names, but that is OK to ignore. Your part will now be visible in your library.

Some parts are already in existing OrCAD libraries. It is usually OK to copy these parts for use in your own design. For example, let's say we want to use a simple resistor in our design. First, we need to open the library that contains the resistor. To do this, select File_>Open_>Library. OrCAD keeps all of its libraries in the path:

C:\Program Files\OrCAD\Capture\Library

Select the library called Discrete. This will open up a new window showing the contents of the library. Find the part called R and highlight it. This is our resistor. Select Edit_ >Copy from the menu and then highlight

your own library. Select Edit_>Paste from the menu and this will paste the part into your library.

When you do this, some extra parts will show up in your library. These are part aliases (the same part but with a different name). You can tell the aliases by the `-` that is inside the little gate next to the part name. You don't need the aliases they will just cause confusion. Delete them from your library.

Note: There are a few things to note about copying parts from existing libraries. First, always be sure to check the part you are copying against a datasheet for correct pinout, number of pins, etc. Second, some of the standard parts will have power pins that are invisible. Personally, I feel that this is a very bad design practice that can lead to errors in your design. If you copy a part that has invisible power pins, please be sure to make them visible. Trust me, this can save you a lot of pain and trouble later. Finally, beware of so-called _heterogeneous_ parts.

These parts split across multiple symbols. For example, you might see a part with general pins on one symbol and power pins on another. In general, heterogeneous parts should be avoided because they can cause problems. However, they may be acceptable for very large parts such as processors.

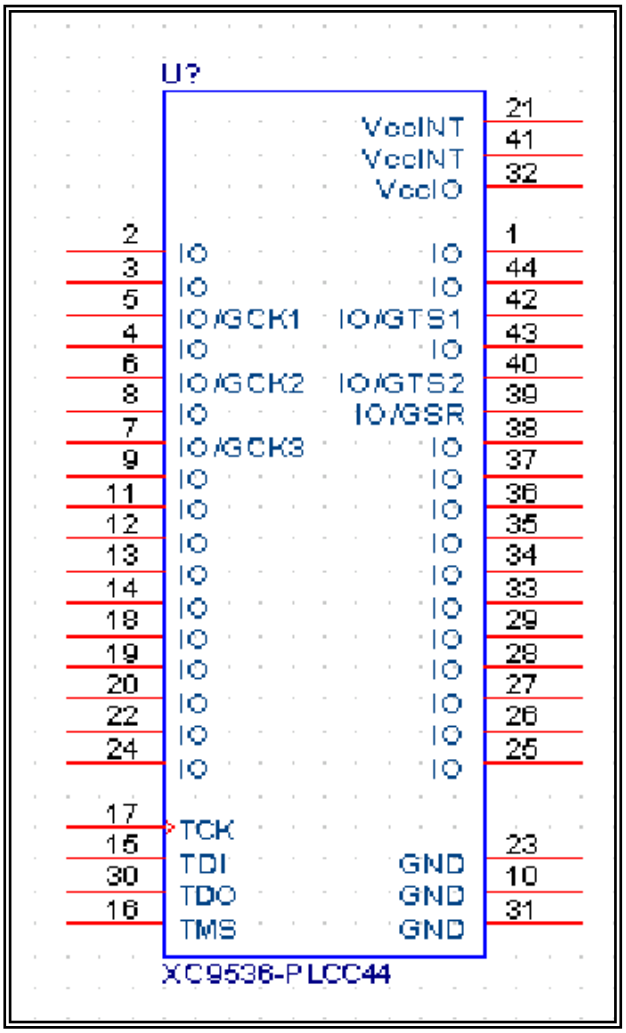


Figure 5: The finished PLD schematic symbol

1-1-5. Case Study

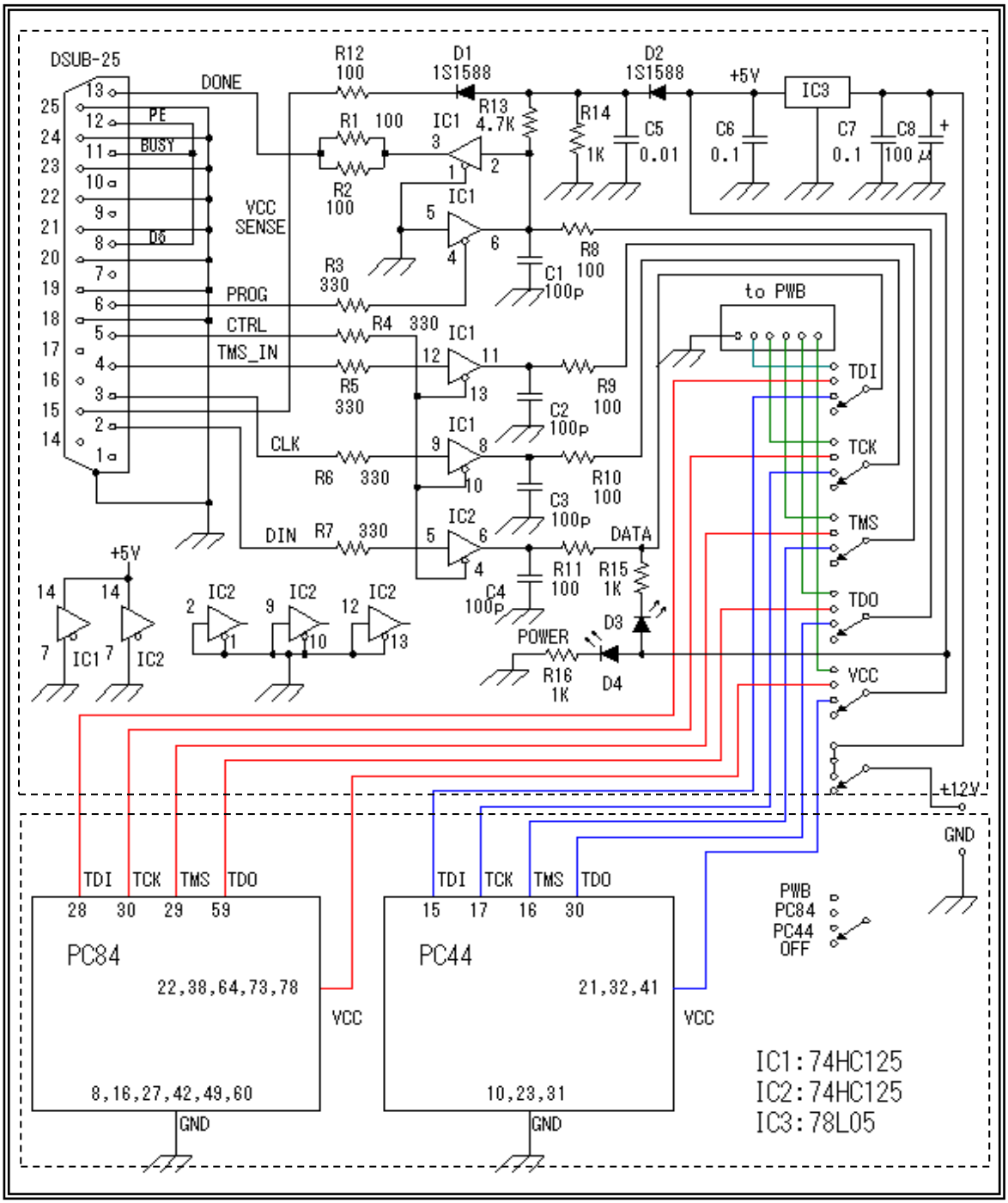


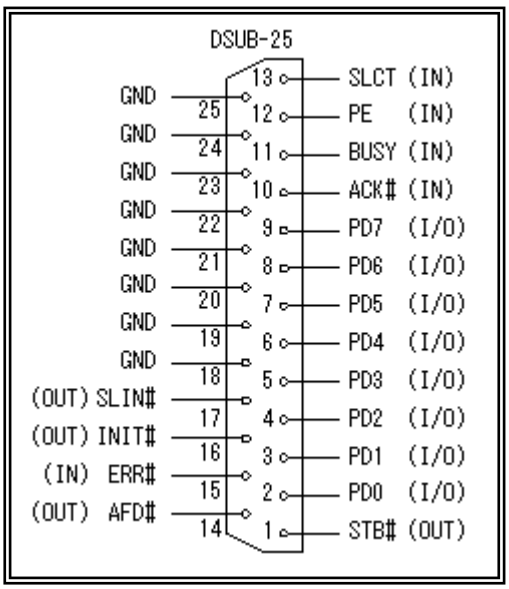
Figure 10: Circuit drawing of CPLD Programmer

For further information review

http://www.interq.or.jp/japan/se-inoue/e_cpld.htm

Parallel port

The CPLD programmer is connected with the parallel port of the personal computer. A printer is generally connected with the parallel port. The figure on the left shows the signal of each pin of the parallel port. A pin numbering is written by the small character at the connector. Because the assignment position with number becomes opposite on the side of the male connector and the side of the female connector, make not make a mistake. The 1st pin is connected with the 1st pin of the opposing connector.



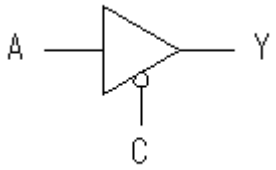
Pin #	Usual name	Name this time	Useage
2	PD0(I/O)	DIN(OUT)	Data signal output(TDI)
3	PD1(I/O)	CLK(OUT)	Clock signal output(TCK)
4	PD2(I/O)	TMS_IN(OUT)	Mode selection output(TMS)
5	PD3(I/O)	CTRL(OUT)	Output control signal
6	PD4(I/O)	PROG(OUT)	Input control signal
8	PD6(I/O)	D6(OUT)	Signal for condition detection?
11	BUSY(IN)	BUSY(IN)	Busy detection
12	PE(IN)	PE(IN)	Parity error detection
13	SLCT(IN)	DONE(IN)	Data signal input(TDO)
15	ERR#(IN)	VCC SENSE(IN)	Dvice status detection
18-25	GND	GND	Grounding

At the equipment this time, each pin is used as above.

In the table above, the IN and OUT are the direction of the signal which was seen from the side of the personal computer. It becomes contrary to the seeing from the side of the equipment.

The 8, 11 and 12th pins are connected at the connector. These three pins seem to be the one to confirm whether or not a programmer is connected.

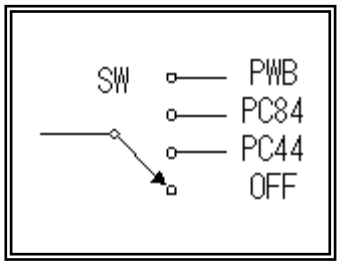
Bus buffer circuit



C	A	Y
H	X	Z
L	L	L
L	H	H

A bus buffer is put in the signal conductor of JTAG (TMS, TCK, TDI and TDO). 3 State buffer is used for buffer circuit. By this, the writing circuit to the CPLD device doesn't influence the parallel port of the personal computer. The buffer circuit works only when transferring data with the CPLD device.

When not transferring data, the output of the buffer becomes high impedance and becomes the condition which was separated from the circuit. When the transfer of the data is done, the buffer becomes low impedance to the CPLD device and makes the writing of data possible.



When the C terminal is H level, output terminal (Y) becomes high impedance. In this condition, it becomes the same when a bus buffer isn't connected. When the C terminal becomes an L level, the condition of input terminal (A) comes out to output terminal (Y). Because there is a high impedance condition in addition to H level and L level, this buffer is called a 3 State buffer. In the table, Z shows a high impedance condition.

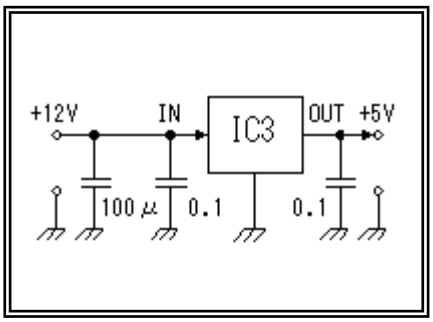
Device switching circuit

A device is switched by the rotary switch. Either one device can be controlled. Because it uses only any one generally, it is to be OK even if it doesn't switch. In the case, it is necessary to be careful when using. In case of the PWB mode, the power supply to the CPLD device uses the outside power. It is possible to use the power of this equipment only in about 100 mA.

LED display

The green LED displays the situation of power (Vcc) and the TDI-signal makes a red LED light up at the time of the L level.
Because the red LED is during the blink while forwarding data, don't dissolve to switch off the power, to pull out a cable and to remove a device.
To make an influence over the TDI-signal little, the value of the resistor to be putting in the LED in series is big comparatively.

Power circuit

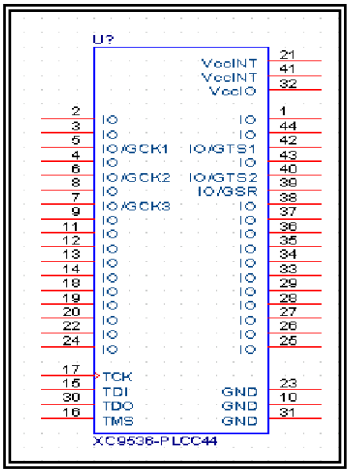


This power circuit makes the stable voltage (+5V) which the bus buffer and the CPLD device needs. 3 terminal regulator is used to get +5V output from +12V power in.

1-2. Library organization

Follow these conventions when organizing your part libraries:

- Organize libraries by component type.
- Group identical graphical representations of parts together using the part aliasing feature in Capture.
- If the graphical representation of a part is not unique but the package style is different, create one graphical representation and re-use it by using the part alias feature in Capture.
- Use different graphical representations for parts powered by different power supplies (for example, one works on a standard power supply [invisible power pins] and the other works on a non-standard power supply).
- Save a part in one library file (.OLB) only. The exception is if the part name is the same, but the part has two different graphical representations drawn to two different standards (for example, a component drawn to IEEE standards and to OrCAD standards). In this case, the parts can reside in two different libraries under the same name.
- Do not include IEEE libraries in searches for pre-existing symbol names. These libraries contain parts with graphical representations drawn to IEEE standards.
- Graphical representation creation



The following table lists the part reference prefix that should be used for each part type.

Part type	Part Reference Prefix	Part type	Part Reference Prefix
Capacitor	C	Transistor	Q
Diode, LED	D	Resistor	R
Isolation	ISO	Switch	SW
Connector	J	Transformer	T
Header	JP	IC	U
Inductor	L	Variable Resistor	VR
Relay	LS	Crystal	Y

Use the following conventions when placing pins on a part outline. Group the pins on each side of the part outline in the order they are listed below:

Left side	Right side
Data input	Data Output
Reference Voltage inputs	Data Bi-directional
Passive pins	
Clock inputs	Clock outputs
Control inputs	Control outputs
Visible power pins	

1-2-1. Power pins

Power pins in general

- Use the following conventions when placing power pins:
- Use the same standard name (that is, VDD as opposed to VDD1, VDD2) for parts with multiple instances of power that have the same supply inputs.
- Arrange the supplies so that all pins of the same power type are grouped together (for example, all VCC should be grouped) within each group, place the pins in ascending order of pin numbering.

- If you make non-standard power pins visible, you should preferably have non-fixed voltage names (VCC, VDD, etc.) and not fixed voltage names (-5V, -22V, etc.).

1-2-1-1. Invisible power pins

An invisible power pin is automatically connected globally to all other symbols in a design that have the same power pin name. For example, an invisible power pin on U1 called VCC will be connected (during the netlist operation) to all other power pins in the design called VCC. However, because of the qualifications for a pin to be considered an invisible power pin, you cannot connect a discrete wire to the pin.

note → Visible power pins are not connected globally.

The qualifications for a pin to be considered an invisible power pin include:

- The pin must be a supply input pin or a ground pin.
- The supply voltage must be a fixed voltage (that is, not variable depending on the design application).
- The supply voltage must be an industry standard value (for example, digital +5 Volts).
- The pin is typically connected directly to a power supply and not driven by the circuit.

Conventions

If you decide to make a power pin invisible, use one of the OrCAD standard power pin names in the following table:

Power type	Standard power pin name
+5V digital	VCC
Digital Ground	GND
+5V Analog	+VCC
-5V Analog	-VCC
+12V Analog	+12
-12V Analog	-12
+15V Analog	+15
-15V Analog	-15

Analog Ground	AGND
VEE	ECL
VSS	ECL (If -5.2 volts) GND (if connected to digital ground)

- Place invisible supply pins on the top border of the IC outline and ground pins on the bottom border.
- Always make invisible power pins zero length and invisible.
- When placing invisible power pins on the top and bottom of the part outline, make sure they can be made visible without overlapping pins that are located on the sides of the part.
- Place visible power pins on the left side of the bottom of the part outline.

1-3. Creating a flat design

In this section, we will create a simple flat half adder design with X and Y as inputs and SUM and CARRY as outputs as in next figure.
Create two pages input stage and output stage respectively.

1-3-1. Adding parts

- From the next figure place required parts

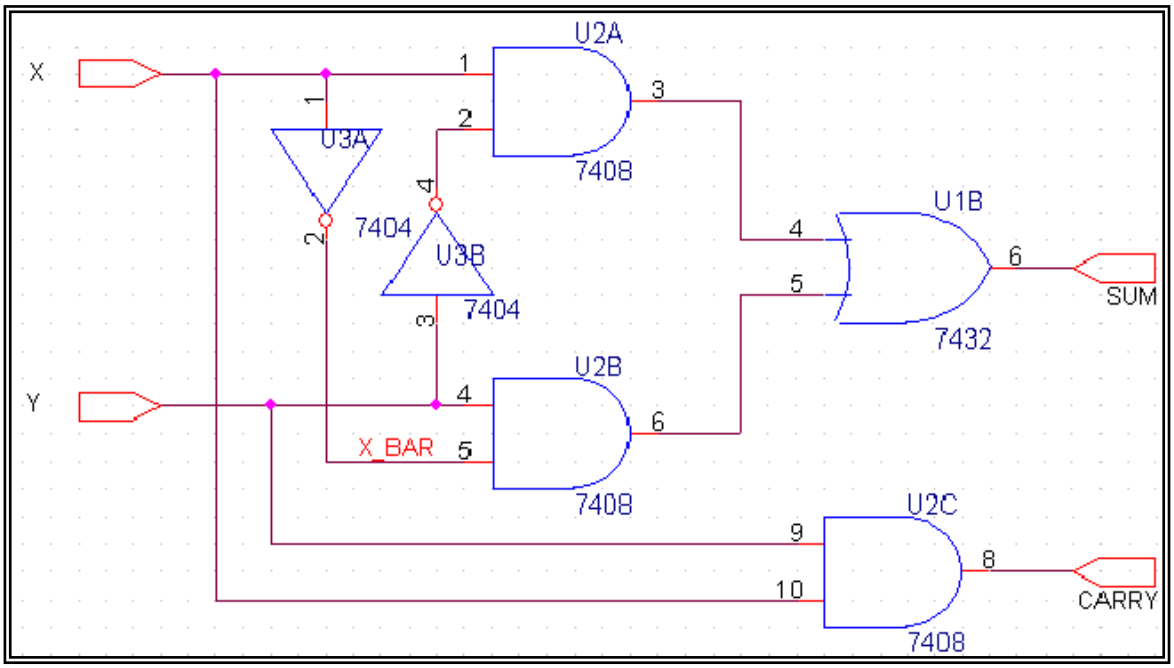


Figure Half adder design

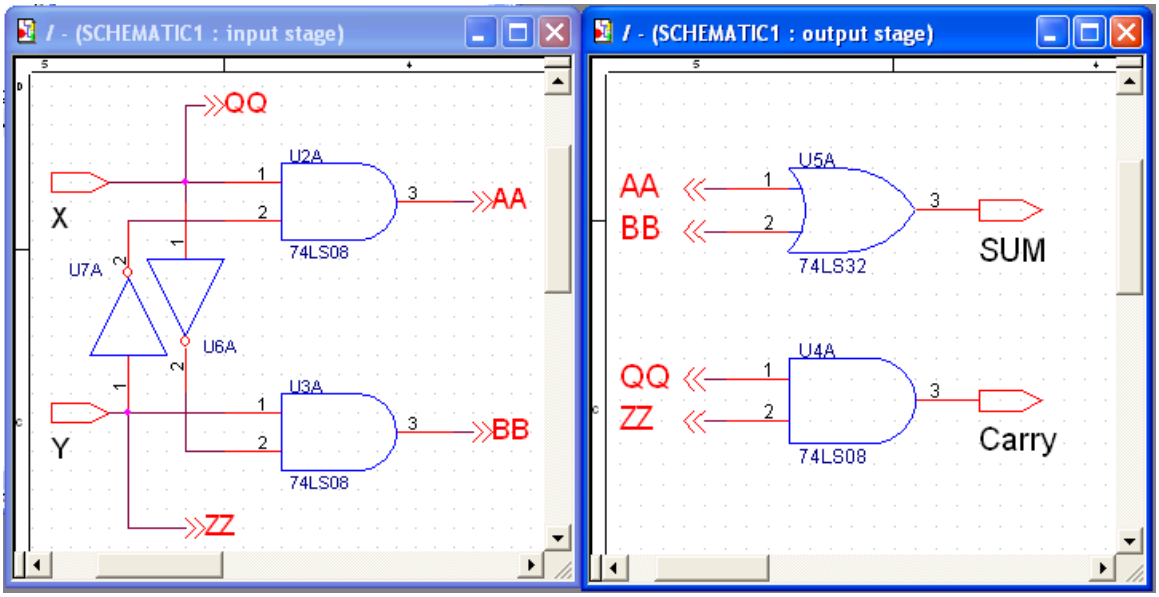


Figure Half adder design presentation through OrCad

- Connect the parts together (place wires) it should be like previous figure.

To add input and output ports to the design, complete the following sequence of steps:

- From the Place menu in Capture, select off-page connector. Note: Alternatively, you can select the Place off-page connector button from the Tool Palette.
- To rename the off-page connectors to indicate input signals AA, BB, QQ and ZZ, double-click the port name. In the Display Properties dialog box, change the value of the Name property to AA and click OK. Similarly, change the names of the other off-page connectors.
- From the Place menu in Capture, select Hierarchical Port. The Place Hierarchical Port dialog box appears. Note: Alternatively, you can select the Place port button from the Tool Palette.
- From the Libraries list box, select CAPSYM.
- First add input ports. From the Symbols list, select PORTRIGHT-R and click OK.
- Place two instances of the port as shown in the figure above. Right-click and select End Mode.
- To rename the ports to indicate input signals X and Y, double-click the port name. In the Display Properties dialog box, change the value of the Name property to X and click OK. Note: You can also use the Property Editor to edit the property values of a component. Similarly, change the name of the second port to Y. Note: The Place Part dialog box is not used for placing ports, because ports in CAPSYM.OLB are only symbols and not parts. Only parts are listed in the Place Part dialog box.
- Add two output ports as shown in the figure below. To do this, select PORTLEFT-L from the CAPSYM library.
- Rename the ports to SUM and CARRY, respectively.
- Save the design.

The half adder design is ready. The next step is to create a full adder design that will use the half adder design.

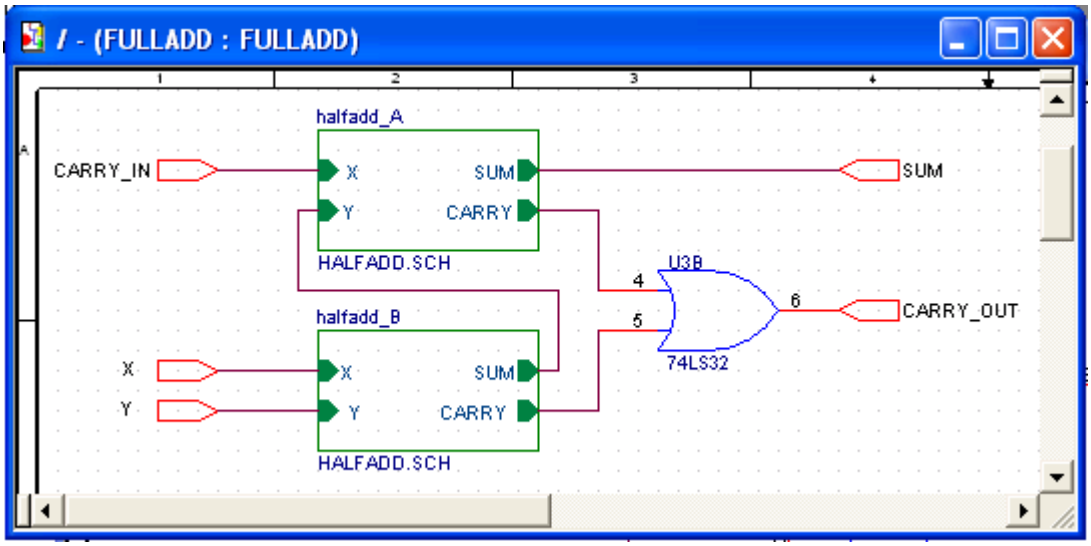
1-3-2. Creating a hierarchical design

In Capture, you can create hierarchical designs using one of the following methods:
_ Bottom-up method
_ Top-down method
In this section, we will create the full adder hierarchical design. The half adder design created in the Creating a flat design section will be used as the lowest level design.
Bottom-up method
When you create a hierarchical design using the bottom-up methodology, you need to follow these steps.

- _ Create the lowest-level design.
- _ Create higher-level designs that instantiate the lower-level designs in the form of hierarchical blocks.

In this section, we will create a full adder design using bottom-up methodology. The steps involved are:

- Creating a project in Capture.
- Creating the lowest-level design. In the full adder design example, the lowest-level design is the half adder design.



- Creating the higher-level design. Create a schematic for the full adder design that uses the half adder design created in the previous step.

Creating the full adder design

- In the Project Manager window, right-click on *.dsn and select New Schematic.
- In the New Schematic dialog box, specify the name of the new schematic folder as FULLADD and click OK.
- In the Project Manager window, the FULLADD folder appears below *.dsn.
- Save the design.

- To make the full adder circuit as the root design (high-level design), right-click on FULLADD and from the pop-up menu select Make Root. The FULLADD folder moves up and a forward slash appears in the folder.
- Right-click on FULLADD and select New Page.
- In the New Page in schematic: FULLADD dialog box, specify the page name as FULLADD and click OK. A new page, FULLADD, gets added below the schematic folder FULLADD.
- Double-click the FULLADD page to open it for editing.
- From the Place menu, choose Hierarchical Block.
- In the Place Hierarchical Block dialog box, specify the reference as HALFADD_A1.
- Specify the Implementation Type as Schematic View.
- Specify the Implementation name as HALFADD and click OK. The cursor changes to a crosshair.
- Draw a rectangle on the schematic page. A hierarchical block with input and output ports is drawn on the page.
- If required, resize the block. Also, reposition the input andoutput ports on the block. Note: To verify if the hierarchical block is correct, right-click on the block and select Descend Hierarchy. The half adder design you created earlier should appear.
- Place another instance of the hierarchical block on the schematic page. Select the hierarchical block.
- From the Edit menu, choose Copy.
- From the Edit menu, choose Paste.
- Place the instance of the block at the desired location.
- By default, the reference designator for the second hierarchical block is HALFADD_A2. Double-click on the reference designator, and change the reference value to HALFADD_B1.
- Using the Place Part dialog box, add an OR gate (74LS32) to the schematic.
- To connect the blocks, add wires to the circuit. From the Place menu, choose Wire. Draw wires from all four ports on each of the hierarchical blocks
- Save the design.

1-4. Preparing for OrCAD Layout

1-4-1. Annotation

Now that your schematics are complete, you are ready to prepare to export the design to Layout. From now on, you will be working in both Capture and Layout. The first step in preparing your design is to annotate it. Annotation really involves several steps. First, we will assign unique reference designators to all of the parts in our circuit. Remember reference designators? These are just labels that are used in Layout to uniquely identify different types of parts. If you look at the hierarchy view in the project window, you will see a jumble of reference designators. You might have several capacitors named C1 or a lot of parts that have the label, R?, C?, U?, etc.

To fix this, we will use a few of the annotation tools. In the file view of the project explorer, highlight the top-level design file (the one with the *.dsn extension) and then select Tools_>Annotate. You will see the Annotate dialog box.

In a new design, it is best to first reset all the part designators. To do this, click the radio button that says Reset Part References to "?" and then click OK. You will be asked if you want to save your design before proceeding. Every part in your design will now have a question mark in its reference designator instead of a number. Now, reopen the annotate dialog box and check the box that says Incremental Reference Update and click OK. This will go through your entire design and number each part starting with 1 for each part type. If you now look in the hierarchy view, you will see that you have a nicely ordered list of parts.

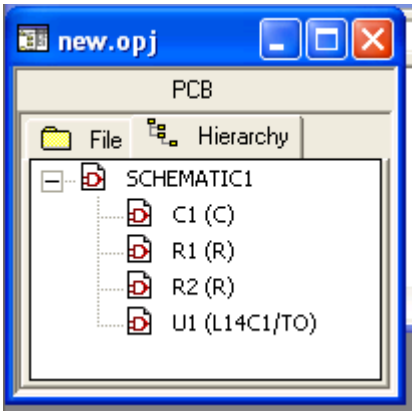


Figure11: Parts design reference

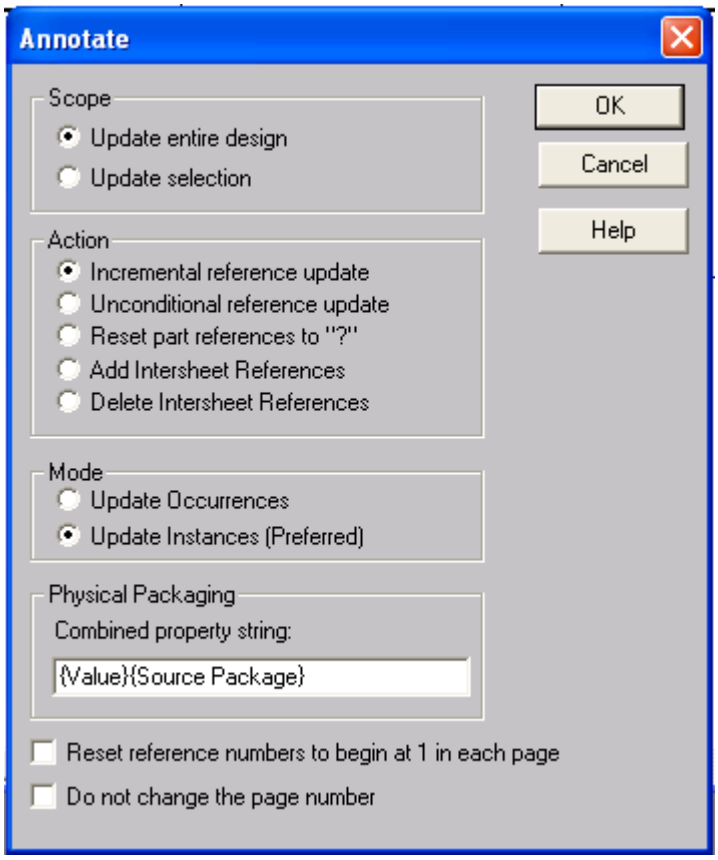


Figure 12: Annotate dialog

1-4-2. Inter-sheet References

The next thing we will do is add inter-sheet references to your schematics. Doing this will place page numbers near each off-page connector that indicate to which other pages that net is connected. This is invaluable during design and debug because it will help you track individual nets across a large design in many pages of schematics. Since we only have two pages of schematics in this design, we could probably get away without adding intersheet references; however, it is a useful tool and should always be used for good design practice. Another reason for using this tool is that it helps to find mistakes in naming nets. For example, say you have a net named CLKIN but on one page of schematics you mislabel this net CLKIM. After annotation, these two o_ page connectors will not have page numbers next to them, indicating that they are single-pin nets. This would be an immediate warning flag that something is seriously wrong with your schematics. To add intersheet references, bring up the annotate dialog box again. Select the radio button that is labeled Add Intersheet References. You will get a secondary dialog box, and you can leave the default values as they

are for now. Just click OK to continue. As far as schematics are concerned, your design is now fairly complete.

1-4-3. Design rule check

After you have completed your design, it is recommended that you run design rules check (DRC) to isolate any unwanted design errors that might be there in the design. To run DRC on the full adder design, complete the following steps:

1. In the Project Manager window, select the design file,
2. From the Tools menu, select Design Rule Checks.
   Note: Alternatively, you can select the Design Rule Checks button from the toolbar.
3. In the Design Rules Check dialog box, the Design Rules Check tab is selected by default. Specify your preferences. By default, the Check entire design option button is selected. To run DRC on the complete design, accept the default selection.
4. Select the Use Occurrences option button. Note: For complex hierarchical designs, the occurrence mode is the preferred mode. Therefore, ignore the warning that is displayed when you select the Use occurrences option button.
5. To run the DRC, select the Check design rule option button.
6. In the Report section, select appropriate check boxes to specify what all are required in the DRC report. For the current design example, select the Check unconnected nets and Report identical part references check boxes.
7. Select the View Output check box. When this check box is selected, the DRC report is opened automatically for viewing after the checks are complete.
8. Clicks OK. After the checks are done, the DRC report is displayed in the format shown below.

```
Checking Pins and Pin Connections
-------------------------------------------------
Checking Schematic:FULLADD
-------------------------------------------------
Checking Electrical Rules
Checking for Unconnected Nets
Checking for Invalid References
Checking for Duplicate References
Check Bus width mismatch
-------------------------------------------------
Checking Schematic:HALFADD_A1 HALFADD
-------------------------------------------------
   Checking Electrical Rules
```

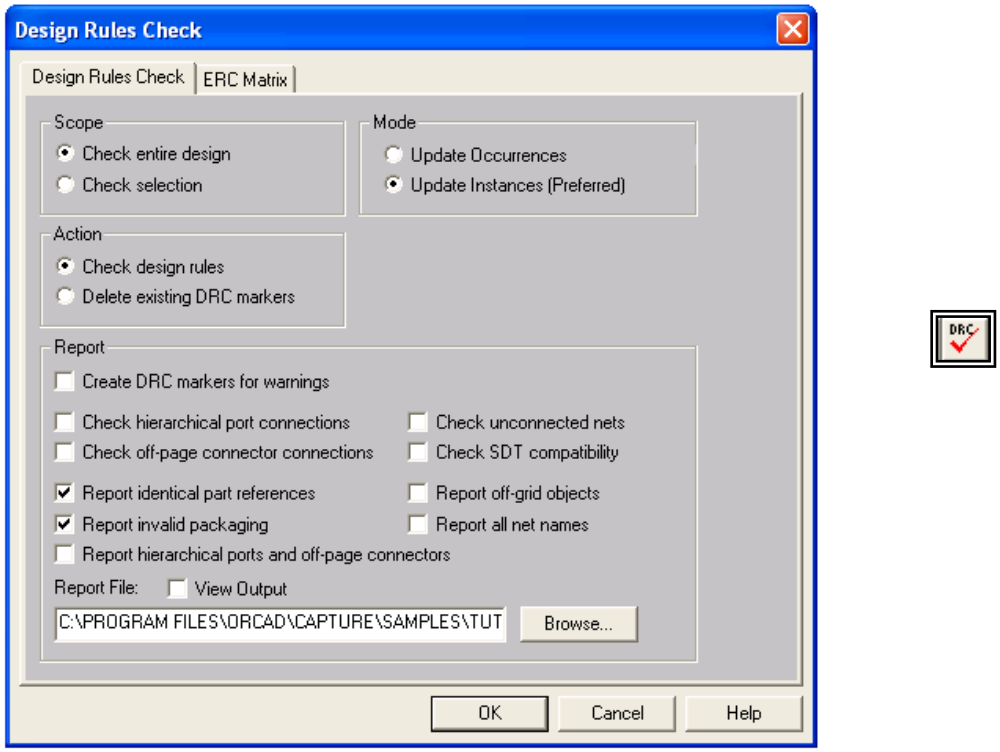


Figure 13: DRC dialog

1-4-4. Creating Layout netlist

After running the Design Rule Checks, you create the Layout netlist in Capture.

1. 1 In the Project Manager window, select the design file.
2. 2 From the Tools menu in Capture, choose Create Netlist.
3. 3 In the Create Netlist dialog box, select the Layout tab

4. 4 In the Netlist File text box, type FileName.MNL as the name for the layout netlist to be created.
5. 5 Click OK.

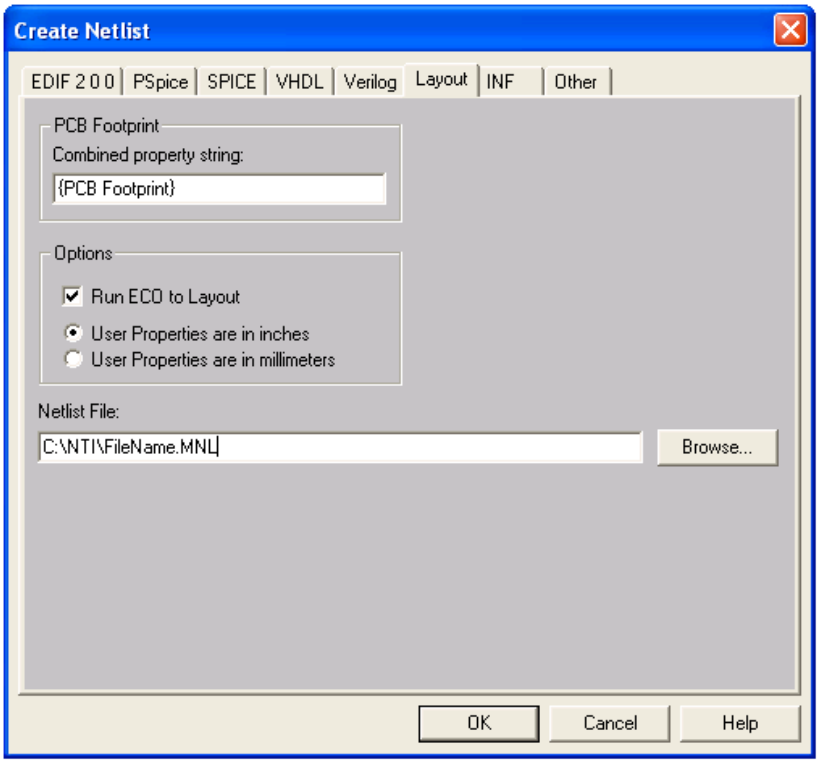


Figure 14: NetList dialog.

1-5. OrCAD Layout

1-5-1. Objective:

This part will introduce the basic layout design steps, such as , Creating a new board , Setting up board parameters, Placing components, Routing critical nets and Finishing the board.

1-5-2. Experiment flow:

1. Creating new board.
2. Setup board parameter.
3. Add mounting holes.
4. Creating new padstack.
5. Creating a new footprint.
6. Smartrout.

1-5-3. Procedure

Creating a board

1-Start a new project by clicking on File → New

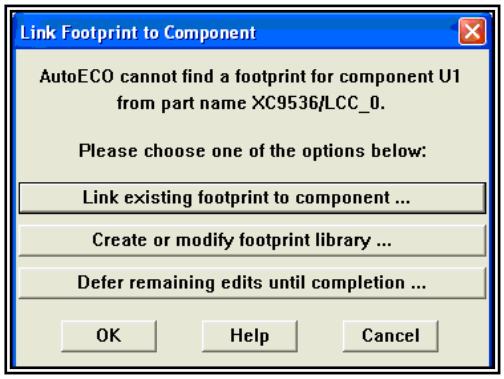
2-load template file which provides the framework within which you can create a board design

c:/program file/orcad/layout_plus/data/386lib.tch

3- Load the netlist file generated from schematic file. It is in the same directory as your Capture file (open as file name XC9536_1.mnl)

4- Save the Layout file as File name XC9536_1.max.

5- **Auto ECO** screen will appear. Note**:** **AutoECO** is **A**utomatic **E**ngineering **C**hange **O**rder process that uses the information in layout netlist to produce a new board file or update an existing board file



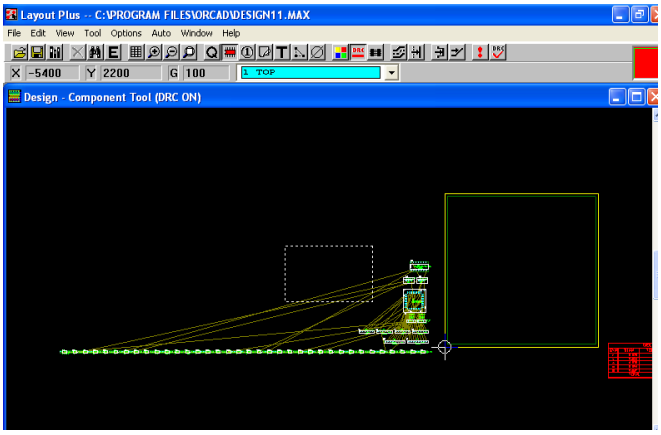
We can choose one option from three:

a) **"Link existing footprint to component";** at the beginning, you will define the description of footprint which describe the physical description of components. A footprint generally consists of three object types padstacks, obstacles (representing among other things, the physical outline of the component, silkscreen outline, assembly outline, and placement and insertion outlines), and text (for example, the component name or component value each time you see it (which will be about once per component you have in your schematic.

b) **"Create or modify footprint library";** you can create new footprints and add them to the libraries of your choice.
c) **"Defer remaining edits until completion";** Used for cancel link footprint to components

Setting up board parameters

In Layout, you should setup the board's parameters before you begin placing components. The parameters are listed below



1.Create a board outline

- Choose the obstacle toolbar button then double click. The edit obstacle dialog box displays.
- Modify the board outline setting and draw the board outline.

2.Set the units of measurement

- To specify the units of measurement for the design
- From the option menu choose system setting modify the setting in the dialog box then press ok.

3.Set the system grids

- From the Options menu, choose System Settings. The System Settings dialog box appears.
- Set these options, then press OK button.

4.Set routing layers

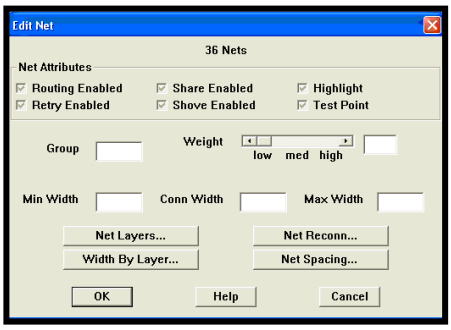
- Choose the spreadsheet toolbar button then choose Layers. The Layers spreadsheet appears.
- Review the type assignments for the routing layers and double-click in the Layer Name column of a layer you want to modify. The Edit Layer dialog box appears.
- In the Layer Type group box, select the desired option
- Choose the ok button.

5.Set global spacing

- From spreadsheet choose strategy then choose route spacing double click on layer name the edit spacing dialog appears then modify the spacing value as the same from the option menu choose global spacing.

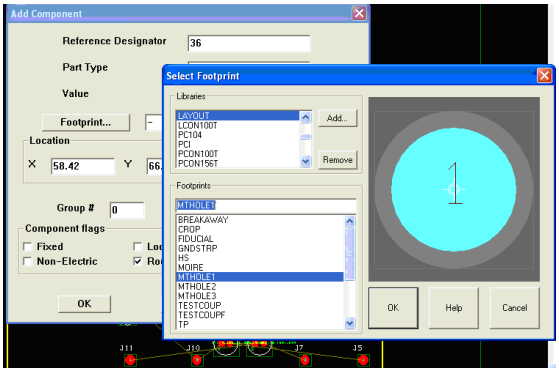
6.Set the widths of nets

- From spreadsheet choose nets, double click on layer name the edit net dialog appears then modify it.



Add mounting holes

1. Choose the component toolbar button.
2. From the pop-up menu, choose New. The Add Component dialog box appears.
3. Choose the Footprint button. The Select Footprint dialog box appears.
4. In the Libraries group box, select LAYOUT.LLB. Use the Add button.
5. In the Footprints group box, select a mounting hole1. Choose the OK button.

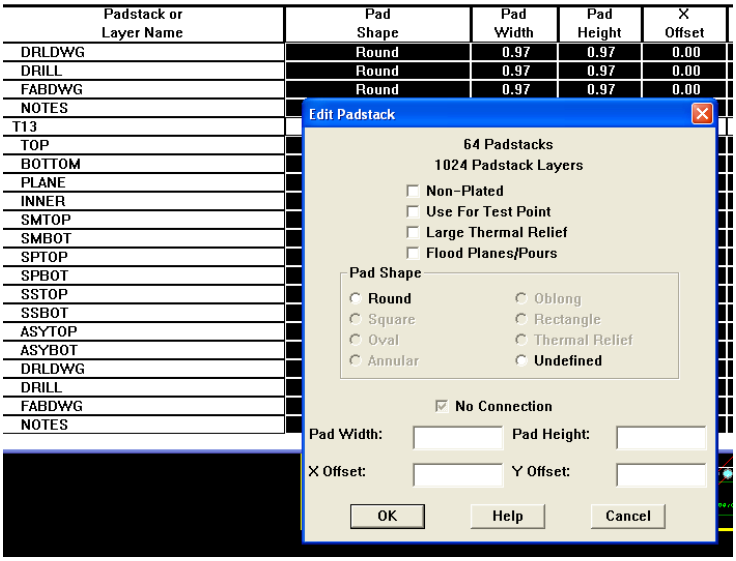


Creating new padstack

1. Select padstack from spreadsheet and press the insert key this creates a copy of padstack
2. Double click on layer name or padstack the edit padstack dialog appears then modify it.

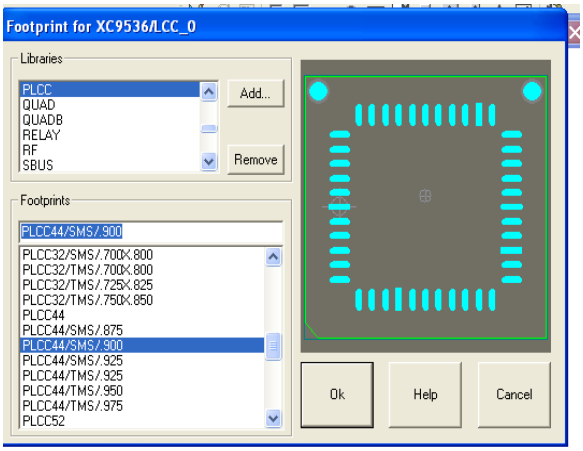
Editing padstacks

You can edit the default padstack, or padstacks that you have defined while setting up the board. Editing changes you make in the Edit Padstack dialog box are applied to all layers of the padstack. Editing changes you make in the Edit Padstack Layer dialog box are only applied to the selected layer.



Creating a new footprint

1. In the library manager, choose the Create New Footprint button.
2. Enter a name for the new footprint.
3. If the footprint is to be a metric footprint, select the Metric option.
4. Choose the OK button. The footprint origin, one pin and default text objects display in the footprint editor.

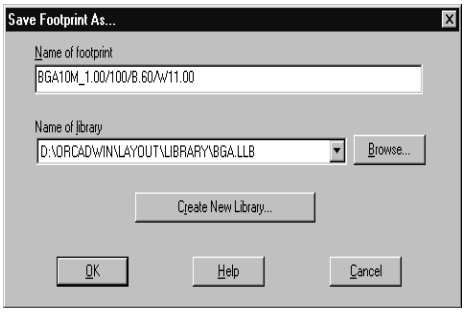


Note: To start the library manager Choose the library manager toolbar button. Or From the File menu, choose Library Manager.

To create a custom footprint library

1. Choose the library manager toolbar button. The library manager appears.
2. In the Footprints list, select a footprint to save to the new library. The footprint appears in the footprint editor.
3. Choose the Save As button. The Save Footprint As dialog box appears.
4. Choose the Create New Library button. The Create New Library dialog box appears.

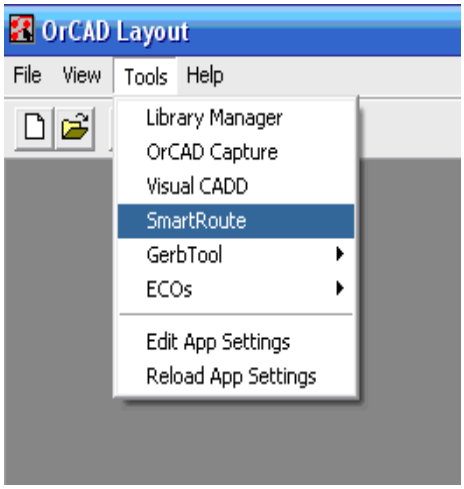
5. Enter the name for the new library (using a .LLB extension) in the File name text box, select a directory for the library, then choose the Save button



1-6. The SmartRouting

The component are placed on the board, It must be routed the electrical connections. The circuit Layout Plus provides autorouter called SmartRouter. Exclusive to Layout Plus, SmarteRoute has fast routing speeds, high completion rates, and high router quality.

To start SmartRoute



1. From the Tools menu in the Layout Plus session frame, choose martRoute. You see the SmartRoute session frame is displayed.
2. From the File menu, choose Open. The Open Design File dialog box will be opened Browse the .MAX design file then click open Note, You can save SmartRoute designs using the Save As command. You can also use the Backup command to automatically save designs.
3. How could you change the name of your circuit from XT9536 into CPLD?……
   ……

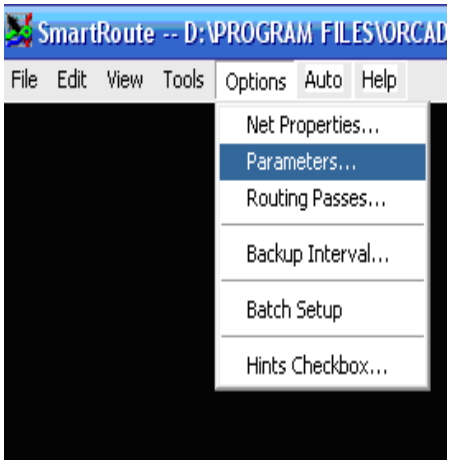
When routing the board there are two main parameters have a greatly effect of routing success. The parameters are:

- The way you place the individual parts in the board.
- Design parameters

Note: The part position could be modified only in layout not in Smart route!

4. State the needed steps to modify the placing of the part?……
   …….

The routing parameters

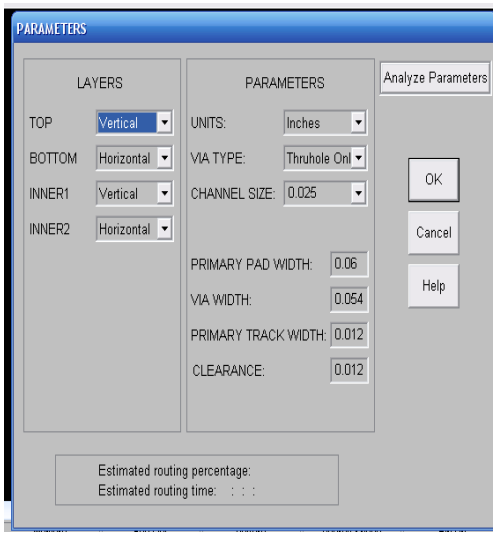


5. Layout passes all design parameter information to SmartRoute. Verify that the design parameters are expected. (Such as board technology, number of layers, and pad, track,

and clearance sizes).It could be changed them using the options in this dialog box.

Layers

The Layers box lists the copper layers as defined in Layout Plus. The dominant directions of the routing layers could be modified



Write the required changes you must do

- If a single layer circuit is selected……
- If a double layer circuit selected……..

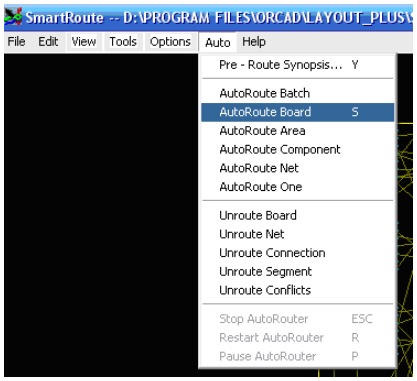
Parameters

In the Parameters dialog box, you can Check the parameters you set in Layout Plus (including units, pad and via width, track width, and clearance to make sure they display as expected). Before the new parameter settings are accepted in SmartRoute, you must choose the OK button in the Parameters dialog box and respond to the questions that display. The answers you provide confirm your decision to modify parameters before the changes are accepted by SmartRoute.

- Write the meaning of Via type …… and Clearance……...
- Make your design track width 0.6 mm and the pad width 2.2mm.
  State a comparison between via and padstack ……..

To Autoroute the board

From the Auto menu, provides multiple choices of autorouting SmartRoute initiates the autorouting sequence specified in the Routing Passes dialog box.



To pause the autorouter

From the Auto menu, choose the PauseAutoRouter command. SmartRoute temporarily suspends the autorouting sequence.

- To restart the autorouter after a pause choose ……..……
- To stop the autorouter Choose the ……command.

- Restarting the routing sequence starts the routing process from the ……

Note, the routing contentions appears when a track segment crossing a track segment of a different net (When a contention is created, a small yellow circle created) the number of contentions appears in the status bar. At the end of the routing, the number of contentions must be a zero.

- If you have a contentions in your design. Write a five different ways to solve this problem.

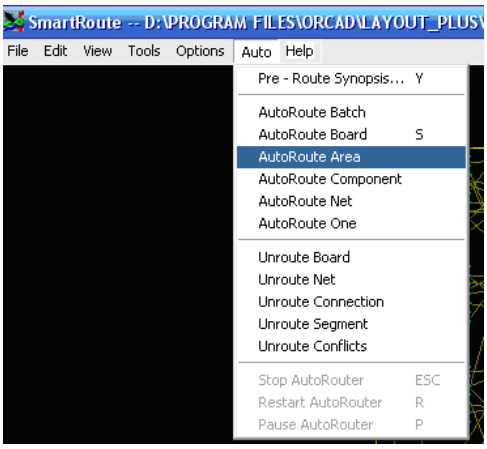
1- .....
2- .....
3- .....
4- .....
5- .....

Interactive routing

There are four interactive routing commands that are actually autorouting commands that route only portions of the board. They are AutoRoute Area, AutoRoute Component, AutoRoute Net, and AutoRoute One.

AutoRoute Area

The AutoRoute Area command routes a selected area on the board.



To autoroute a selected area on the board

From the Auto menu, choose Auto Route Area. The pointer becomes a vertical arrow. Pressing the left mouse button, drag the pointer to select the area to be routed. All connections starting or ending in the designated area are routed.

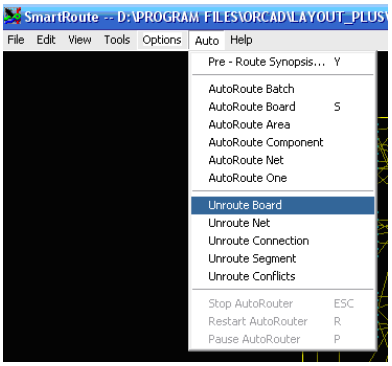
AutoRoute Component

Use the AutoRoute Component command to route all of the connections originating or ending on a pin of a component. Note that within a net, only the connections starting or ending on the selected component will be routed.

- From the Auto menu, choose AutoRoute Component. The pointer becomes a vertical arrow. Select a component. The connections starting or ending on a pin on the component are automatically routed
- There are another two types of interactive routing..... and .....
- Try to make them in your circuit and write the difference between them.....

Deleting routes

In SmartRoute, it is possible to unroute routed tracks using five commands on the Auto menu. You have several levels of routing deletion to choose from: Unroute Board.



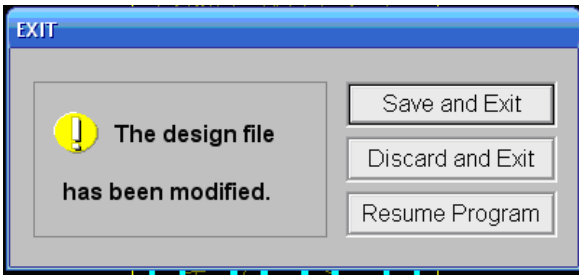
- Use the Unroute Board command to delete all routing on the entire board, even tracks that were routed in Layout Plus (including locked preroutes), or in previous SmartRoute sessions.
- When you choose this command, SmartRoute prompts you to make sure that you really want to unroute all of the nets on the board. This command cannot be undone using the Undo command.
- To Unroute the net of vcc in your circuit …….

Closing a design and exiting SmartRoute

To close a design in SmartRoute, you must either open another design, or exit SmartRoute (there is no Close command).

To exit SmartRoute

- From the File menu, choose Exit. If there are unsaved changes in the design, SmartRoute prompts you with the following three options. Select the desired option.



- Save and Exit SmartRoute opens the Save As dialog box. Choose the OK button. SmartRoute saves the design and exits.
- Discard and Exit SmartRoute discards the unsaved changes and exits.
- Resume Program This option cancels the Exit command.

1-7.

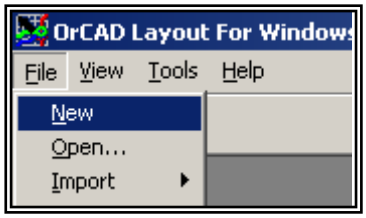
1-8. OrCAD Layout

ORCAD Layout is a powerful circuit board layout tool that has all the automated functions you need to quickly complete your board

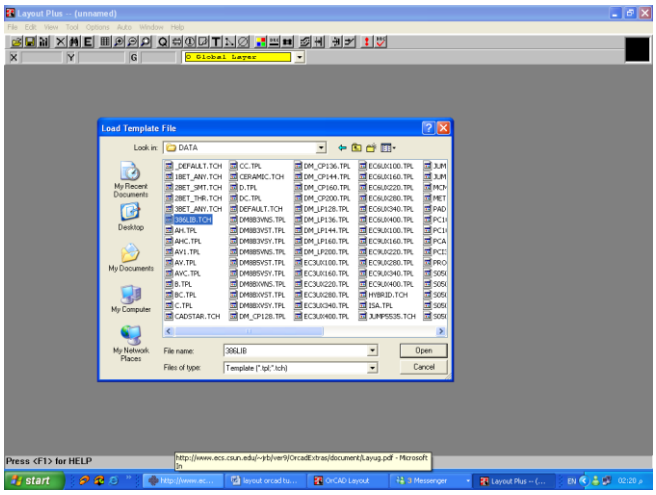
1-8-1. Creating a New design

You can open a new design or an existing design. When you open a new board design, Layout prompts you to choose a template and a schematic netlist. A board template provides the framework within which you can create a board design. A netlist describes the parts and interconnections of a schematic design

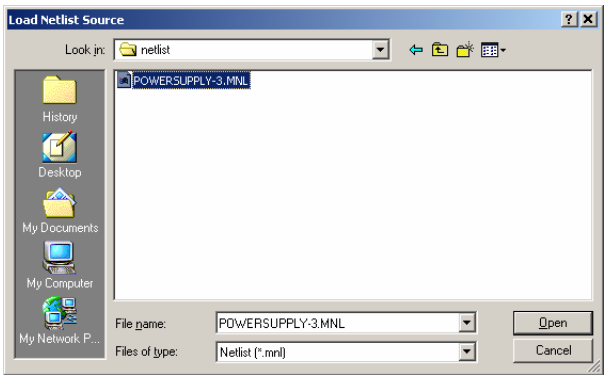
1. Start a new project by clicking on File _ New.



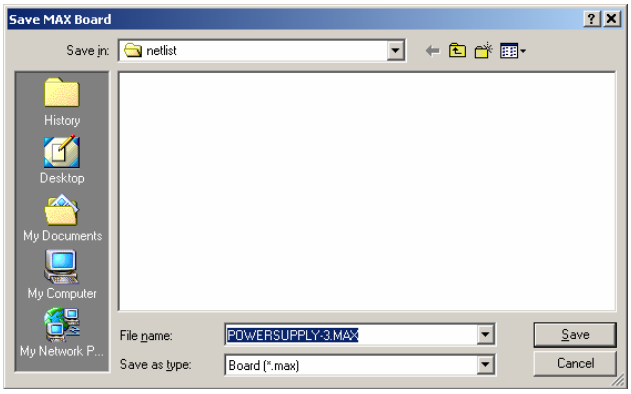
to select the arrows around its outside and deleting them.



2. Now load the netlist you exported from OrCAD. Once again, by default it is in the same directory as your Capture file.

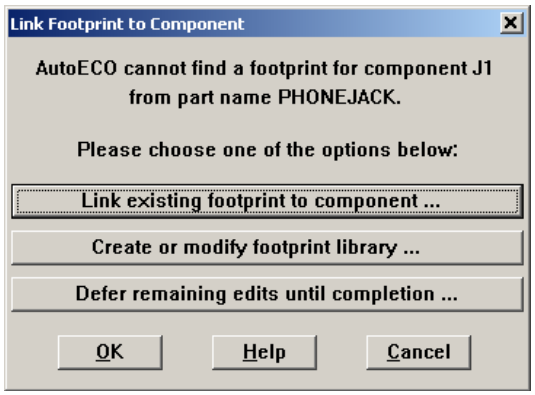


3. Now you must pick a name to save the Layout file as.(filename.max)



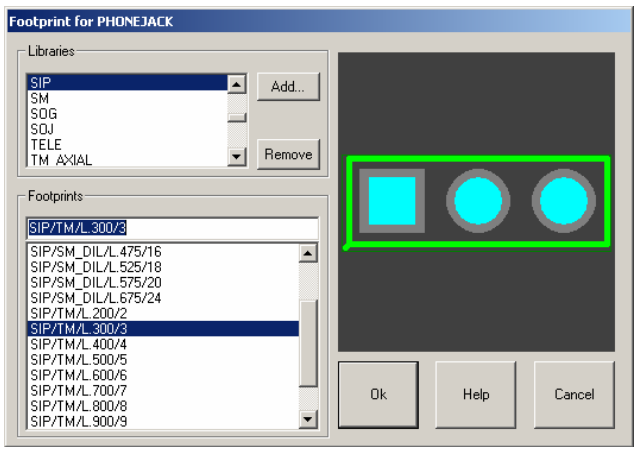
can it not find the footprint for these parts? I took them straight out of the OrCAD libraries." Well, you could have all sorts of different sized capacitors and resistors (Surface mount, axial, radial, etc.) And it may take you a very long time to find the right sized footprint, but it is critical to you board design.

4. Click on "Link existing footprint to component" each time you see it (which will be about once per component you have in your schematic.

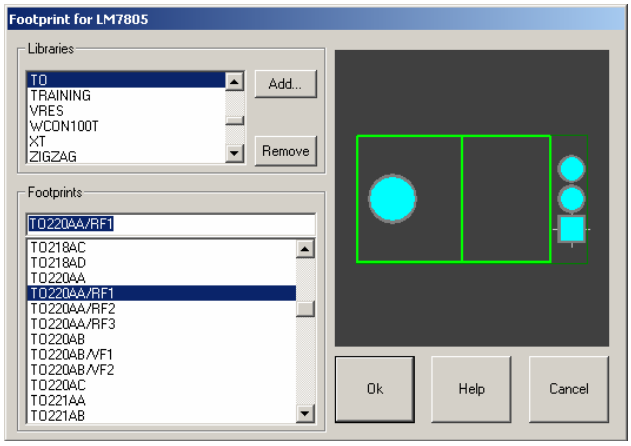


Example:

For my phonejack (which is actually a power connector) I am going to use a 3 pin SIP socket that is .300” wide with .100” spacing between pins.



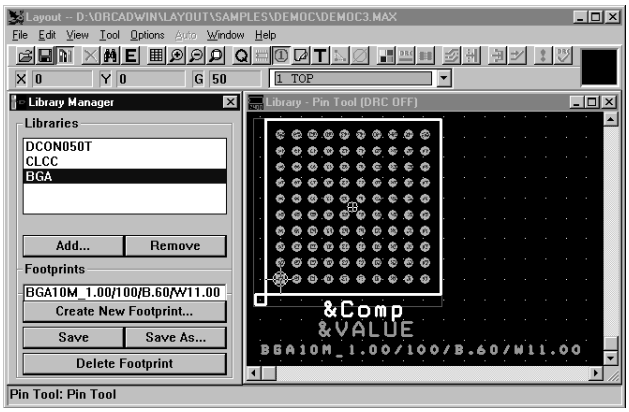
My LM7805 is a TO220 package with 3 pins, and I want it mounted on the board laying



1-8-2. Footprints

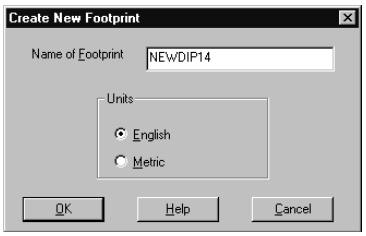
Footprints describe the physical description of components. A footprint generally consists of three object types: padstacks, obstacles (representing among other things, the physical outline of the component, silkscreen outline, assembly outline, and placement and insertion outlines), and text (for example, the component name or component value).You can view footprint data graphically in the footprint

1. To start the library manager
2. Choose the library manager toolbar button. Or From the File menu, choose Library Manager.



From The library manager and footprint editor.Creating and editing footprints You can create new footprints and add them to the libraries of your choice.

3. 1 In the library manager, choose the Create New Footprint button. The Create New Footprint dialog Note:you can create a footprint from link footprint to component screen box appears.

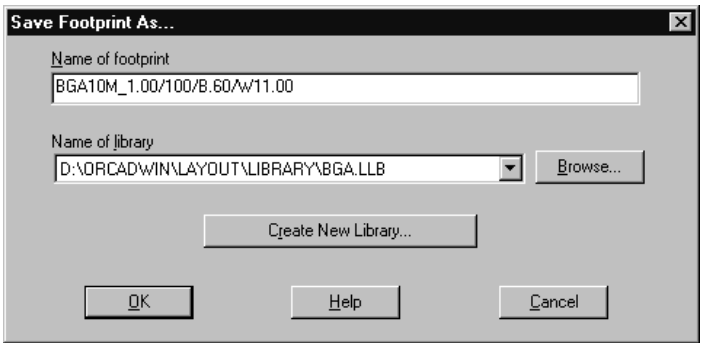


4. Enter a name for the new footprint. If the footprint is to be a metric footprint, select the Metric option.
5. Choose the OK button. The footprint origin, one pin and default text objects display in the footprint editor.

To create a custom footprint library

1. Choose the library manager toolbar button. The library manager appears.

2. In the Footprints list, select a footprint to save to the new library. The footprint appears in the footprint editor.
3. Choose the Save As button. The Save Footprint As dialog box appears.
4. Choose the Create New Library button. The Create New Library dialog box appears.



5. Enter the name for the new library (using a .LLB extension) in the File name text box, select a directory for the library, then choose the Save button.
6. Choose the OK button to close the Save Footprint As dialog box. The new library is added at the top of the Libraries list.
7. Add footprints to the new library by following the instructions in Adding, copying, and deleting footprints

1-8-2-1. Editing padstacks

You can edit the default padstack definitions predefined in Layout, or padstacks that you have defined while setting up the board. Editing changes you make in the Edit Padstack dialog box are applied to all layers of the padstack. Editing changes you make in the Edit Padstack Layer dialog box are only applied to the selected layer.

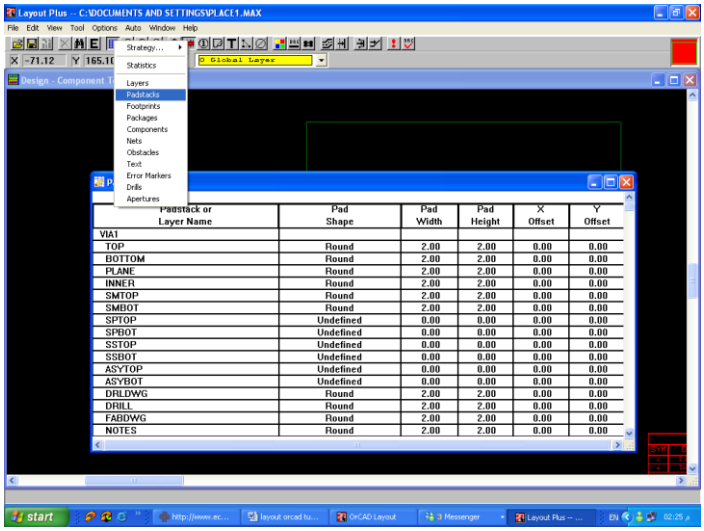
To edit a padstack on all layers

1. Choose the spreadsheet toolbar button, then choose Padstacks. The Padstacks spreadsheet appears.
2. Double-click on the padstack name. The Edit Padstack dialog box appears.
3. Edit the settings as desired

To edit a padstack on selected layers

1. Choose the spreadsheet toolbar button, then choose Padstacks. The Padstacks spreadsheet appears.
2. Double-click on a layer name. The Edit Padstack Layer dialog box appears.

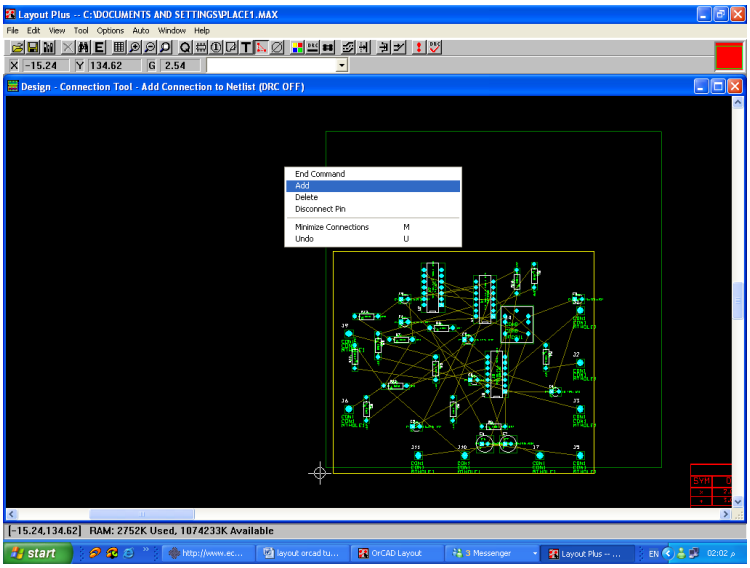
3. Edit the settings as desired (choose the dialog box's You can add a new layer to your board and copy the padstacks from an existing layer to the new layer.



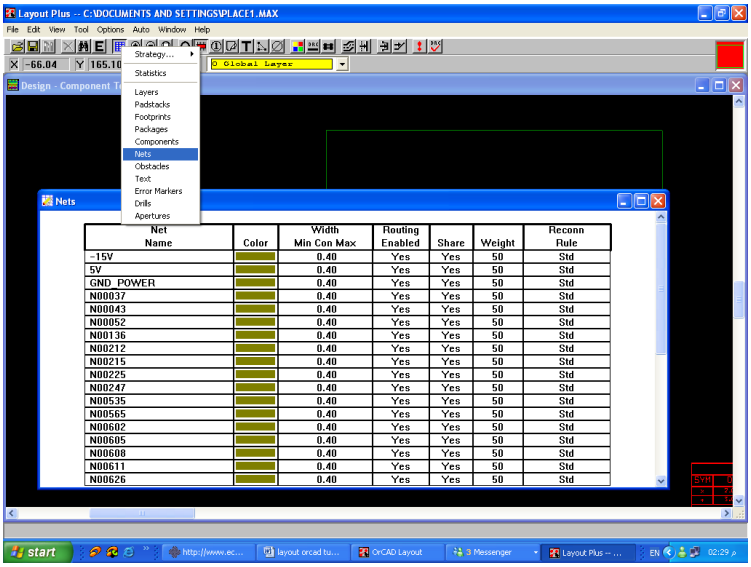
Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
VIA1					
TOP	Round	2.00	2.00	0.00	0.00
BOTTOM	Round	2.00	2.00	0.00	0.00
PLANE	Round	2.00	2.00	0.00	0.00
INNER	Round	2.00	2.00	0.00	0.00
SMTOP	Round	2.00	2.00	0.00	0.00
SMBOT	Round	2.00	2.00	0.00	0.00
SPTOP	Undefined	0.00	0.00	0.00	0.00
SPBOT	Undefined	0.00	0.00	0.00	0.00
SSTOP	Undefined	0.00	0.00	0.00	0.00
SSBOT	Undefined	0.00	0.00	0.00	0.00
ASYTOP	Undefined	0.00	0.00	0.00	0.00
ASYBOT	Undefined	0.00	0.00	0.00	0.00
DRLDWG	Round	2.00	2.00	0.00	0.00
DRILL	Round	2.00	2.00	0.00	0.00
FABDWG	Round	2.00	2.00	0.00	0.00
NOTES	Round	2.00	2.00	0.00	0.00

1-8-3. Creating a new net

1. Choose the connection toolbar button.
2. From the pop-up menu, choose Add.
3. Select a component pin.
4. Draw the new net and click the left mouse button on the end pad. The Modify Nets dialog box appears.
5. Enter the name of the new net, then choose the OK button.
6. From the pop-up menu, choose End Command.



To change the sitting of nets

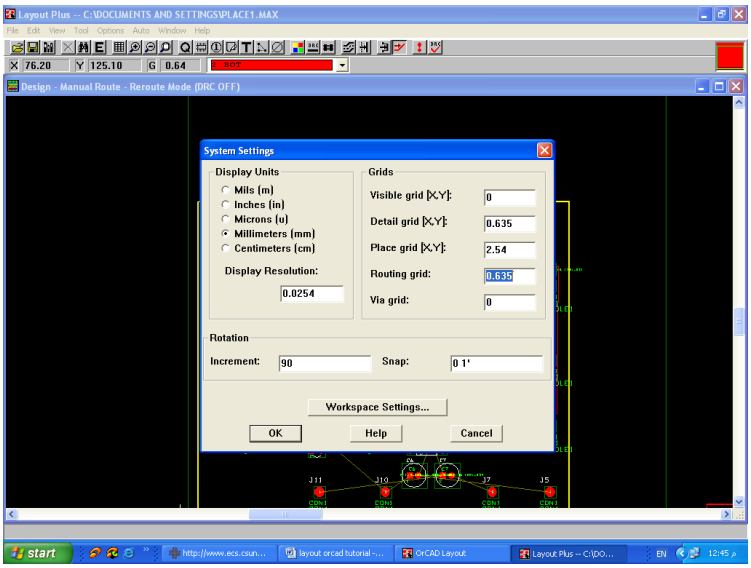


To set measurement units

1. Open your board in Layout.
2. From the Options menu, choose System Settings. The System Settings dialog box appears.
3. Select mils, inches, microns, millimeters, or centimeters.
4. Choose the OK button

To set system grids

1. From the Options menu, choose System Settings. The System Settings dialog box appears.
2. Set these options, then choose the OK button.



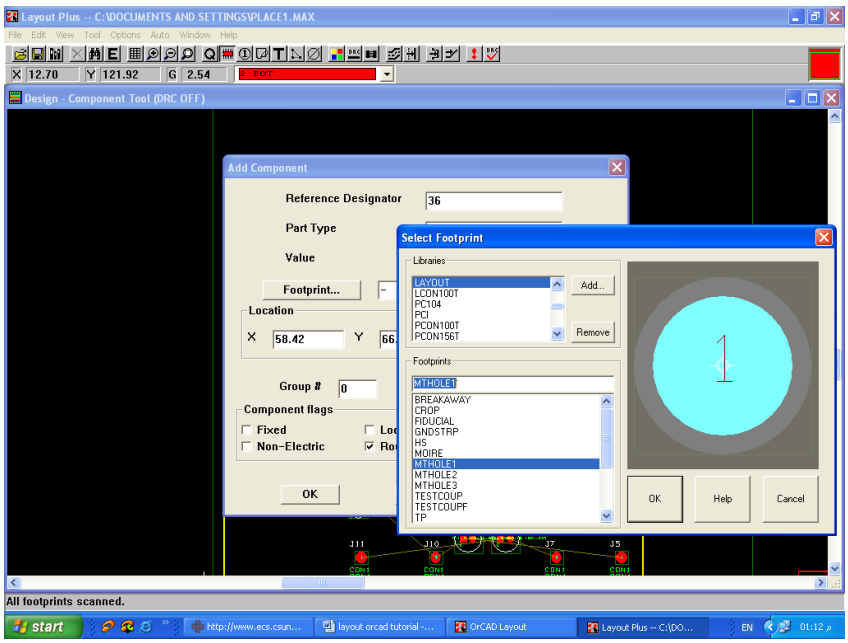
To add mounting holes to your board

1. Choose the component toolbar button.
2. From the pop-up menu, choose New. The Add Component dialog box appears.
3. Choose the Footprint button. The Select Footprint dialog box appears.
4. In the Libraries group box, select LAYOUT.LLB. Use the Add button, if necessary, to add this library to the list of available libraries. (LAYOUT.LLB resides in the LIBRARY directory.)
5. In the Footprints group box, select a mounting hole (OrCAD provides three: MTHOLE1, MTHOLE2, and MTHOLE3). Choose the OK button to close the Select Footprint dialog box.
6. As the same if you want add new component

To define layers for routing

1. Choose the spreadsheet toolbar button, then choose Layers. The Layers spreadsheet appears..
2. Review the type assignments for the routing layers and double-click in the Layer Name column of a layer you want to modify. The Edit Layer dialog box appears.
3. In the Layer Type group box, select the desired option (for example, to disable a layer for routing, select Unused Routing; to define an additional plane layer, select Plane Layer).
4. If you changed a routing layer to a plane layer, change the Layer LibName to PLANE.

5 Choose the ok button

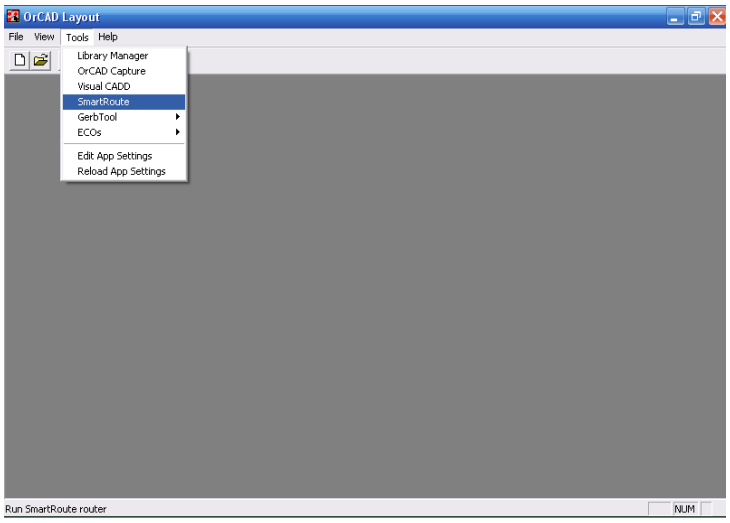


1-9. Starting SmartRoute

Start SmartRoute from the Layout Plus session frame. To start SmartRoute

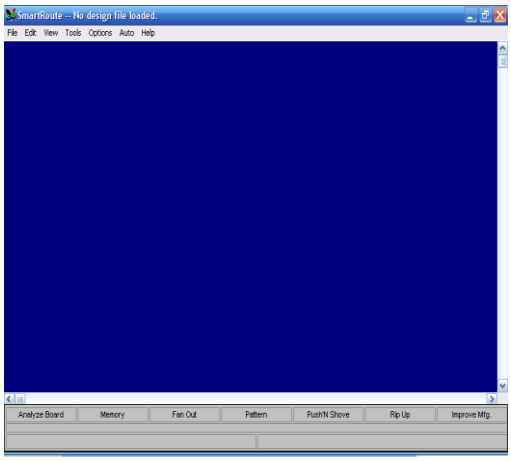
1. From the Tools menu in the Layout Plus session frame, choose SmartRoute.

Note if you are running a version of Layout other than Layout Plus, the Tools menu lists SmartRoute Demo instead of SmartRoute. In this case, you will only be able to run SmartRoute in demonstration mode.



1-9-1. The SmartRoute session frame

Once you start SmartRoute, you see the SmartRoute session frame. This is the area where the board is displayed.

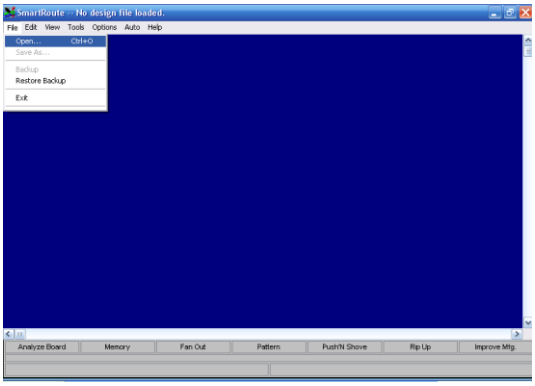


Before you load a design, the title bar at the top of thesession frame reads, “No design file loaded.” When you open a design, that is replaced

with the design's name. In SmartRoute, you can only open one design file at a time. At the bottom of the session frame, you see the names of the seven routing passes available for the autorouting sequence.

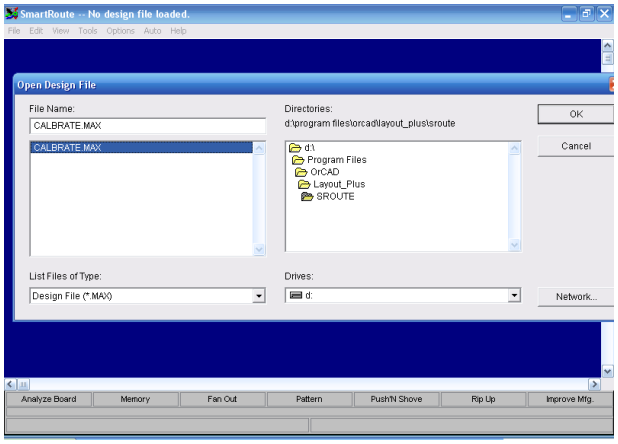
To open a design

1. From the File menu, choose Open. The Open Design File dialog box displays.



2. Locate and select a .MAX design file.
3. Choose the OK button.

Tip the files that you have opened most recently are listed at the bottom of the File menu. You can select files from this list to open them. This is the fastest way to open designs that you have worked on recently.

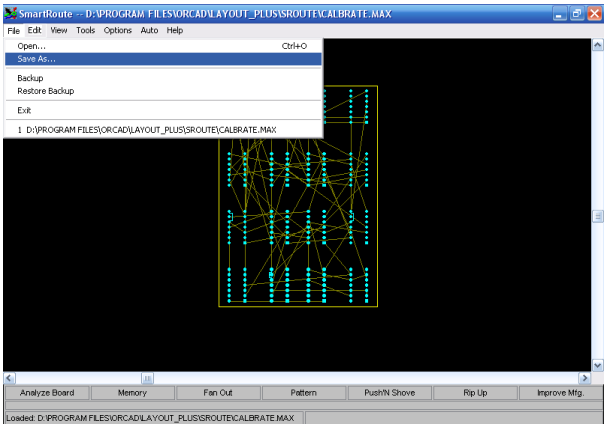


Saving a design

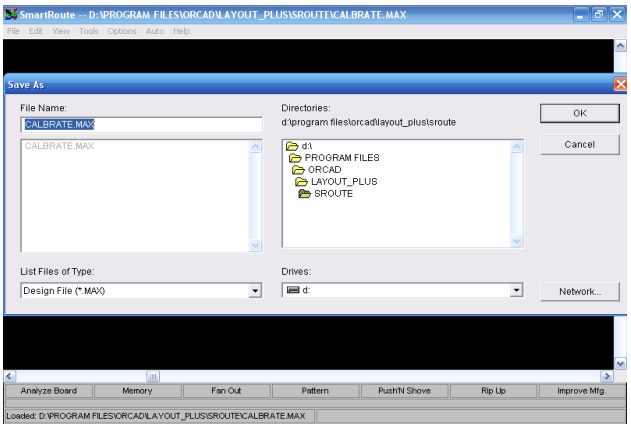
You save SmartRoute designs using the Save As command. You can also use the Backup command to automatically save designs.

To save a design

1. From the File menu, choose Save As. The Save As dialog box displays.



2. To save a board under a new name, enter the name of the file, locate the target directory, and choose the OK button. *Or* To save the board under the same name, just choose the OK button. SmartRoute asks you if you want to replace the existing file. Choose the Yes button.



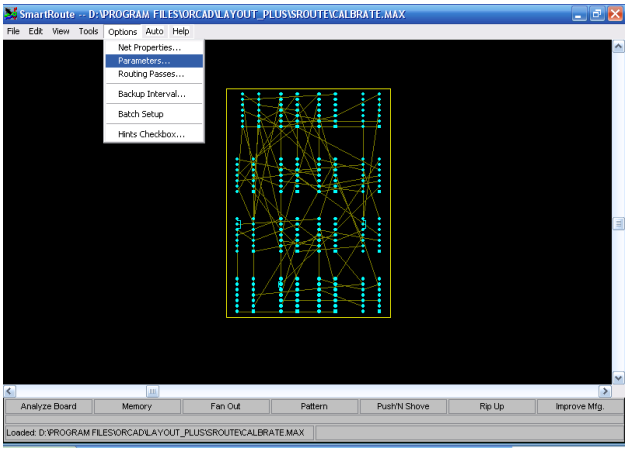
1-9-2. Setting parameters

After the net properties have been set, set the design parameters. There are three categories of parameters. They are all controlled in the Parameters dialog box.

- Layers
- Design parameters
- Analyze parameters

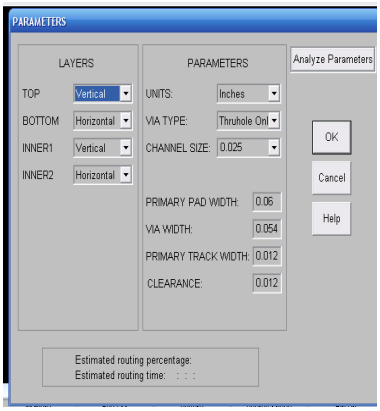
To change the parameters for routing

1. From the Options menu, choose Parameters. The Parameters dialog box displays.
2. To bias the direction for routing on each layer, select the desired option from the drop-down list adjacent to the layer name.
3. Change the parameters for Units, Via Type, or Channel by selecting the appropriate options from the drop-down lists.



4. Change the parameters for Primary Pad, Via Width, Primary Track, or Clearance by typing new values in the text boxes.
5. Choose the Analyze Parameters button. SmartRoute analyzes the effects of the parameters that you set, and displays the results at the bottom of the dialog box.
6. When your parameter settings are as desired, choose the OK button.

The Parameters dialog box



- **Layers**

The Layers group box lists the copper layers as defined in Layout Plus. You can select a direction in which routing will be biased for each layer. The choices are listed below.

Best Choice SmartRoute selects the direction for the layer.

Disabled No routing occurs on the layer.

Fanout The router will fanout vias on this layer but will not otherwise route on it. Use this option when you wish to fanout the layer containing the SMD pads and also restrict routing on that layer.

Plane The layer is reserved for use as a plane layer upon its return to Layout Plus. When this option is selected, the layer is no longer displayed in the Parameters dialog box.

Vertical The tracks are biased to be routed vertically.

Horizontal The tracks are biased to be routed horizontally.

Any Direction The router is not biased in any direction. The suggested use for this option is on the third layer of a three-layer board. Do not use this option on more than one layer.

Angled options Options include right and left 45° angles, 1 o'clock, 2 o'clock, 4 o'clock, and 5 o'clock angles. These options will bias the layer in the direction selected.

The options may be used for all layers on a multilayer board, although top and bottom layers are usually horizontally or vertically biased. These options are usually used by board designers to achieve shorter track lengths and fewer vias. These options can only be used on multilayer boards.

- **Parameters**

Parameters are read directly from Layout Plus. In the Parameters dialog box, you can check the parameters you set in Layout Plus—including units, pad and via width, track width, and clearance—to make sure they display as you expect. Before the new parameter settings are accepted in SmartRoute, you must choose the OK button in the Parameters dialog box and respond to the questions that display. The answers you provide confirm your decision to modify parameters before the changes are accepted by SmartRoute.

Units From the drop-down list, select the desired data structure units for autorouting. OrCAD recommends that you use the same unit structure that you used in Layout Plus.

Via Type From the drop-down list, select the type of vias that you want to use on your board.

Channel in SmartRoute, the channel size that displays is automatically calculated by SmartRoute for your board.

OrCAD strongly recommends that you use the default channel size calculated by SmartRoute. When you return to Layout Plus, the system grid value will reflect the channel size selected by SmartRoute. If you have different grid requirements, you must change the system grid in Layout Plus.

Primary Pad The Primary Pad option displays the diameter width of the most commonly used pad on the board. If there are no through-hole pads, the Primary Pad option displays the width of the largest SMD pad.

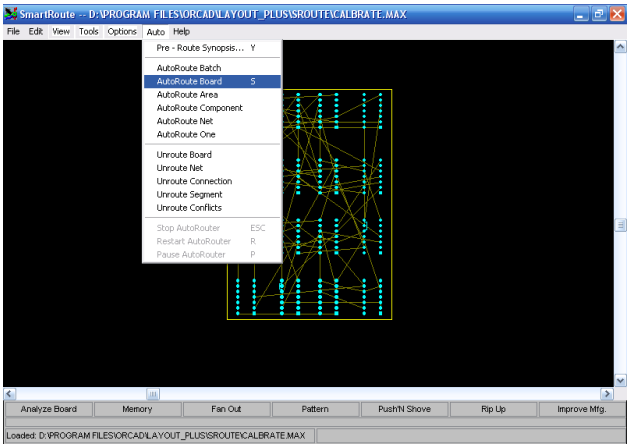
Via Width The via width is the same as the first via defined in Layout Plus. SmartRoute, however, will choose the best via size for a given situation when routing.

Primary Track The primary track width is the routing width of the majority of the nets as defined in Layout Plus

Clearance The Clearance option specifies the spacing required between tracks (track-to-track clearance). This value is defined in Layout Plus.

1-9-3. Autorouting the board

1. From the Auto menu, choose AutoRoute Board. SmartRoute initiates the autorouting sequence specified in the Routing Passes dialog box.

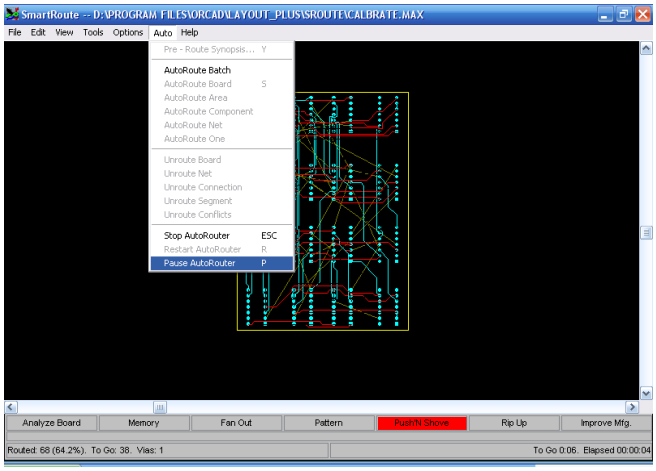


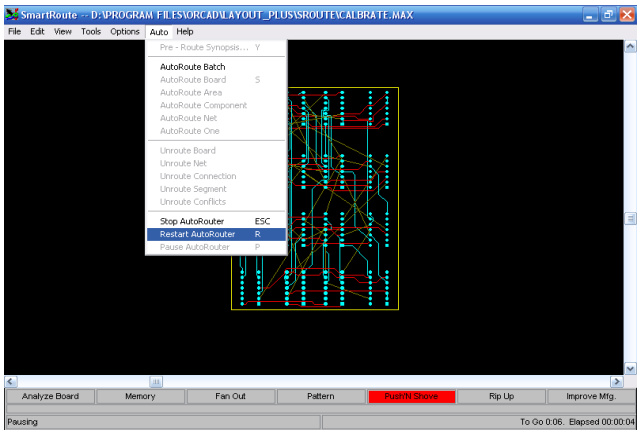
Note as the router progresses, tracks may display small, jagged steps. SmartRoute automatically runs a pass that cleans up tracks and minimizes vias during routing.

To pause the autorouter

1. From the Auto menu, choose Pause AutoRouter. SmartRoute temporarily suspends the autorouting Sequence.

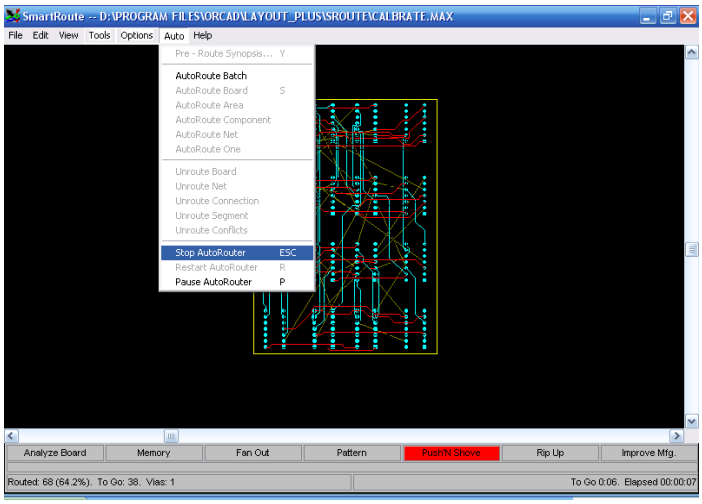
Note To restart the autorouter, choose Restart AutoRouter from the Auto menu. SmartRoute restarts the routing process from the point at which it paused.





To stop the autorouter

1. From the Auto menu, choose Stop AutoRouter. SmartRoute ends the autorouting sequence.



Note To restart the routing sequence, choose the autoroute command of your choice from the Auto menu. SmartRoute starts again at the first enabled routing pass.

1-9-4. Editing the board

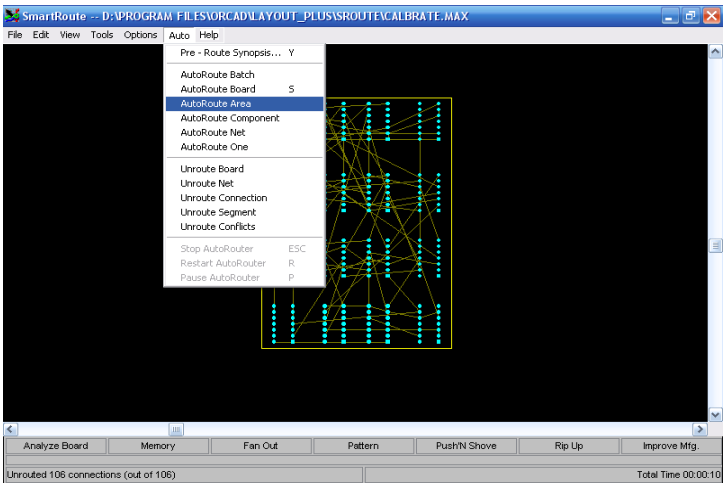
Interactive routing

There are four interactive routing commands that areactually autorouting commands that route only portions of the board. They are AutoRoute Area, AutoRoute Component, AutoRoute Net, and AutoRoute One.

AutoRoute Area

The AutoRoute Area command routes a selected area on the board.To autoroute a selected area on the board

1. From the Auto menu, choose AutoRoute Area. The pointer becomes a vertical arrow.
2. Pressing the left mouse button, drag the pointer to select the area to be routed. All connections starting or ending in the designated area are routed.

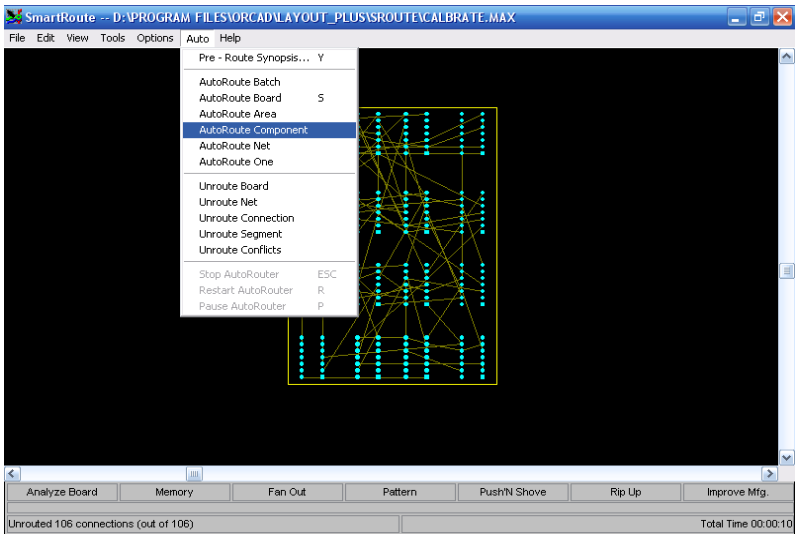


AutoRoute Component

Use the AutoRoute Component command to route all of the connections originating or ending on a pin of a component. Note that within a net, only the connections starting or ending on the selected component will be routed.

To autoroute the connections originating or ending on a pin of a component

1. From the Auto menu, choose AutoRoute Component. The pointer becomes a vertical arrow.
2. Select a component. The connections starting or ending on a pin on the component are automatically routed.

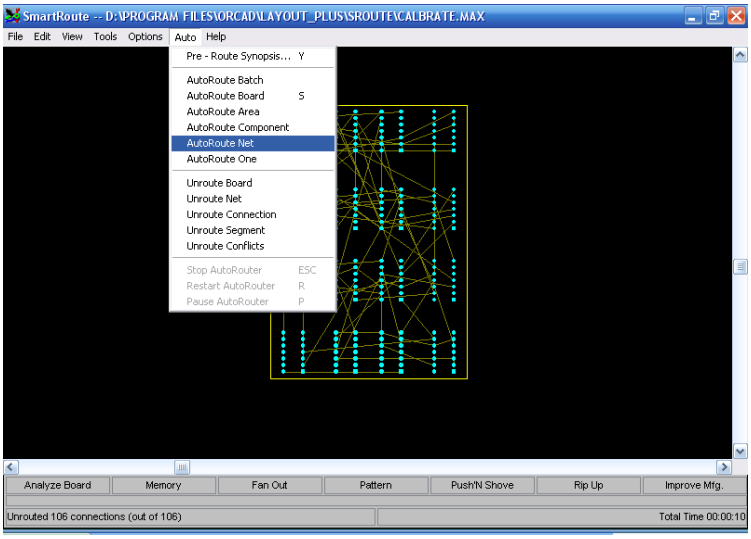


AutoRoute Net

Using the AutoRoute Net command, you can route all of the connections associated with a net.

To autoroute the connections associated with a net

1. From the Auto menu, choose AutoRoute Net. The pointer becomes a vertical arrow.
2. Select a connection within the net. All of the connections within that net are routed.

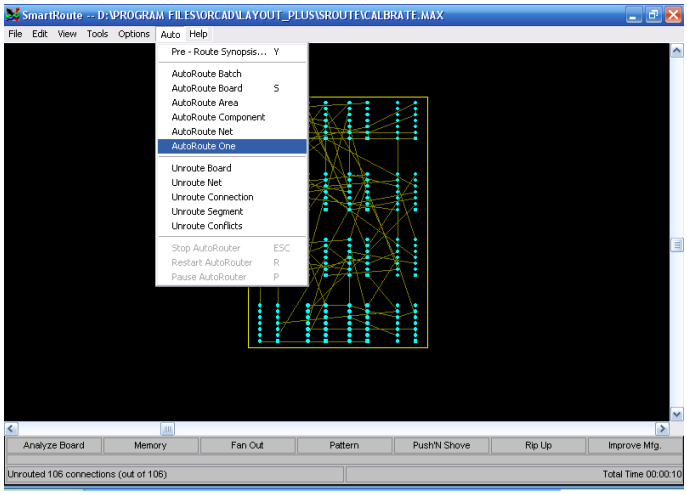


AutoRoute One

The AutoRoute One command autoroutes one connection at a time.To autoroute one connection

1. From the Auto menu, choose AutoRoute One. The pointer becomes a vertical arrow.

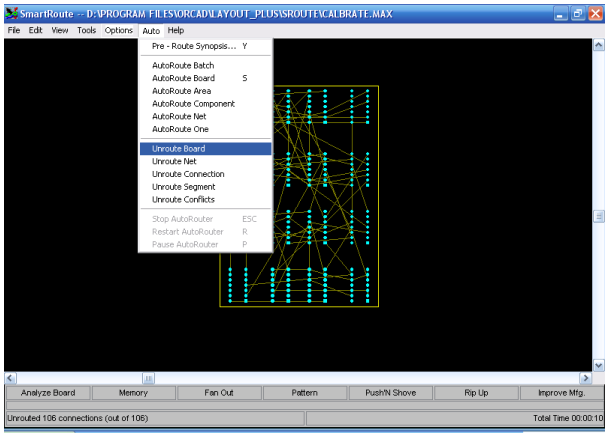
2. Place the pointer over any connection to be routed and click the left mouse button.
3. Repeat step 2 for each connection that you want to route.



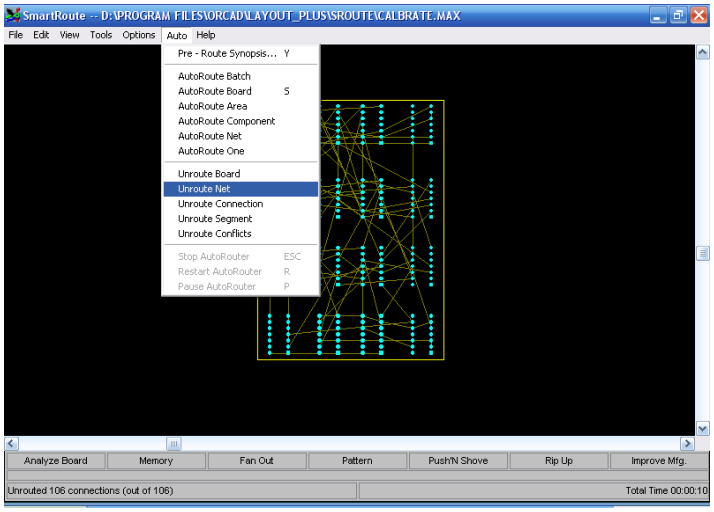
Deleting routes

In SmartRoute, it is possible to unroute routed tracks using five commands on the Auto menu. You have several levels of routing deletion to choose from:

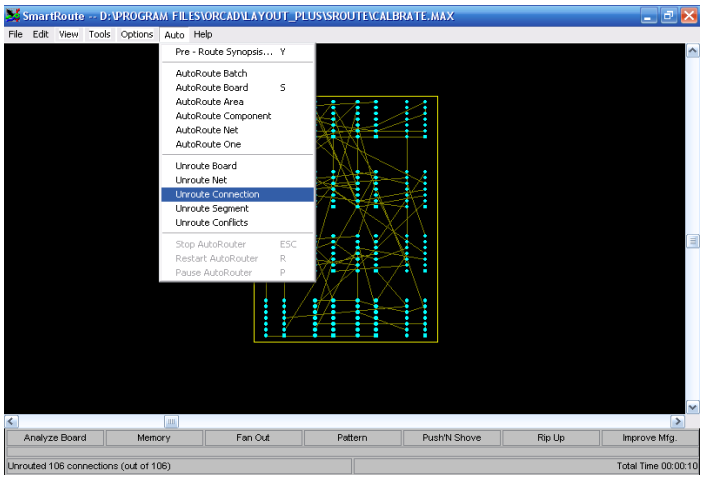
Unroute Board Use the Unroute Board command to delete all routing on the entire board, even tracks that were routed in Layout Plus (including locked preroutes), or in previous SmartRoute sessions. When you choose this command, SmartRoute prompts you to make sure that you really want to unroute all of the nets on the board. This command cannot be undone using the Undo command.



Unroute Net Use the Unroute Net command to unroute one routed net. To do so, choose the Unroute Net command from the Auto menu and select the net that you want to unroute.



Unroute Connection Use the Unroute Connection command to unroute one connection (a connection is an unrouted net that connects two pads). To do so, choose the Unroute Connection command from the Auto menu and select the connection that you want to unroute.



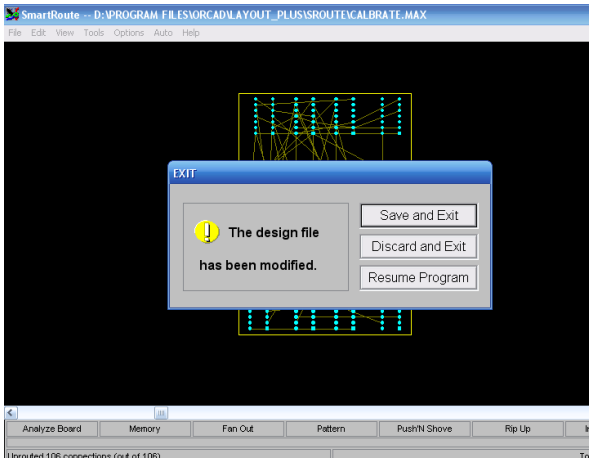
1-9-5. Closing a design and exiting SmartRoute

To close a design in SmartRoute, you must either open another design, or exit SmartRoute (there is no Close command). For information on opening a design, see

To exit SmartRoute

1. From the File menu, choose Exit. If there are unsaved changes in the design, SmartRoute prompts you with the following three options. Select the desired option.
2. Save and Exit SmartRoute opens the Save As dialog box. Choose the OK button. SmartRoute saves the design and exits.

3. Discard and Exit SmartRoute discards the unsaved changes and exits.
4. Resume Program This option cancels the Exit command.



1-10. Gerber Format; Rules and Guidelines

This section provides background information, describes organization, and presents guidelines for use of RS-274X.

1-10-1. File structure

An RS-274X plot file is a file consisting of RS-274X parameters and standard RS-274D codes which, when correctly interpreted, result in an image that may be displayed or plotted.

1-10-1-1. Data blocks

The file is composed of a number of data blocks containing parameters and codes. Each data block is delimited by an end-of-block character, typically an asterisk (*). Each data block may contain one or more parameters or codes. For example:

X0Y0D02*
X50000Y0DO1*

D-code	Function
D01 or D1	Shutter open (begin draw).
D02 or D2	Shutter closed.
D03 or D3	Flash.
D10 and higher	Apertures.

1-10-1-2. Layers

One or more data blocks may be grouped into a layer of information that describes part of a graphic image. In RS-274X context, a layer is a named information component of the image composed of one or more data blocks. Each layer may have characteristics, such as name, polarity, and interpolation mode that differ from other layers of information.

Note: A layer must not be confused with a PCB layer. A PCB layer has a physical definition and might be compared to a physical plane. An RS-274X layer is simply a group of data blocks that may be manipulated collectively and separately from other layers.

1-10-2. Data types

An RS-274X file may contain the following kinds of data appearing in the following general order:

1. **RS-274X Parameters**: are also called mass parameters or extended Gerber format. The inclusion of these parameters in the file makes the plot file RS-274X, or X data, instead of standard RS-274D.
2. **Standard RS-274D Codes:** were once called *word address* format. They consist of:
   - One-character function codes such as G codes, D codes, M codes, etc. Function codes were the words of the old terminology. They describe how coordinate data associated with them should be interpreted (such as linear or circular interpolation), how the imaging device should move (light source on or off), and more.
   - Coordinate data define points to which the imaging device must move. The coordinate data represented the address of the old terminology. X,Y coordinate data describe linear positions. I, J coordinates define arcs.

1-10-3. RS-274X parameters

RS-274X parameters define characteristics that apply to an entire plot or to a single layer, depending on the parameter's position in the file and whether it generates a new information layer in the file (as, for example, layer-specific parameters do). RS-274X parameters consist of two alpha characters followed by one or more optional modifiers.

RS-274X parameters are delimited by a parameter delimiter, typically a percent (%) sign. Because parameters are also contained in a data block, they are also delimited by an end-of-block character (*). For example,

%FSLAX23Y23*%

RS-274X parameters may be grouped according to the scope of their function in the file. The groups should appear in the file in the following order:

1. Directive parameters control overall file processing.
2. Image parameters supply information about an entire image.
3. Aperture parameters describe the shape of lines and components throughout the file.
4. Layer-specific parameters describe processing of one or more data layers.
5. Miscellaneous parameters provide capabilities that do not fall into the above groups.

RS-274X parameters are generally placed at the beginning of the file in the order shown above. Certain parameters, such as the layer-specific parameters, may be embedded within the file. The next sections describe each parameter type.

1-10-4. Directive parameters

Directive parameters control overall file processing. They include:

AS Axis Select
FS Format Statement
MI Mirror Image
MO Mode of units
OF Offset
SF Scale Factor

As a general rule, directive parameters should be placed at the beginning of the file. Each directive parameter controls processing until another like it is encountered.

1-10-5. Image parameters

Image parameters supply information about the entire (composite) image. Image parameters include:

IJ Image Justify
IN Image Name
IO Image Offset
IP Image Polarity
IR Image Rotation
PF Plotter Film

If an image parameter occurs more than once in a file, the last one encountered will be the operative parameter.

1-10-6. Aperture parameters

Vector plotters control the width and shape of features by projecting light through a series of openings, or apertures, in a rotating wheel. Each position on the wheel is identified by a unique D code. When the D code appears in the data, the wheel rotates to the referenced position for exposure.

The aperture parameters include:

AD Aperture Description
AM Aperture Macro

In general, aperture parameters apply to an entire file. An exception is an embedded AD parameter, which will generate a new layer if it redefines a D code previously used in the image data.

The AM parameter describes a special aperture by using the following set of predefined aperture shapes to describe an aperture:

Circle
Line (vector)
Line (center)
Line (lower left)
Outline
Polygon
Moiré
Thermal

1-10-7. Layer-specific parameters

Layer-specific parameters supply information for the processing of one or more information layers (not to be confused with board layers). They may be used more than once in a file. Layer-specific parameters always generate a new layer and should be placed at the beginning of the new layer. If not repeated for a given layer, the previous layer-specific parameters remain in effect.

The layer-specific parameters include:

KO Knockout
LN Layer Name
LP Layer Polarity
SR Step and Repeat

1-10-8. Standard RS-274D Codes and Coordinate Data

Standard RS-274D codes (D codes, G codes, M codes, etc.) specify how the coordinate data should be manipulated. Each code applies to coordinate data located in the same data block as the code. It also applies to coordinate data following it until another code of the same type is encountered, or until a new layer is generated.

For example, G02 specifies clockwise, single-quadrant circular interpolation and is modal. All coordinate data following it will be considered clockwise arc data until another interpolation code is encountered, or until a new layer is generated.

Standard RS-274D codes may be grouped according to function. They generally appear in the file in the following sequence:

1. N codes (sequence numbers) are similar to line numbers and may be assigned to data blocks to simplify organization. Sequence numbers may be 0 to 99999. N codes are not necessary.

2. G codes (general functions) specify how to interpolate and move to the coordinate locations following the code until changed or until a new layer is generated (modal).
3. D codes (plot functions) select and control tools, specify line type, etc.
4. M codes (miscellaneous functions) perform a variety of functions such as program stop and origin specification. Standard RS-274D codes are described in detail starting on page 45.

1-10-8-1. Coordinate Data

Coordinate data includes:

- X,Y data define linear positions along the X and Y axes.
- I,J data define arcs.

For example,

X200Y200D02*

This data block directs the plotter to move in a positive direction to coordinate location 0.2,0.2 (assuming leading zeroes are omitted) with the light source off (tool up). Additional X,Y coordinate data positions following this code will also cause motion with the light source off until a different code is encountered.

1-10-9. RS-274D Data Guidelines

Follow these guidelines when preparing RS-274D data:

- Enter functions codes and coordinate data following the RS-274X parameters.
- Function codes apply to coordinate data in the same block as well as to subsequent coordinate data. They do not affect coordinate data preceding the block in which they occur.
- Enter function codes in the file in the order shown in Table 2.

Table 2 RS-274D Code Order of Entry

Code	Function	Comments
N	Sequence number	Optional
G	General functions: linear interpolation, circular interpolation, polygon area fill, etc.	Once encountered, remains in effect until countermanded.
D	Aperture or tool assignment; line/flash control	Once encountered, remains in effect until countermanded.
M	Miscellaneous function: program stop or end.	Every file must end with M00 or M02.

Sample Files

The examples on these pages illustrate the use of both mass parameters and standard RS-274D codes.

Example 1

Example 1 illustrates a single layer image.

***G04 EXAMPLE 1: 2 BOXES**	
%FSLAX23Y23*%	Format statement - leading zeroes omitted, absolute coordinates, X2.3, Y2.3.
%MOIN*%	Set units to inches.
%OFA0B0*%	No offset
%SFA1.0B1.0*%	Scale factor is A1, B1
%ADD10C,0.010*%	Define aperture D-code 10 - 10 mil circle
%LNBOXES*%	Name layer "BOXES".
G54D10	
X0Y0D02*X5000Y0D01*	
X5000Y5000D01*X0Y5000D01*X0Y0D01*	RS-274D data
X6000Y0*X11000Y0D01*	
X11000Y5000D01*X6000Y5000D01*	
X6000Y0D01*D02*	
M02*	End of data

1-10-10. Lab exercise: Prepare Gerber file settings

Experiment objectives:

- Learn to create Design file (*.gtd file) written in a gerber format style.
- Understand how to tune the gerber settings.

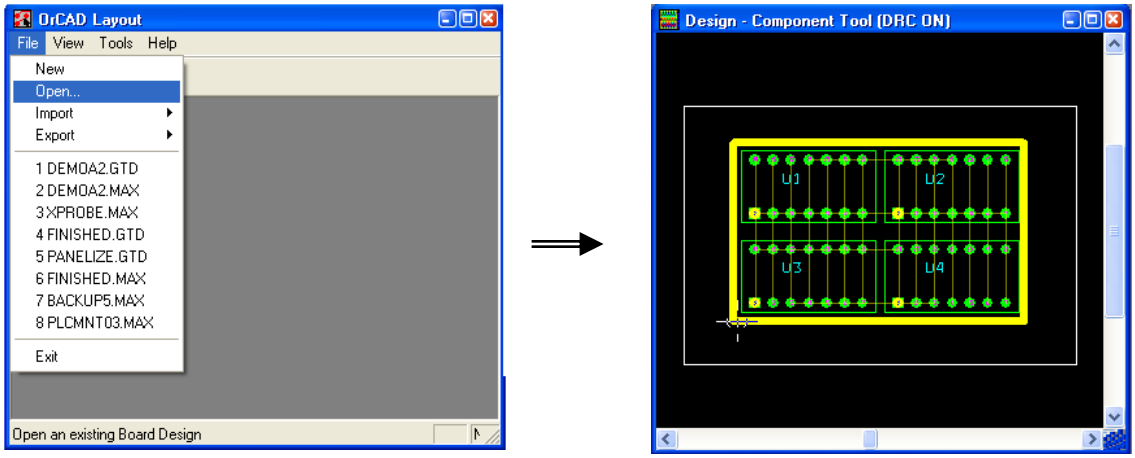
Experiment Flow:

1. Opening a new max file in Layout Plus.
2. Auto routing the desired board.
3. Editing the setting of the output files.
4. Verifying the output files.

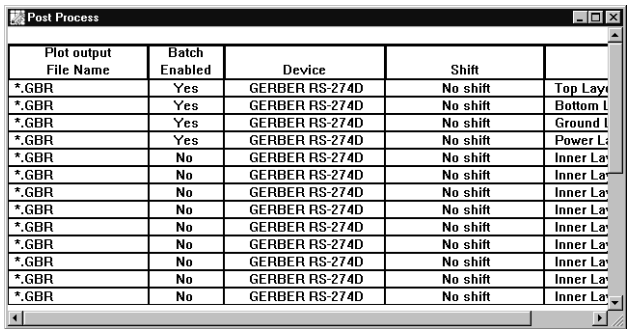
Experiment procedure:

Opening the Gerbtool

1. From start→ All programs→ Orcad Release 9 → Layout plus
2. To open a max file (PCB layout Format); from pull down menu Select File → open.



3. Select the file DemoA2.Max from the path
   C:\Program Files\OrCAD\Layout_Plus\SAMPLES\DEMOA
   Note rate nest lines (yellow lines) which indicate the connections of the components. Guess number of needed layers?..... why??
   ……
4. All gerber file format are prepared using the setings in post process spreadsheet; Display the post process spreadsheet by choosing Post process setting from options menu.



5. In the plot Output File Name column, select the layer top . Press the right mouse button, the pop up menu will be displayed select Preview. The gerber output file will be displayed for layer top. Why all connections are invasible?..... …… …… ……..…… …….
6. From Auto menu select Autoroute → Board. All rate nest lines replaced by true physical tracks.
7. View all windows simultaneously by selecting Tile option from Window menu.
8. Repeat steps 4 and 5. Is there a notable modification? Illustrate the modifications with causes? ……. ……..
9. Repeat step 5 to preview other layers.
10. From post Process window select restore Original Colors from pop up menu.
11. Tune the output file for each layer. Highlight top layer field (raw). From the pop up menu, select properties option.
12. The available formats are Gerber besides DXF format output for AutoCAD and HPGL output for printers. Select extended Gerber. Review all other options then click OK.
13. Repeat the last step for the other layers.
14. ***Batch Enabled*** column Indicates whether output will be generated for the layer ("Yes") or not ("No"). Compare the properties of contrary batch enabled layers. Which option effect Bach enable: ……
15. Process all layer have a Yes in the Batch Enabled column. Select Run Batch from pop up menu.
16. State the file name with its extension of Gerber Design file ……
17. State the file name with its extension of Drill file ……
18. Open the Drill File. Recognize and decode the drill format.

19. From list file (DEMOA2.lis). Determine the number of used D-codes ….....
20. Close the post process window.
21. Custmize the output file settings; From options menu ,select Gerber setting.
22. By using help button, clearify the perpose of the ***Create Apertures as Needed*** option…… …….....
23. End-of-Block Character:Defines the character that divides Gerber commands. Which gerber format?
    - standered (274D)
    - extended Gerber (274x)
24. Output Resolution: Either 2.3 format (mils) or 3.4 format (10th mils). Contrast the two formats?
    - 2.3 format defines arc as ……..……
    - 4.4 format defines arc as ……..
25. Click cancel.

1-10-11. Lab exercise: GerbTool

Experiment objectives:

- Learn to create Gerber files for photo plotter and CNC machine.
- Understand various skills (drawing, measuring).
- Determine the optimum results and understand how to achieve correct results.

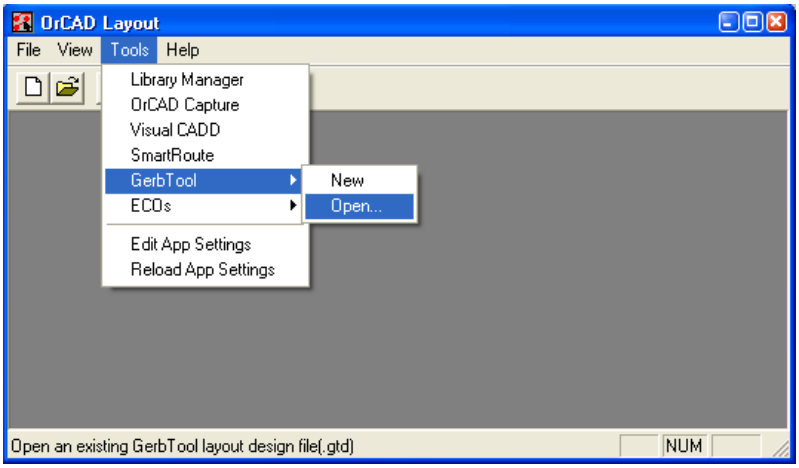
Experiment Flow:

5. Opening the Gerbtool.
6. Editing the setting of the file.
7. Drawing Skills.
8. Editing Aperture file.
9. Generating Drill File.
10. Saving the files.

Experiment procedure:

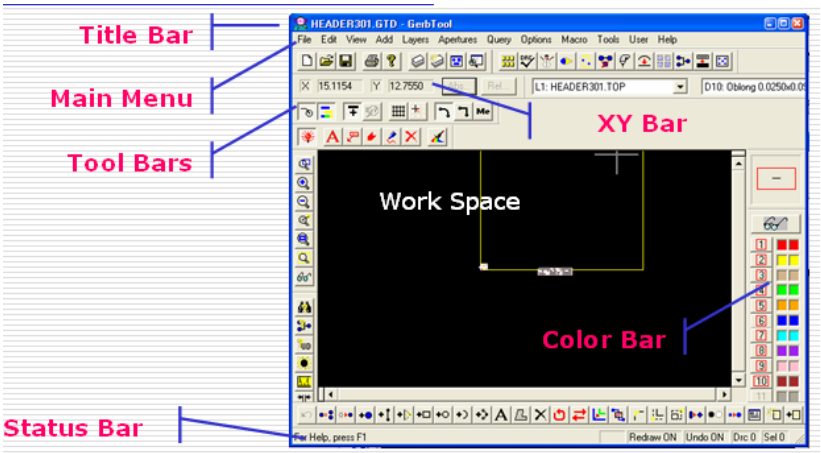
Opening the Gerbtool

26. From start→ All programs→ Orcad Relese 9 → Layout plus
27. From pull down menus select tool→ Gerb Tool → open.
28. Select the file FINISHED.GTD from the path
    C:\Program Files\OrCAD\Layout_Plus\SAMPLES\DEMO

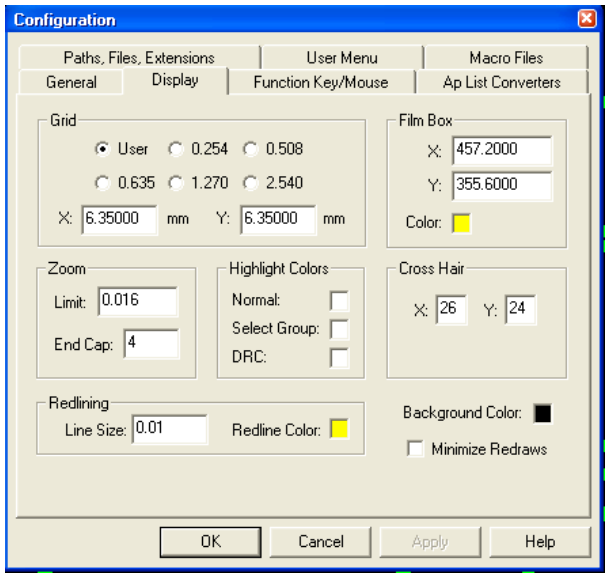


29. From color Bar toggle among the layers (deselect all, then select one by one).

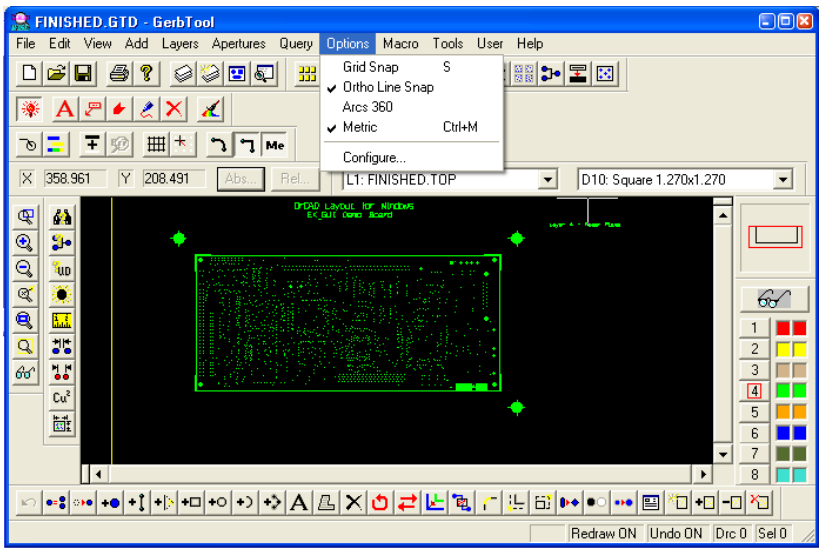
Editing the setting of the file:



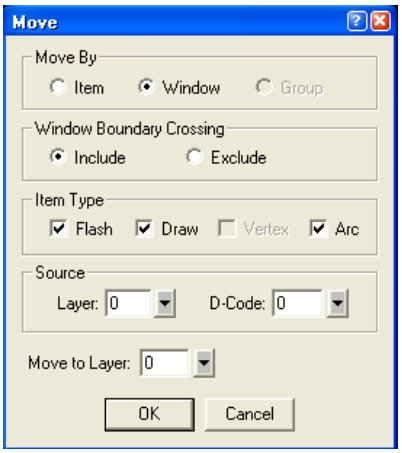
30. From options→configure, the configuration dialog box will be appeared.



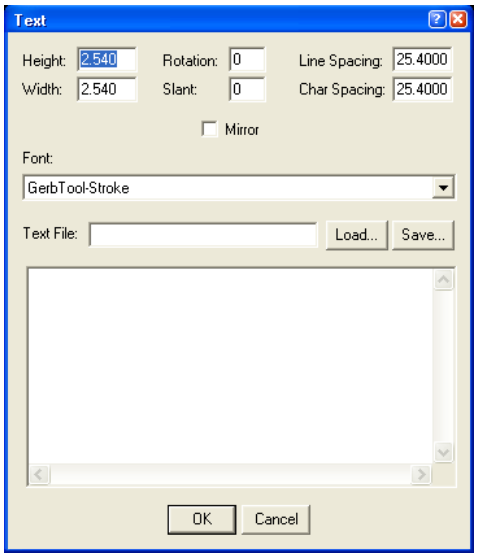
31. Select Display tab (it should be like above) if the unites in inches close the dialog box and change the units from options→ Metric or activate [Me] icon

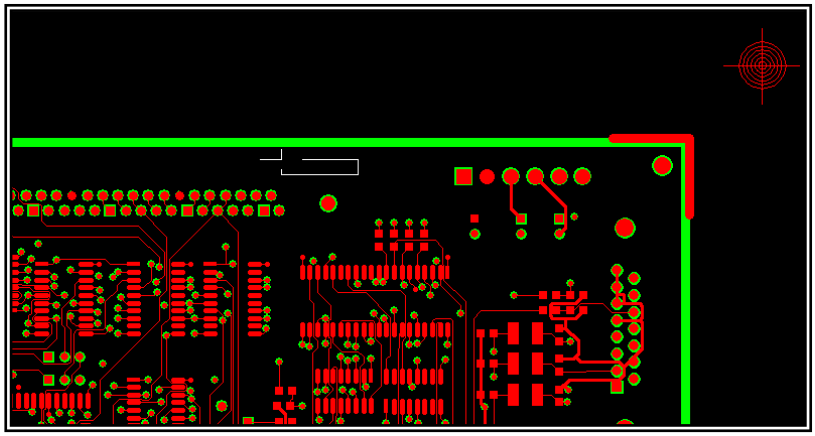


32. Repeat step 5 and 6 then type the size of film box as 500x500.
33. Assign a white color for back ground color.
34. Change the cross hair size to be 0x0.
35. By using the help button define the utility of (end cap) option:……
……
36. From paths, Files, Extensions tab define the extension of drill file …… Design File ……and Gerber File ……
37. Press OK.



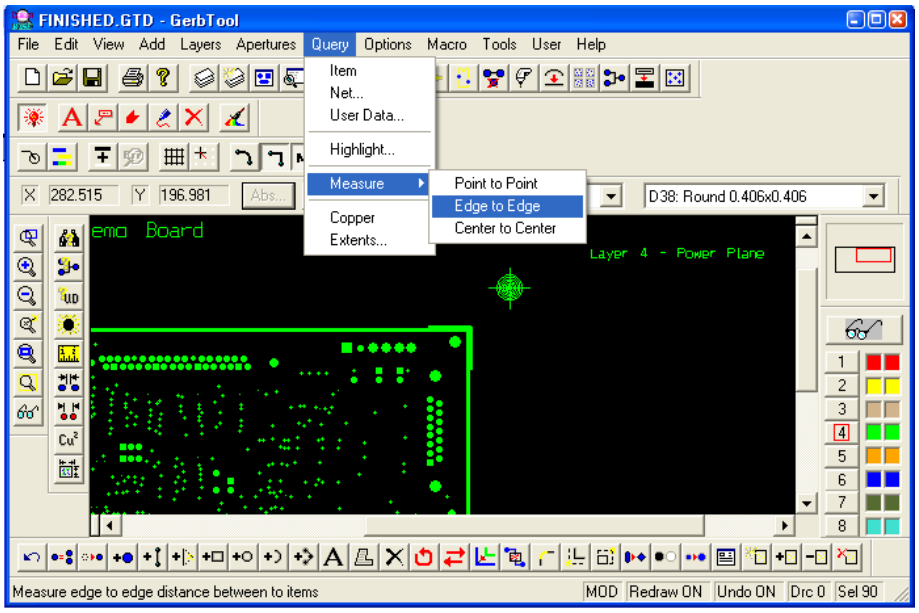
38. From Edit→ Move (the move dialog box will appear).
39. Modify the radio buttons to match the above dialog.
40. Draw a rectangle around the design and move it to the lower left corner.
41. From XY Bar select The top layer and D36
42. From Add→Text (the text dialog will appear)
43. In the blank area write your name.
44. Place the hallow rectangle as in the next figure.
45. Why your name is ambiguous?.....
    .....
46. Change the D code to D38. Attempt again to write your name. Discuss what is the effect of D-code……
    ……..





47. Write the layer name (top, bottom, inner1, etc) on each belongs.

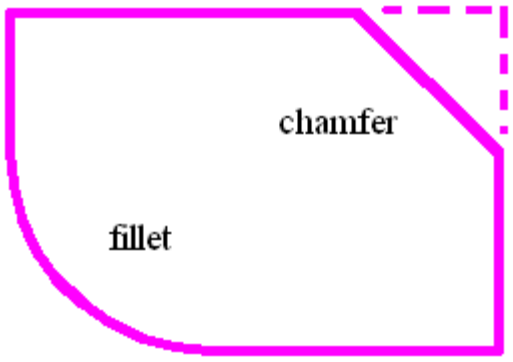
Measuring skills:



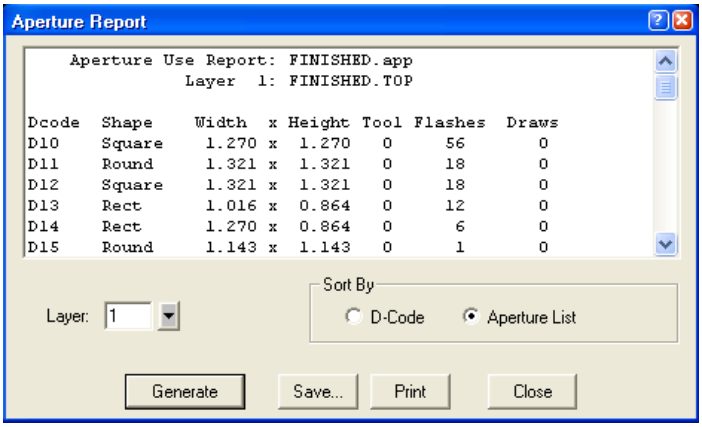
48. Select Point to point function from Query→measure then measure the dimension of the board (…….mm x……..mm).
49. Notes the diagonal filled circles at the upper corner in the design board.
50. From the functions edge to edge and center to center determine the diameter of each one (note the two circles have identical diameter). (φ= ……..).

Drawing Skills:

51. Draw a simplified logo for NTI (depicted at the lower left of this page) by using the drawing tools from **Add** pull down menu.
52. Use Edit menu to polish your logo. Some times you need to use purge command (Edit→purge) Purging destroys any undo information that currently exists. (Memory may become fragmented and less efficient. Therefore, occasional purging may help GerbTool perform optimally). Do not use this command unless you are sure you don't need to undo any previous edits!
53. Use Edit→Join command to join two line segments together using several different methods (on the right side draw a shape like the next one).



Editing Aperture file:

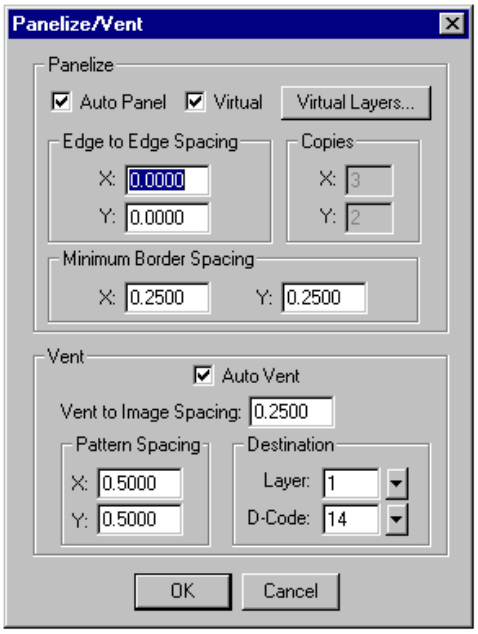


54. Use Aperture→ report command. Select layer one (1) then click generate. All D-codes in layer one will appear.
55. Note all D-codes have the same tool (0).
56. Sort the D-codes in three categories ($\varphi < 2$, $2<\varphi<3$,$\varphi>3$). Write the corresponding numbers.
    $\varphi < 2$:…….. .
    ……..
    $2<\varphi<3$:……..
    ……..
    $\varphi>3$:……..
    ……..
57. Use Aperture→ Edit command. Define tool 0 for first category and tool 1 for second and tool 2 for last ones.
58. Repeat step 29, note the tool numbers.
59. Repeat the last step with layer four then determine the D code of the circles defined in step 25.

Panelizing:

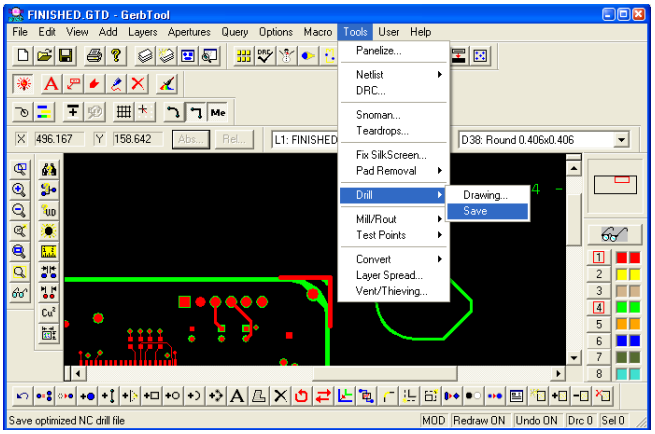
The Panelize command creates multiple copies of a design. This allows multiple copies of the design to be manufactured as one panel.

Automatic Penalization: To perform automatic penalization, follow these steps:Activate those layers you want to include in the panelization.

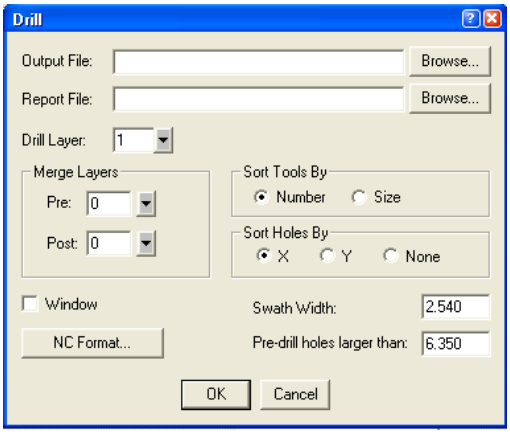


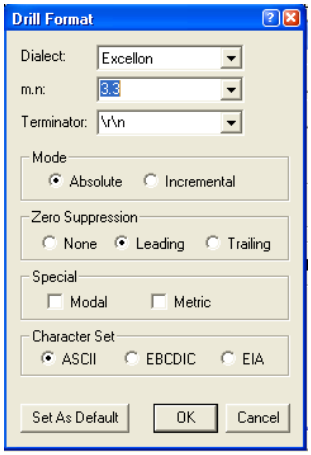
60. Select the Panelize command from the Tools menu. GerbTool displays the Panelize editing dialog box.
61. Select the Auto Panel button.
62. Enter the Edge to Edge (25mm) value.
63. Choose the OK button. GerbTool automatically calculates the maximum number of images that fit inside the current film box, then previews the panel layout. After asking for confirmation, GerbTool completes the panelization process. Depending on the setting of the Virtual button, GerbTool either copies the proper number images into the database or notes the number of copies and their location for display purposes.

Generate Drill File:



64. As above figure use save command to invoke drill dialog.

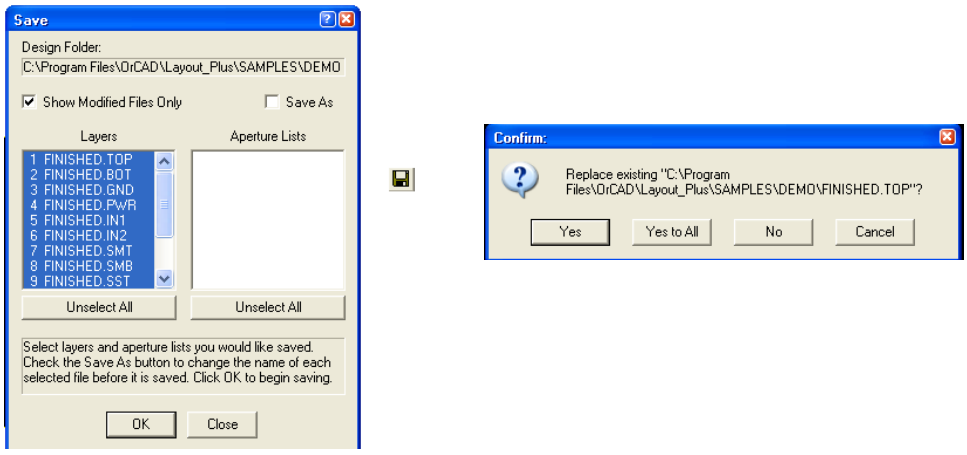




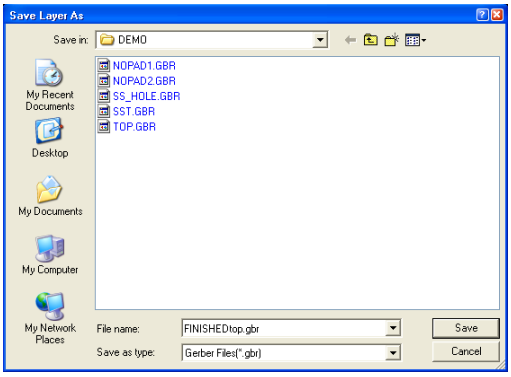
65. Type output file name (do not forget file extension recall step #11).
66. Click NC format button. Be sure m,n factor is 3,4 this means the gerbtool will accept the curved corners (fillet). Click OK for drill format and Drill dialog.
67. Create another drill file. Select sort holes by (y). Discuss the difference between two options relative to the processing driller time.

.....
.....
.....
.....

Files Saving:



68. From File→Save command the above dialog will appear.
69. Click OK.
70. Select No in the confirm dialog.
71. Type top as a suffix for file name with extension gbr In Save layer As dialog (see next figure). Click OK.
72. Repeat the last step for routing layers and solder mask layers.
73. Evoke your instructor to confirm your work. (Do not close your session).

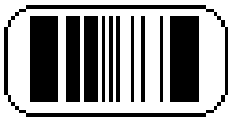


1-10-12. Quiz model A: Gerber Format and GerbTool:

1. Invoke Layout Plus.
2. From windows explorer Delete all files in the path
   C:\Program Files\OrCAD\Layout_Plus\SAMPLES\DEMOC
   Except DemoC2.max and DemoC3.max
3. Open the max file DemoC3.max. A warning massage will be displayed, select no button.
4. Edit the output file setting as:
   - Parameter Gerber format.
   - Do not generate drill files.
   - Top layer will be generated as rotated 90°.
   - Generate Gerber files for routing layers which are

   *,…….. Titled as ……
   *,…….. Titled as ……
   *,…….. Titled as ……
   *,…….. Titled as ……
   Besides *.ast layer which titled as ……...
   - Total number of layers is …….
5. Edit the Gerber setting as 3.4 format. Why the gerber creation is deactivated ……..
6. Generate Design Gerber file.
7. Invoke Gerbtool.
8. Edit the file size to be 30 cm x 30cm.
9. The back ground must be in black color.
10. Name each layer.
11. Panelize the design to generate 3 copies only.
12. Generate a Drill file.
13. Define three tools for drilling (t1 for D-code less than 1 mm t0 for all other D-codes).
14. Add a version bar code number on the top layer as above figure.
15. Save all layers. State the saved file names.

    Layer 1:……..
    Layer 1:……..
    Layer 1:……..
    Layer 1:……..
    Layer 1:……..



1-10-13. Quiz model B: Gerber Format and GerbTool:

1. Invoke Layout Plus.
2. Open the max file Board1.max. in the path
   C:\Program Files\OrCAD\Layout_Plus\SAMPLES\DEMOSR
3. Route the board.
4. Edit the output file setting as:
   - Standard Gerber format.
   - Do not generate drill files.
   - Generate Gerber files for routing layers which are
   *,…….. Titled as ……
   *,…….. Titled as ……
   *,…….. Titled as ……
   *,…….. Titled as ……
   Besides *.ast layer which titled as ……...
   - Total number of layers is …….
5. Edit the Gerber setting as 3.4 format. Why the gerber creation generates an aperture file list ……..
   State the name of generated file with extension …….
6. Generate Design Gerber file.
7. Invoke Gerbtool.
8. Edit the file size to be 30 cm x 30cm.
9. The back ground must be in black color.
10. Name each layer.
11. Panelize the design to generate 3 copies only.
12. Generate a Drill file.
13. Add a pyramids emblem on the top layer as above figure.
14. Save all layers. State the saved file names.

Layer 1:……..
Layer 1:……..
Layer 1:……..
Layer 1:……..
Layer 1:……..

1-10-14. Quiz model A: PCB Fabrication:

1. **Fill the blank spaces.**

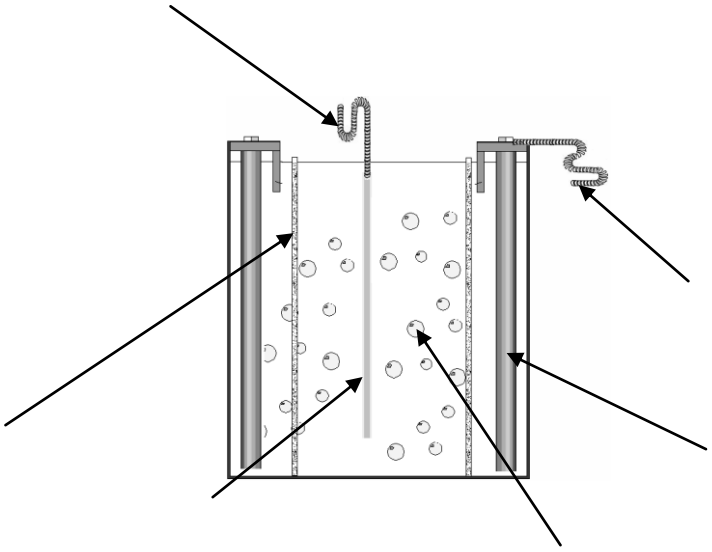
   The PCB Fabrication steps are:

   A. Brushing step by which ……
   B. Drilling step done by …… machine. On the other hand the isolation process done only by ……
   C. Through hole plating (DMT) step plates copper layers by two methods (…… and ……) the first method provides …… um thickness of copper while the other step enhances the thickness of copper to be ……um.
   D. Ceramic filter in galvanic metallization step filters ……. To provide ……. Distribution this filtration depends on ……..
   E. The photoplotter is a high resolution printer. It achieves this highest quality by using ……It can produce both types of films …….. And ……
   F. Laminator machine applies …… on PCB.

2. **Contrast between isolation and etching methods in PCB fabrication.**

……..
……..

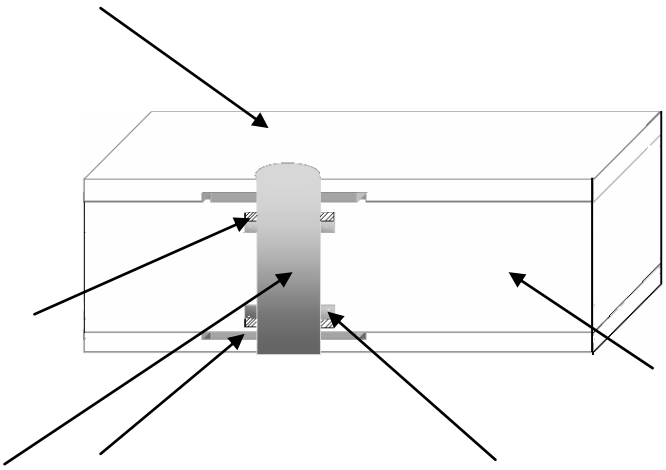
3. **Define each part in the next picture.**



1-10-15. Quiz model B: PCB Fabrication:

1. Fill the blank spaces.
   The PCB Fabrication steps are:
   A. Brushing step.
   B. Developing step eliminates ……while stripping step eliminates …….
   C. Through hole plating (DMT) step plates conductive layer on …….. by using noble metals like ……...
   D. The advantage of micro-etching in DMT step is ……
   E. Laminator machine applies green masks on PCB to …… ……
2. Define Drill smear problem.
……..
……..
3. State the disadvantages of DMT (*Direct metallization technology)*
……..
……..

1-10-16. Define each part in the next picture.



Quiz model C: Gerber Format and GerbTool:

Fill in the blanks with suitable words:

1. Gerber format is a standard format describing the images for …photo plotter… Machine.
2. Gerber format has two standards …274D…….. and …274x, mass parameter , extended gerber….
3. The difference between 2.3 format and 3.4 is 3.4 format support …true arc…. Graphics.
4. The extension of design file is …gtd…….. while drill file is …drl…..
5. CNC machine can …cut.. , …Isolate…. And ……drill…..PCB

Place (√) if the statement is correct and (x) if it wrong:

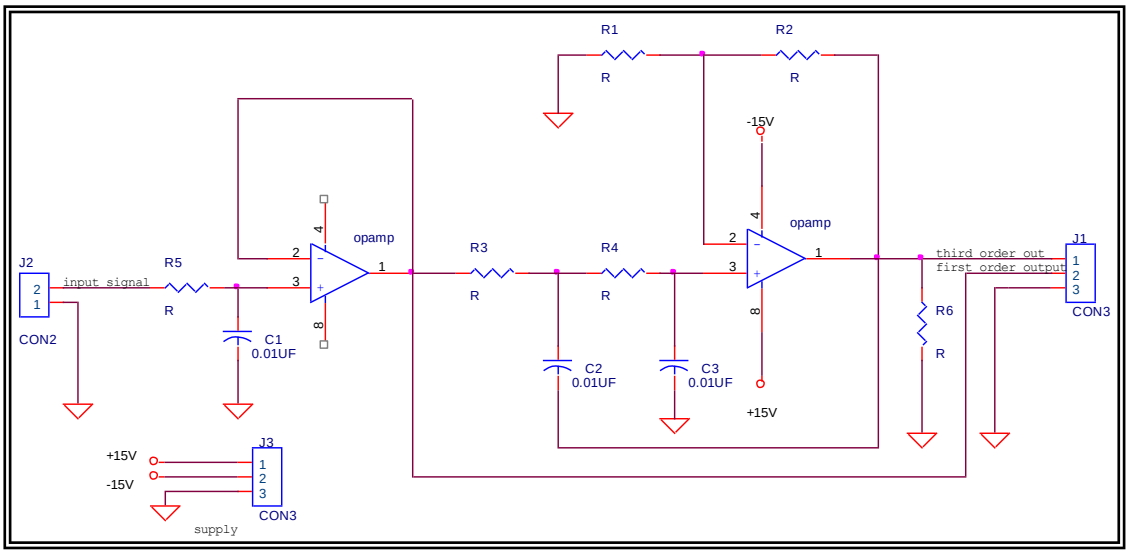
1. After UV exposure step, the developing step eliminates the photo sensitive material under laying the blind area in negative film. (√)
2. The striping step eliminates the photo sensitive material under laying the blind area in negative film. (x)
3. The laminator machine is designed to apply photosensitive materials on PCB (√)
4. The conventional process uses DMT to transfer the track from layer to another (x)
5. Drill Smear problem is occurred when the drilling bits melt the adhesive layer in multilayer PCB. (√)
6. To avoid the void problem in copper platting we use galvanic metallization step. (x)
7. Void problem is occurred when the copper molecules platted in irregular distribution form. (√)
8. copper plating step is done after etching process (x)

Answer the following questions:

1. Discuss the copper platting steps?
2. State the advantages and disadvantages of DMT(direct metallization technique)?
3. Describe the extra steps between multilayer and double layer PCB?

Case Study model A: second order filter:

FIRST: OrCAD Capture.



1- Create a new library (name it "my library") and create the part (opamp) shown in the above design
2- Create a new project (name it "active_filterMA") and draw the above design.
3- Modify the DRC settings to display a warning of unconnected pins.
4- Run DRC then state the warnings and errors in the design

5- Prepare the design for layout (generate netlist file) (……)

Second: Layout tool

6- Create a new layout file for the above design (the extension of layout file is ……..)
Using the following footprints

- -All resistances (TM-AXIAL: AX/400).
- -All capacitors (TM-CYLND: CYL/D250).
- -CON3 (SIP: SIP/TM/L300/3).
- -OPAMP (DIP100T:DIP100/8).
- -CON2 (SIP: SIP/TM/L200/2).

7-use the following physical settings:

- Single side board (routing on bottom layer)
- Track width 0.5 mm
- Global spacing 0.4mm
- All pad stack diameters (1.8 mm) except con2&3 (2.2mm)
- Resize the board to fit the components

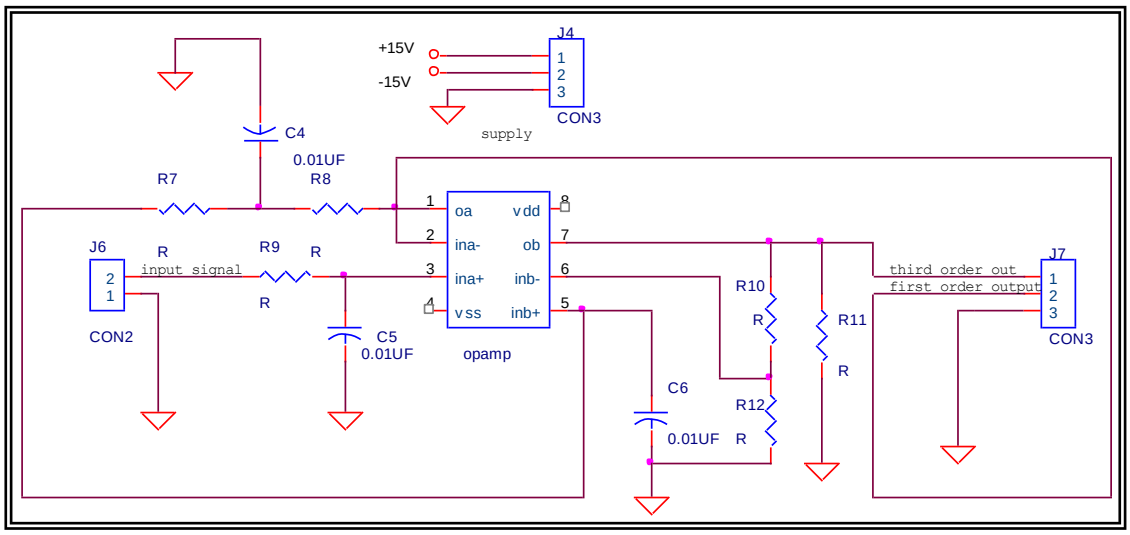
8- Auto route the board
9- Generate the GTD file

Third: Gerb tool

10- Add a text (active filter MA) on the Top layer inside a free space on the board
11- Create a drill file using T1 for (1.8mm) pad stacks and T2 for (2.2mm) pad stacks
12- Save the design and rename the routing and solder mask files with gbr extension

Case Study model B: Active filter:

FIRST: OrCAD Capture.



1- Create a new library (name it "my library") and create the part (opamp) shown in the above design

2- Create a new project (name it "active_filterMA") and draw the above design.

3- Modify the DRC settings to display a warning of unconnected pins.

4- Run DRC then state the warnings and errors in the design

5- Prepare the design for layout (generate netlist file) (……)

Second: Layout tool

6- Create a new layout file for the above design (the extension of layout file is ……..)

Using the following footprints

- -All resistances (TM-AXIAL: AX/400).
- -All capacitors (TM-CYLND: CYL/D250).
- -CON3 (SIP: SIP/TM/L300/3).
- -OPAMP (DIP100T:DIP100/8).
- -CON2 (SIP: SIP/TM/L200/2).

7-use the following physical settings:

- Single side board (routing on bottom layer)
- Track width 0.5 mm
- Global spacing 0.4mm
- All pad stack diameters (1.8 mm) except con2&3 (2.2mm)
- Resize the board to fit the components

8- Auto route the board

9- Generate the GTD file

Third: Gerb tool

10- Add a text (active filter MA) on the Top layer inside a free space on the board
11- Create a drill file using T1 for (1.8mm) pad stacks and T2 for (2.2mm) pad stacks
12- Save the design and rename the routing and solder mask files with gbr extension