

Memory Coding Style

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<http://Drshiple-courses.weebly.com/>

QUOTE OF THE DAY

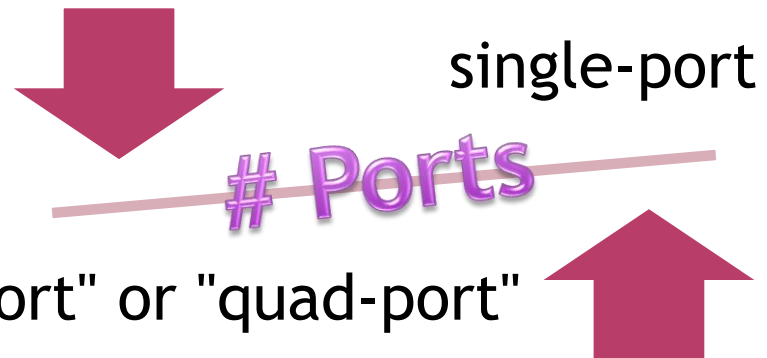
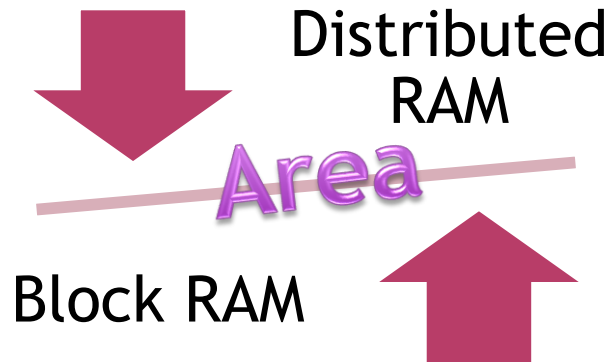
نتائج العمل الجماعي أفضل من
نتائج العمل الفردي. فيد الله مع
الجماعة

Coming together is a beginning.
Keeping together is progress.
Working together is success.

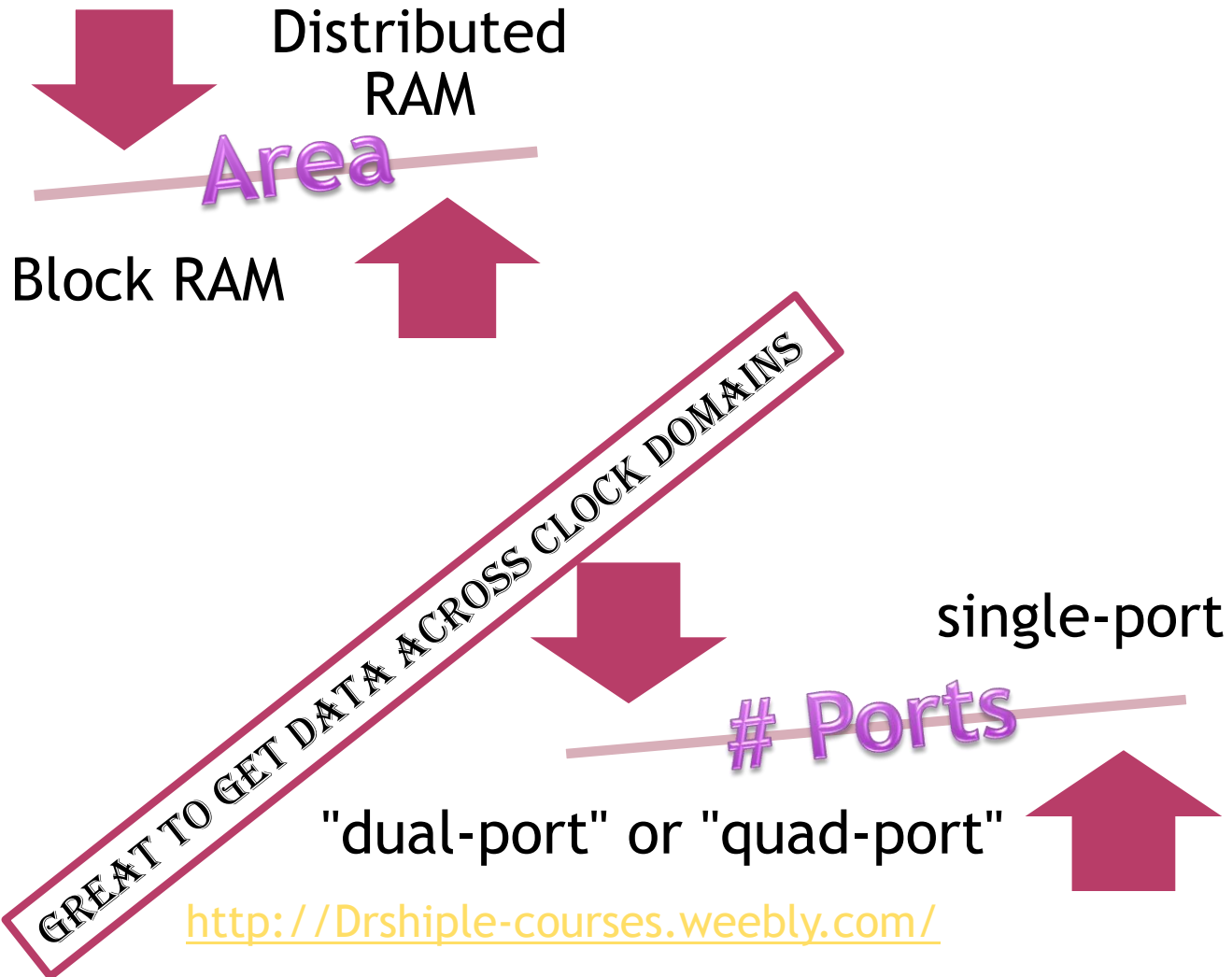
- Henry Ford

“Teachers call it copying..we call it teamwork!”

Memory Types



Memory Types



XILINX vs. ALTERA

Distributed RAM

Altera

- Smaller block-rams.
- Not flexible to use.
- efficient area.

Xilinx

- Very flexible RAM distribution
- Inefficient area

XILINX Distributed vs. Block

Distributed

- Extra wiring delays
- Synchronous write
- Asynchronous read

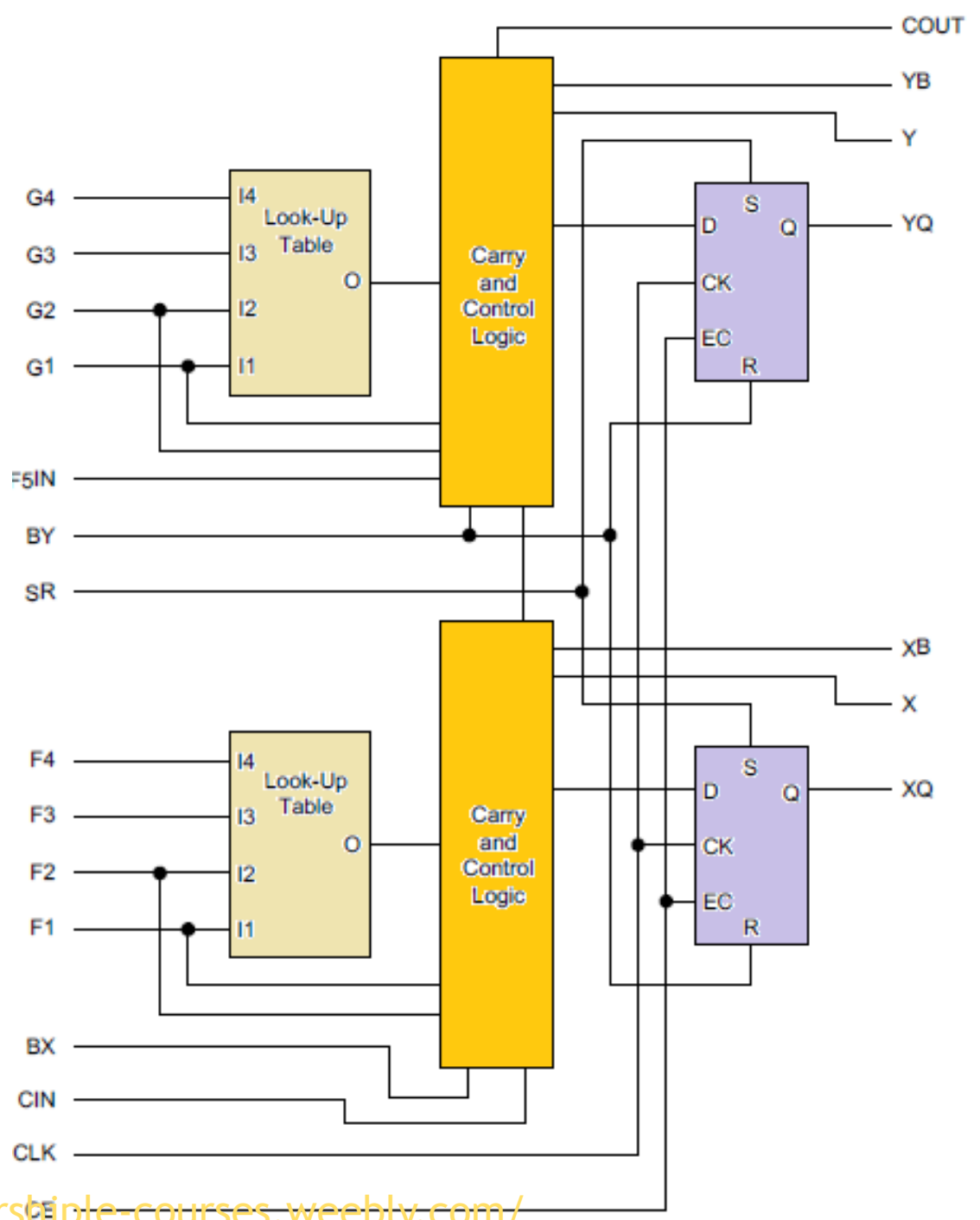


Block

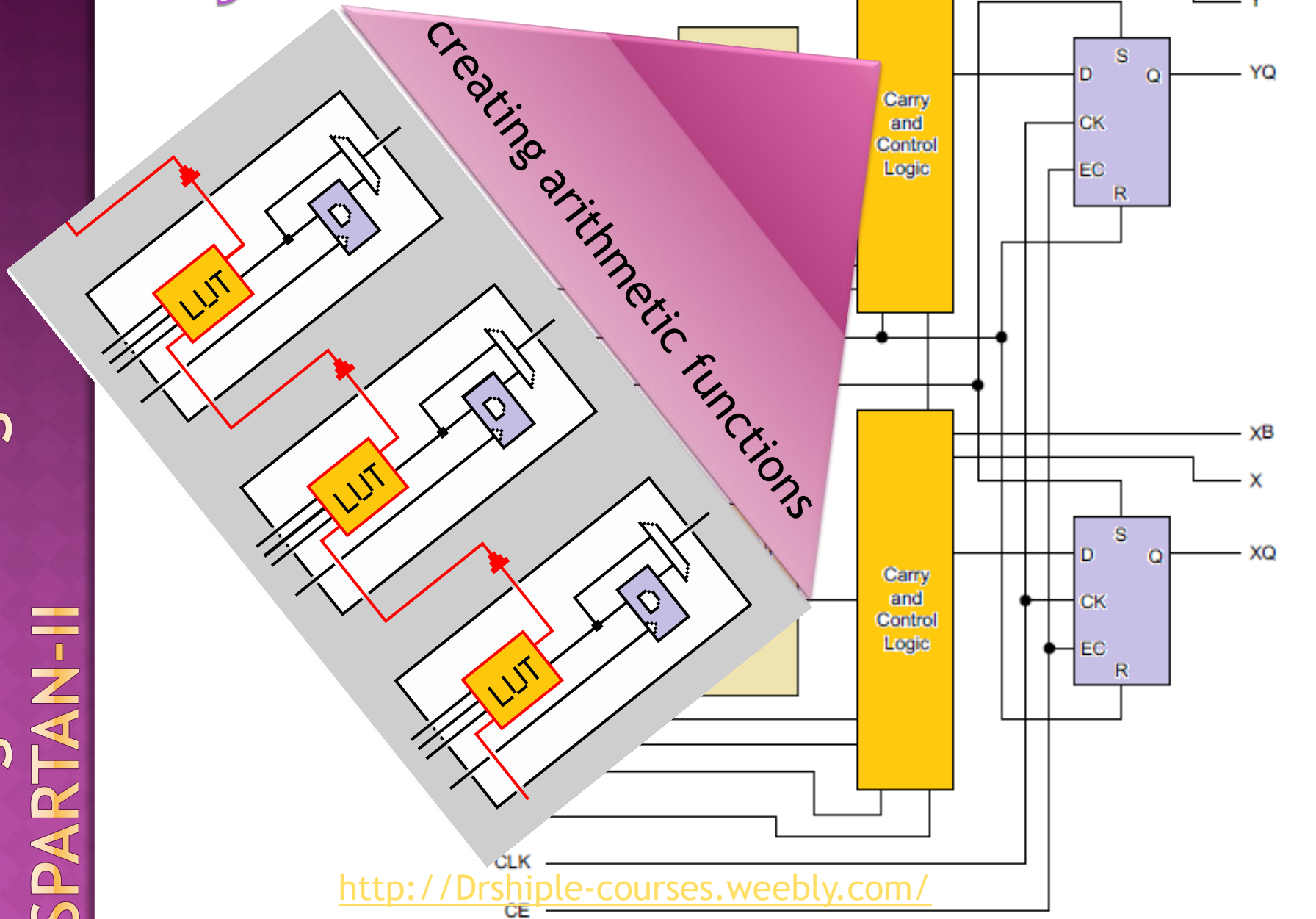
- Wastage of the rest of the space in RAM
- Synchronous write
- Synchronous read



Configurable Logic Block SPARTAN-II



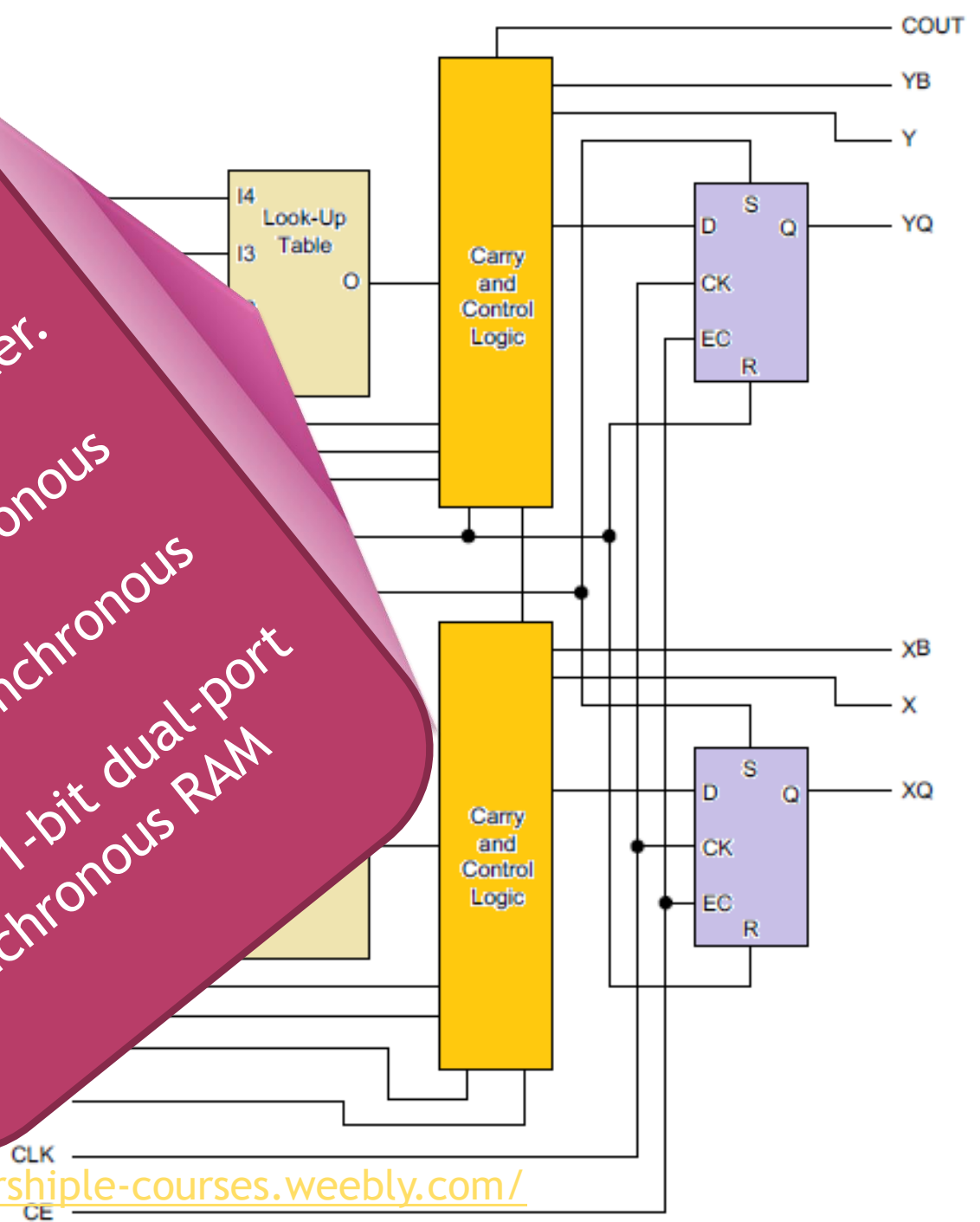
Carry Chain



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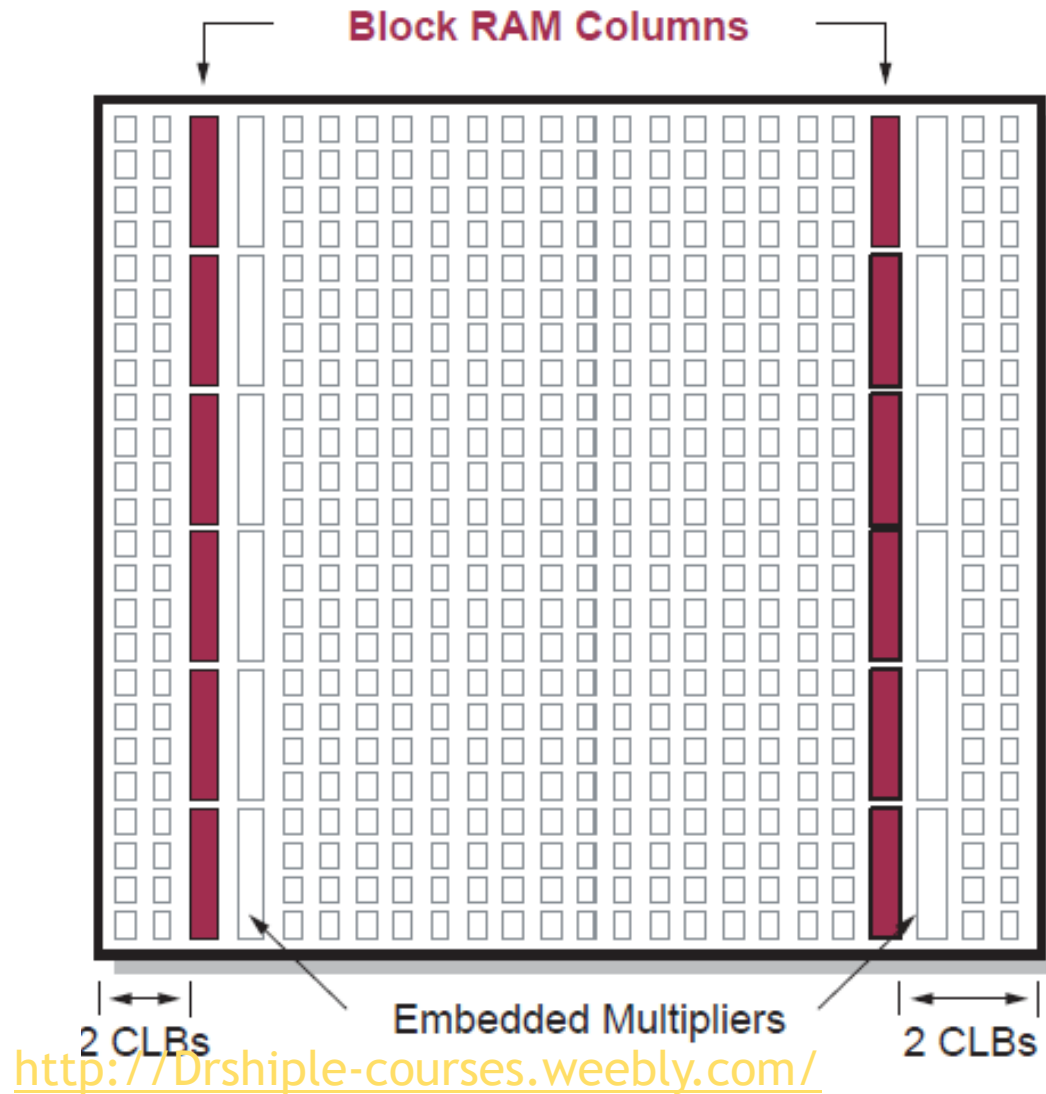
Look up Tables

- One LUT:
 - 16 x 1 synchronous RAM.
 - 16-bit shift register.
- Two LUT:
 - 16 x 2 synchronous RAM.
 - 32 x 1 synchronous RAM.
 - 16 x 1-bit dual-port synchronous RAM



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Block RAM

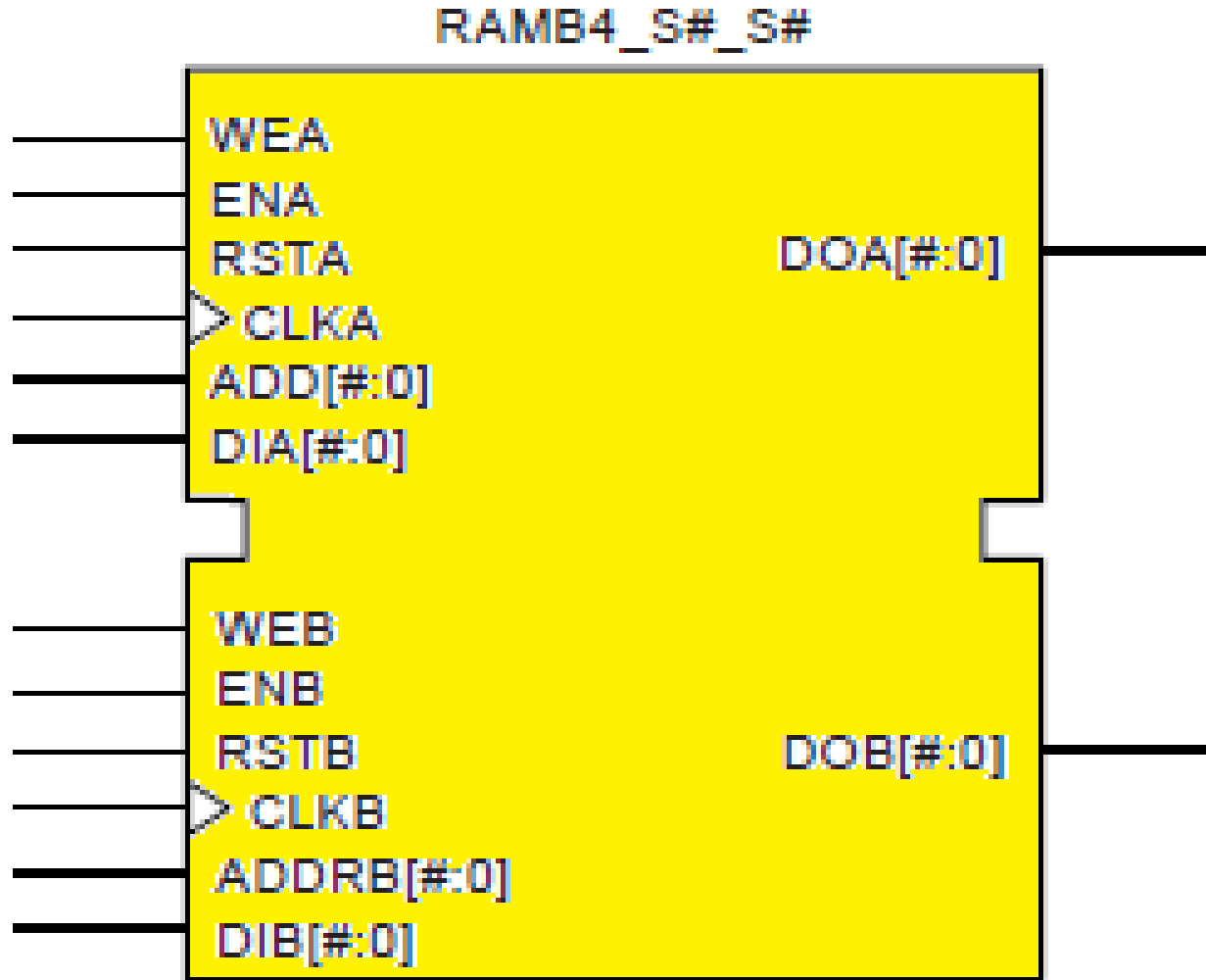


Block RAM

Spartan-II Block RAM Amounts

Spartan-II Device	# of Blocks	Total Block RAM Bits
XC2S50E	8	32K
XC2S100E	10	40K
XC2S150E	12	48K
XC2S200E	14	56K
XC2S300E	16	64K
XC2S400E	40	160K
XC2S600E	72	288K

Block RAM Cont.



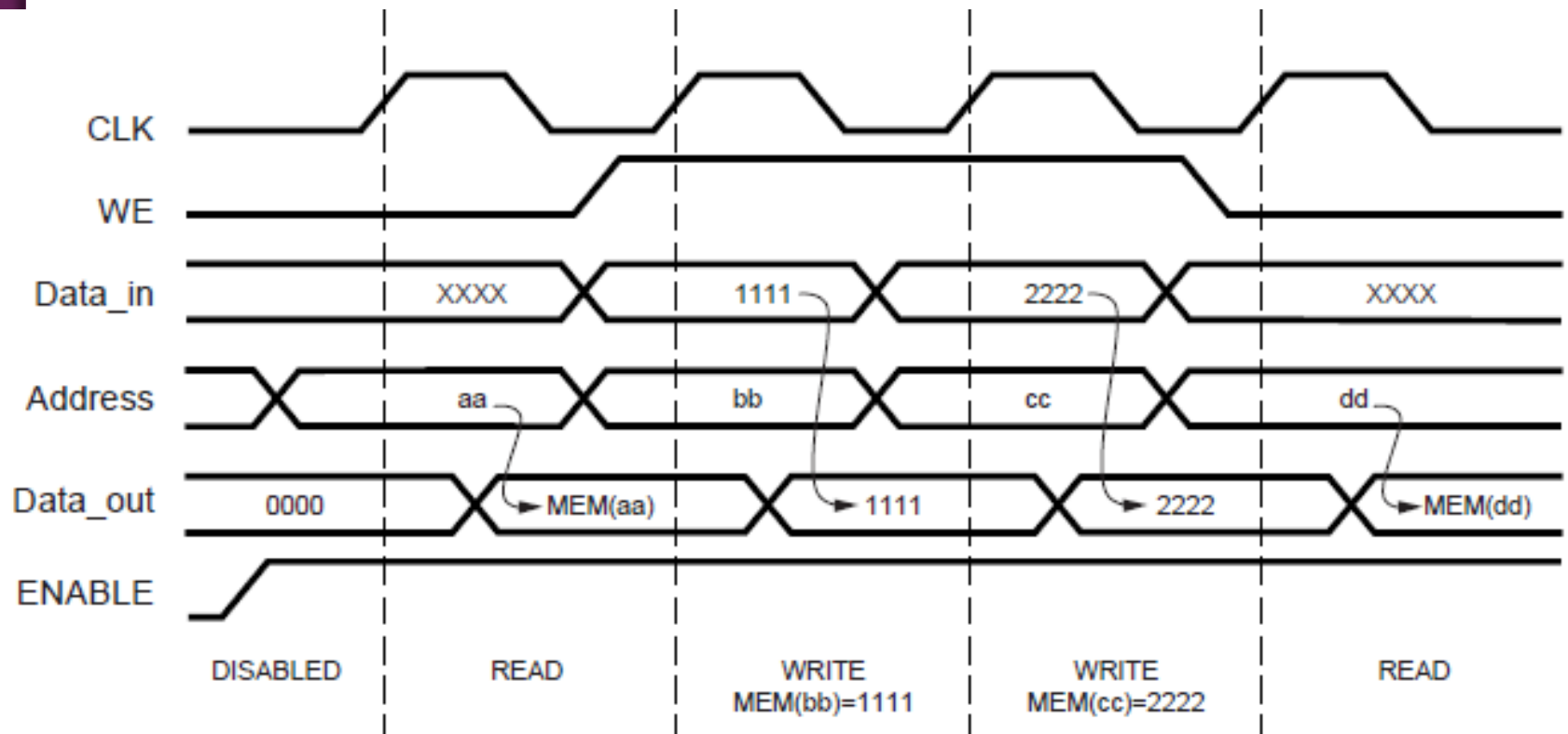
Dual-Port Block RAM

Block RAM Cont.

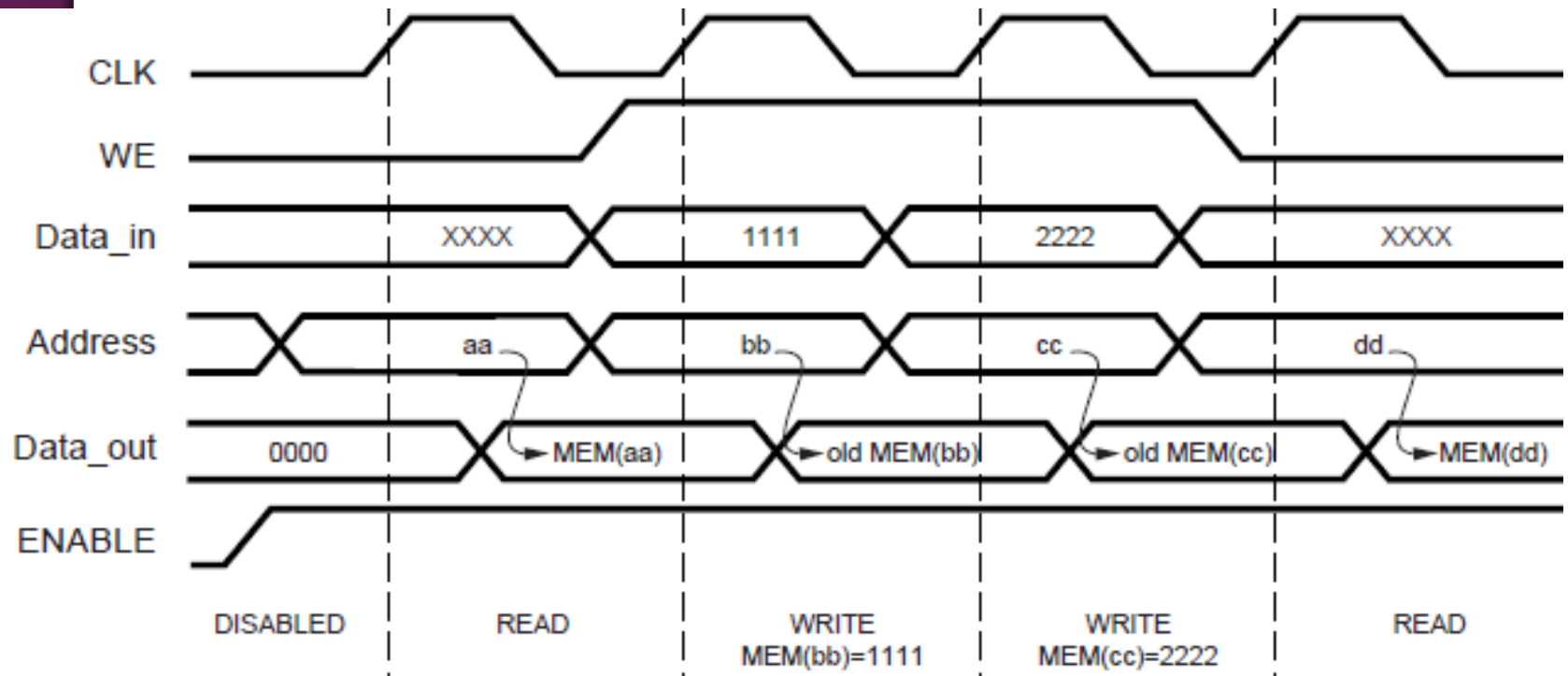
Block RAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

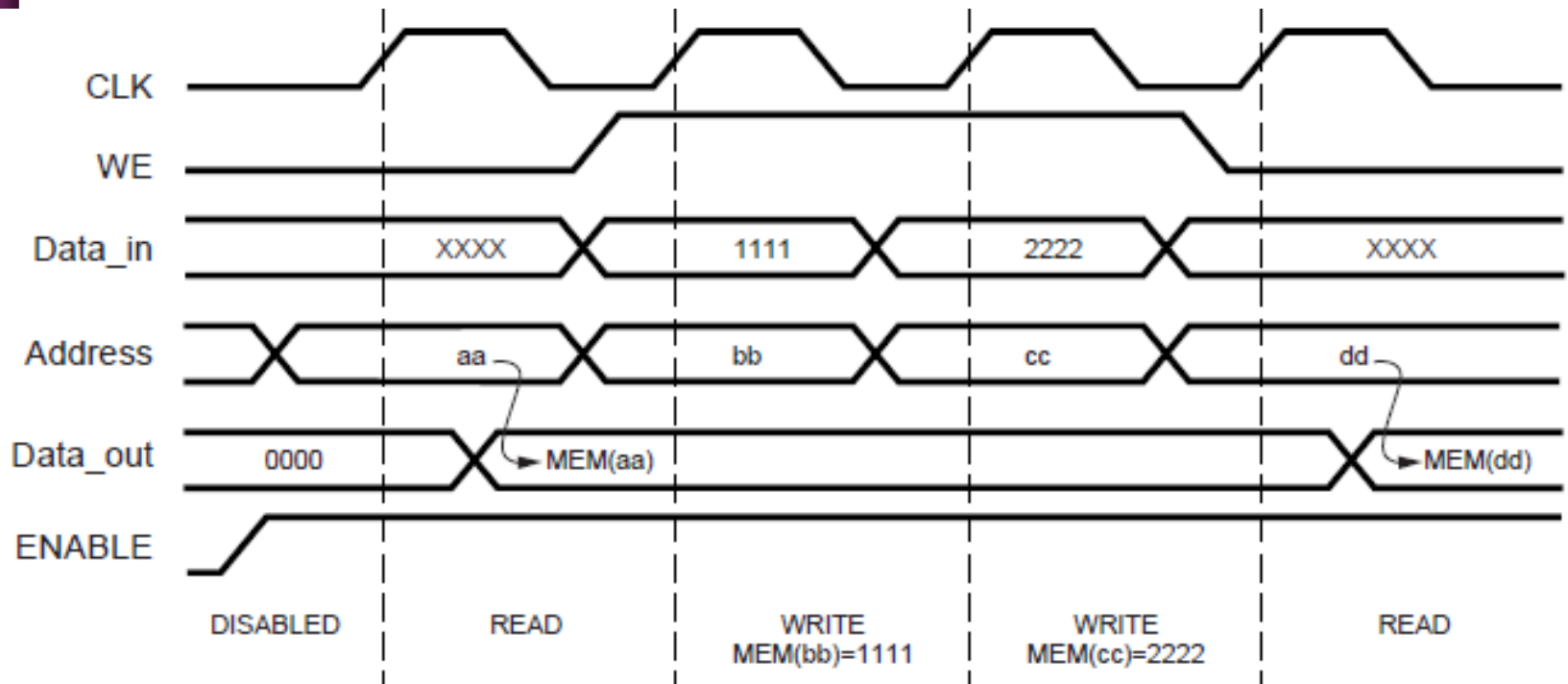
WRITE FIRST



READ FIRST



NO CHANGE



VHDL Code Style

The screenshot displays the ISE Project Navigator interface. The main window shows a project hierarchy for 'Pace ex' with a file named 'Shiple - Behavioral (Shiple.vh...)'. The 'Processes' pane shows a list of tasks including 'Synthesize - XST'. The 'Design' pane shows a tree structure of VHDL code, with annotations 1, 2, 3, and 4 pointing to specific elements: 1 points to the lightbulb icon in the toolbar, 2 points to the 'VHDL' folder, 3 points to the 'Coding Examples' folder, and 4 points to the 'RAM' folder. The 'RAM' folder contains sub-folders for 'BlockRAM' and 'Distributed RAM', each with several example code files.

ISE Project Navigator (M.53d) - F:\Proffisional course\ref2\labs\Pace_ex\Pace_ex.xise - [Language Templates]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- Pace ex
 - xc3s500e-5vq100
 - Shiple - Behavioral (Shiple.vh...)
 - ex2_if - Behavioral (ex2_if.vhd)
 - example1.ucf
 - ex3_case - Behavioral (ex3_ca...)
 - example1 - Behavioral (exam...)
 - mem_test - Behavioral (m...)
 - ex6_1 (ex6_1.sch)
 - XLXI_1 - parity - Behavior...

No Processes Running

Processes: mem_test - Behavioral

- Create Timing Constraints
- I/O Pin Planning (PlanAhea...)
- I/O Pin Planning (PlanAhea...)
- Floorplan Area/IO/Logic (Pl...)
- Synthesize - XST
- View RTL Schematic
- View Technology Schematic
- Check Syntax
- Generate Post-Synthesis Si...

VHDL

- Synthesis Constructs
- Coding Examples
- RAM
 - BlockRAM
 - Dual Port
 - 1 Clock, 1 Read/Write Port, 1 Read Port
 - 1 Clock, 1 Write Port, 1 Read Port
 - 2 Clocks, 1 Read/Write Port, 1 Read Port
 - 2 Clocks, 1 Write Port, 1 Read Port
 - 2 Clocks, 2 Read/Write Ports
 - Example Code
 - Info
 - RAM Type Declaration
 - Single Port
 - Using FILE I/O
 - Distributed RAM
 - Dual Port, Async Read
 - Example Code
 - Single Port, Async Read
 - ROM
 - Example Code
 - ROM Type Declaration
 - Using FILE I/O
 - Using Initialization Signal

ISE Design Suite InfoCenter Language Templates mem_test.vhd

1- DEFINE SIZE OF MEMORY

type <ram_type>

is

array (2**ADDR_WIDTH-1 downto 0)

of

std_logic_vector (DATA_WIDTH-1 downto 0);

signal RAM: <ram_type>;

2- DEFINE TYPE OF IMPLEMENTATION

```
attribute ram_style: string;  
attribute ram_style of ram : signal is "block";  
                        : signal is "distributed";
```

3- DEFINE LIBRARY

```
use IEEE.std_logic_unsigned.all;
```