Memory Coding Style

By: Mustafa Shiple

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QUOTE OF THE DAY

نتائج العمل الجماعي أفضل من نتائج العمل الفردي. فيد الله مع الجماعة

Coming together is a beginning.
Keeping together is progress.
Working together is success.

- Henry Ford

“Teachers call it copying..we call it teamwork!”

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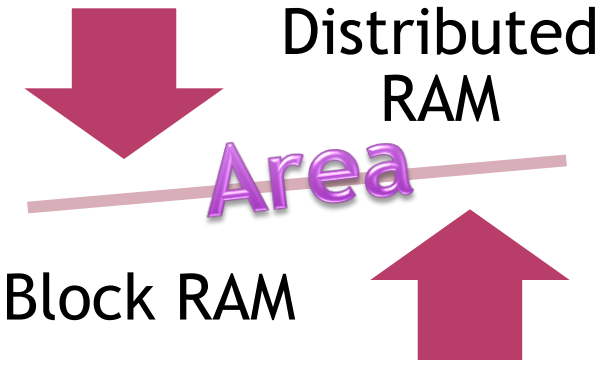
Memory Types



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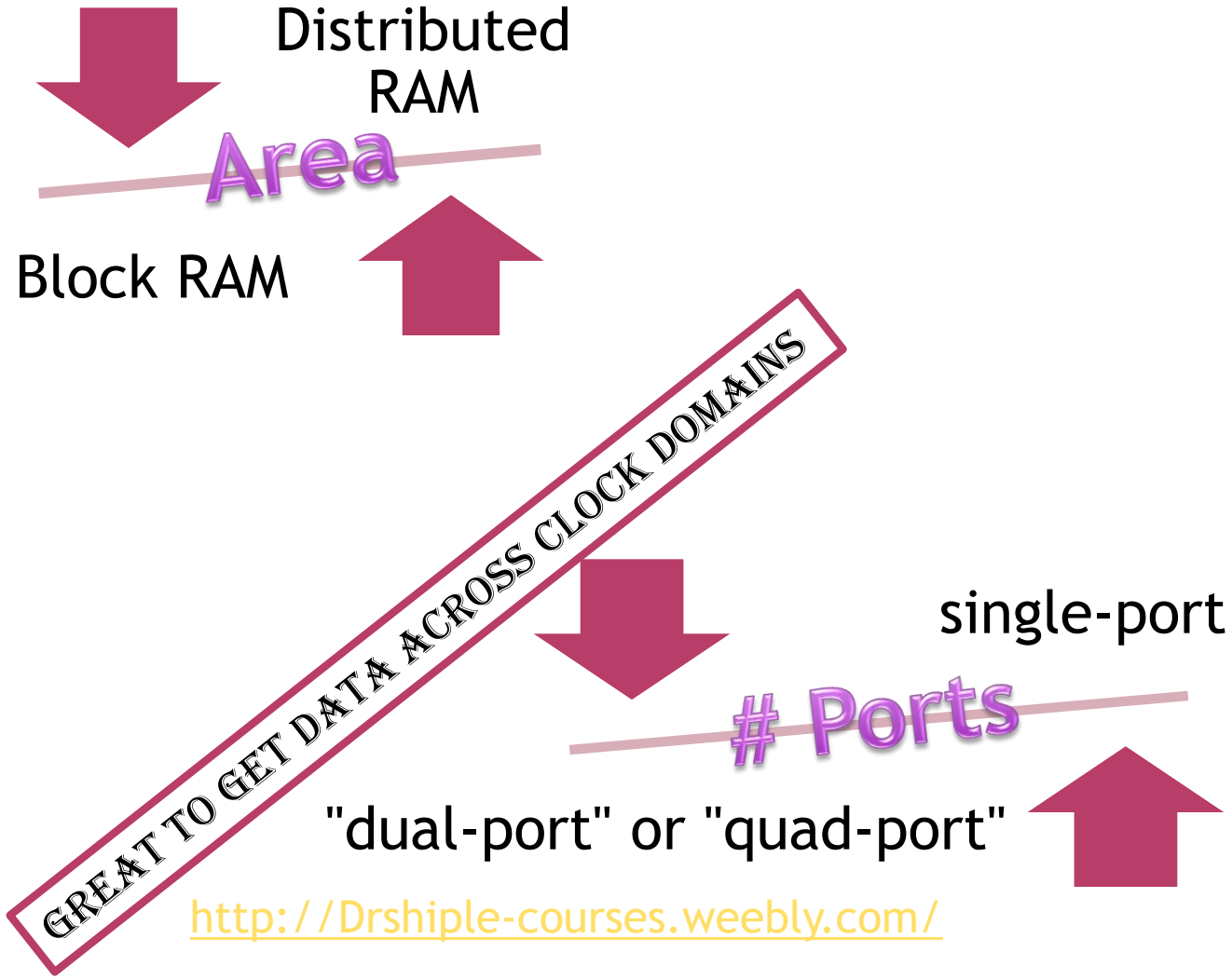
Memory Types



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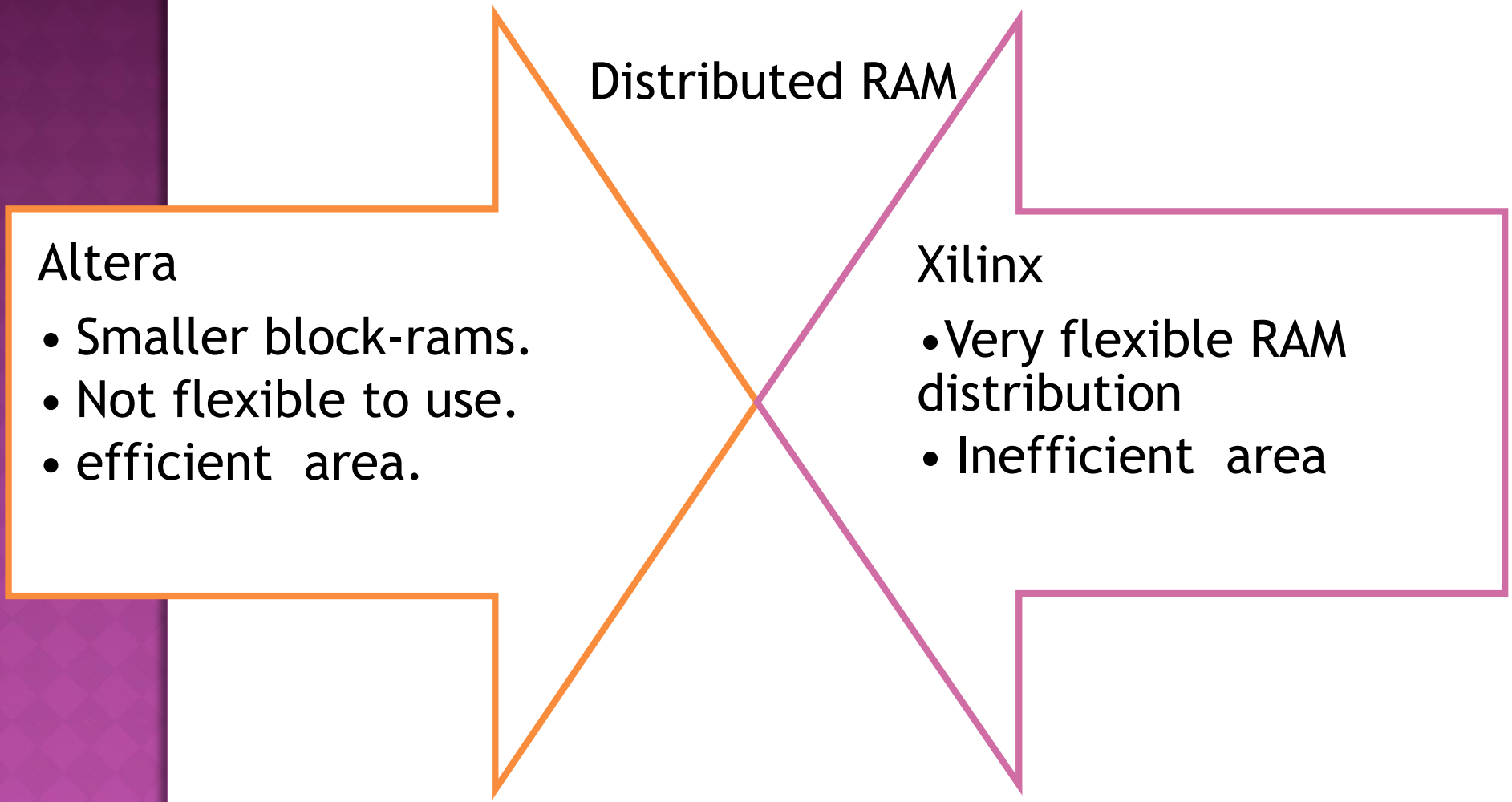
XILINX vs. ALTERA



XILINX Distributed vs. Block

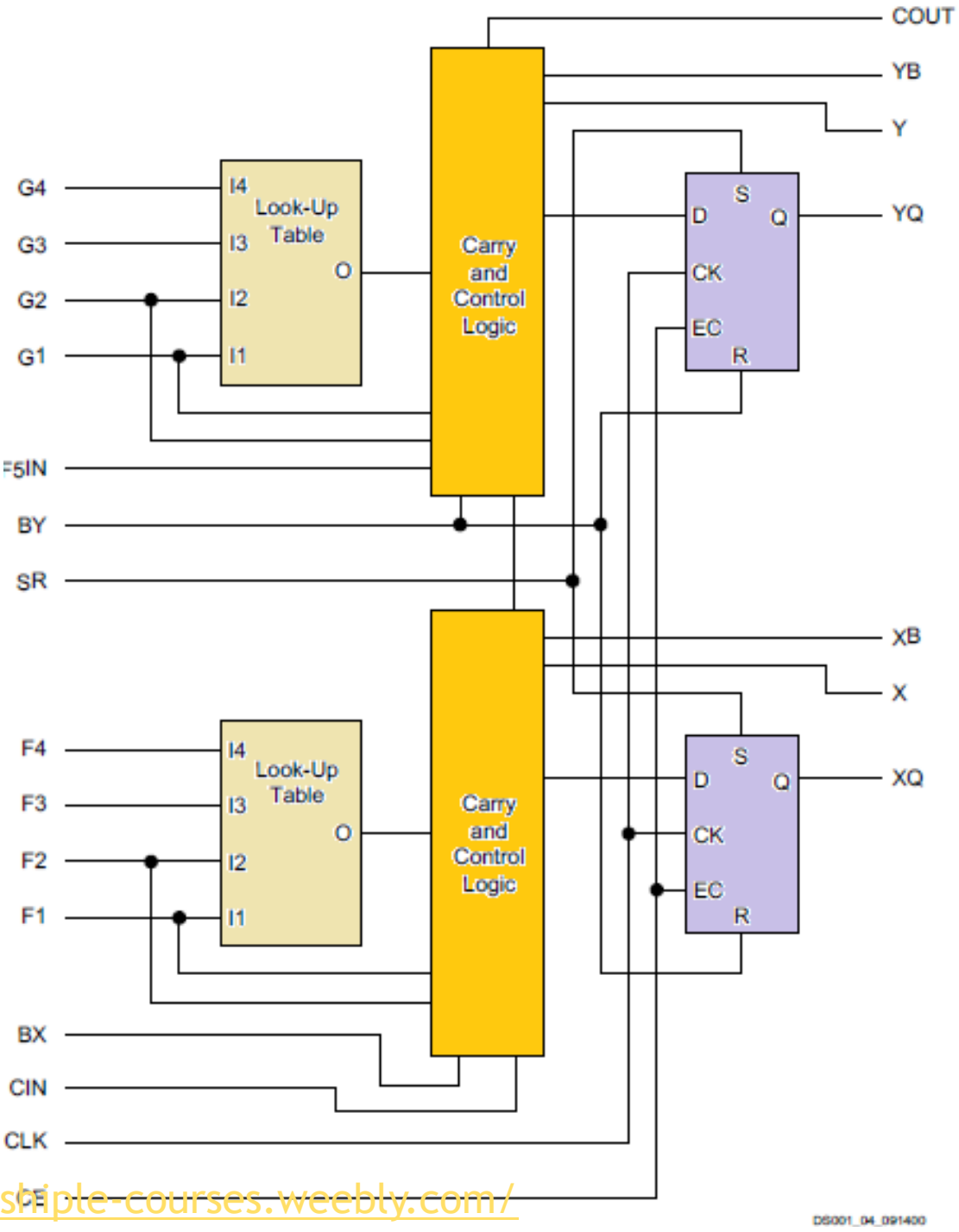
Distributed

- Extra wiring delays
- Synchronous write
- Asynchronous read

Block

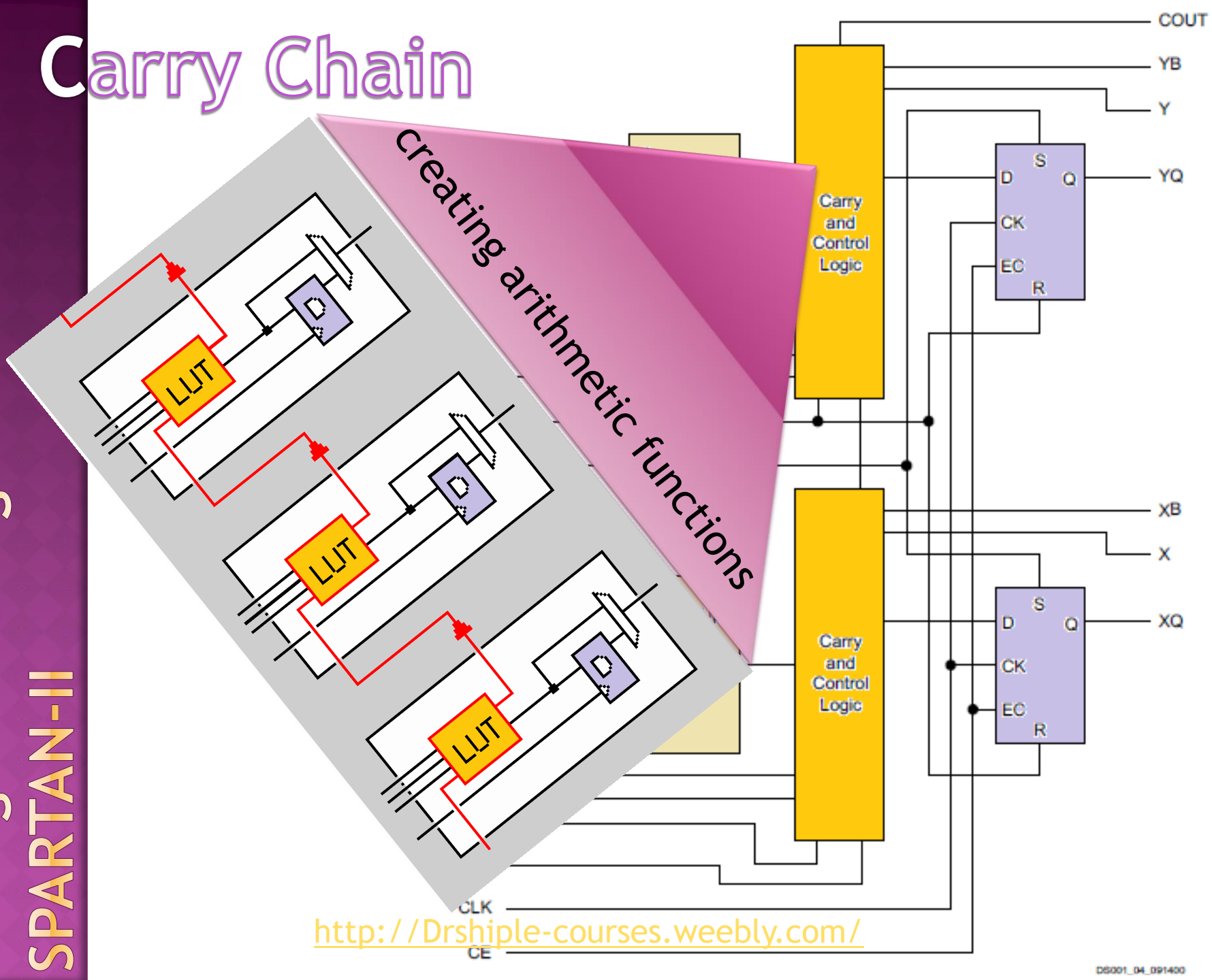
- Wastage of the rest of the space in RAM
- Synchronous write
- Synchronous read

Configurable Logic Block SPARTAN-II



Carry Chain

Configurable Logic Block
SPARTAN-II



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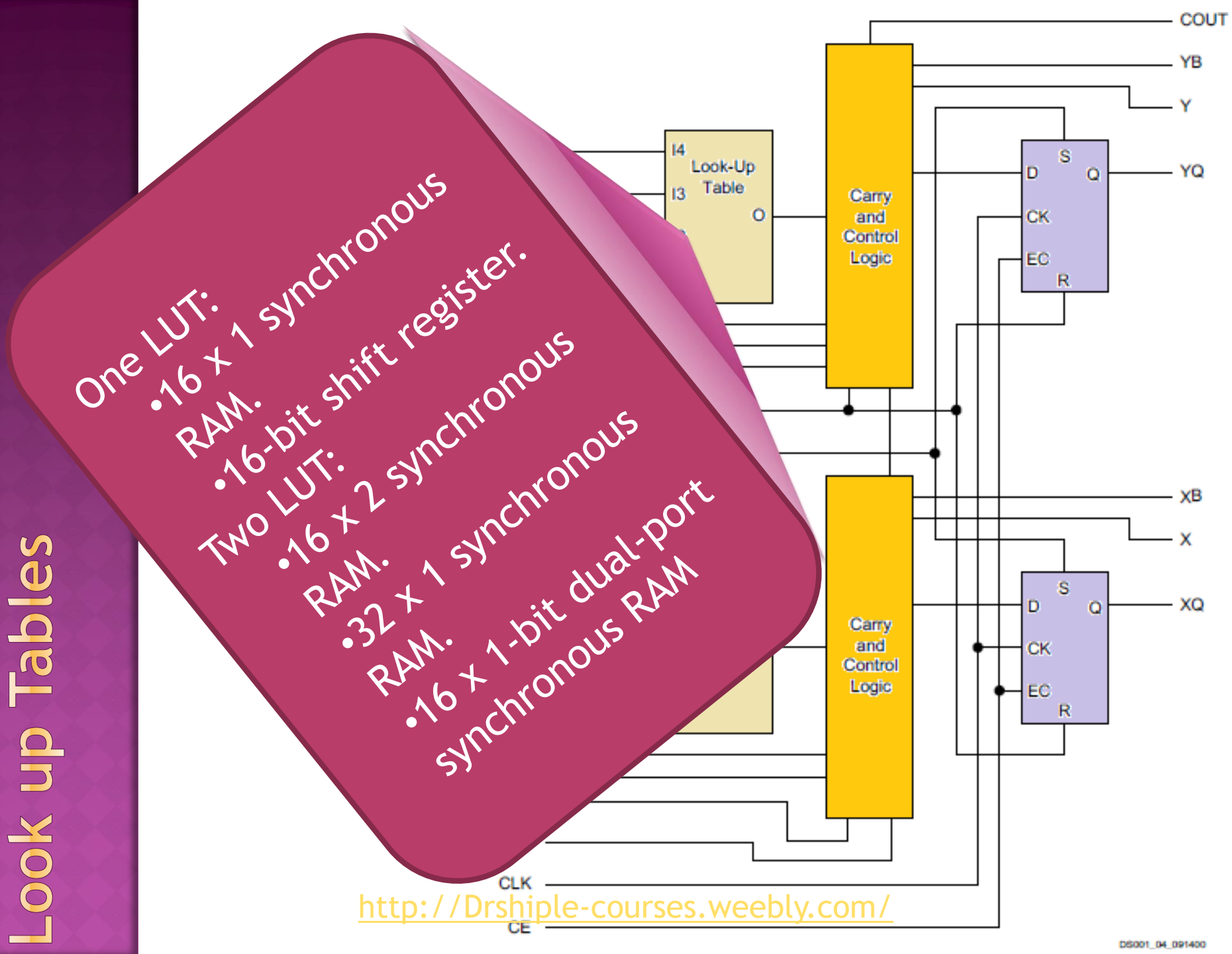
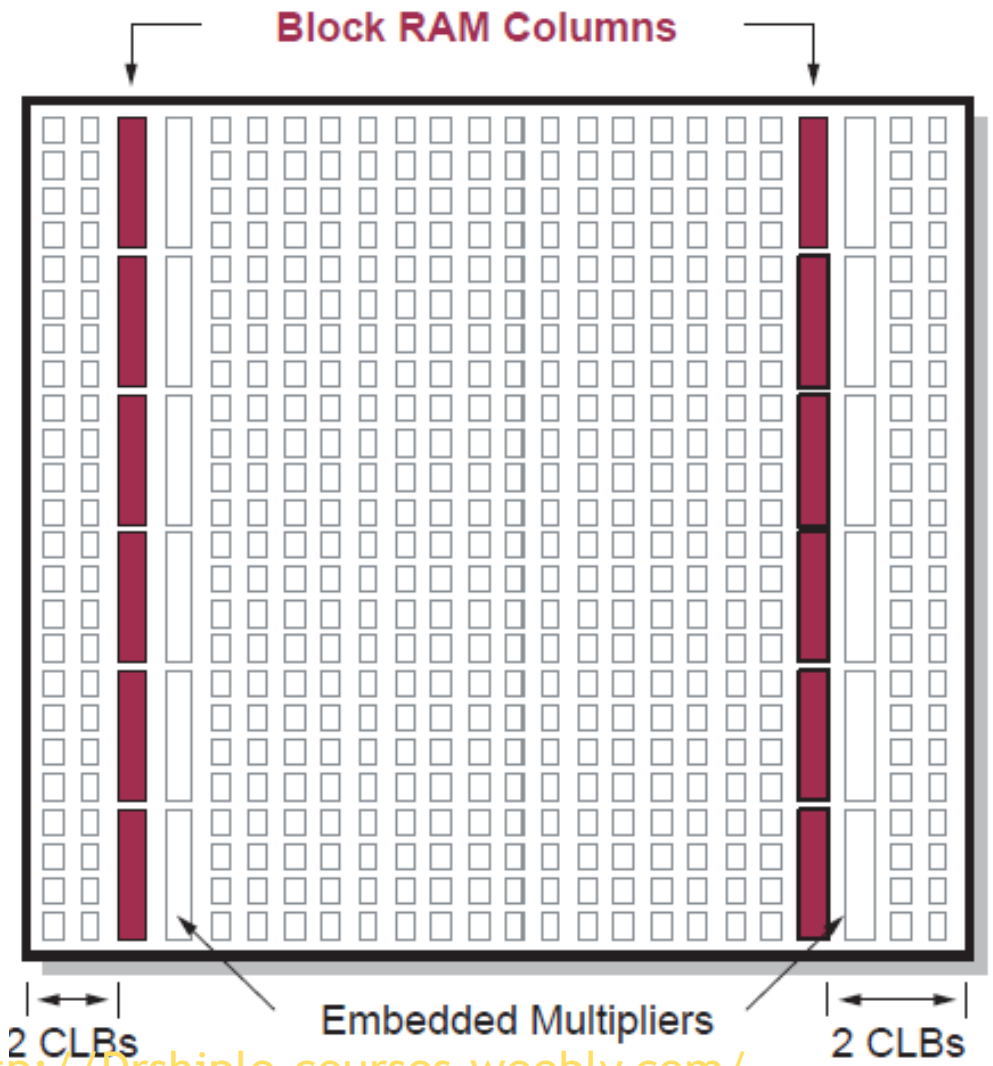
Look up Tables

One LUT:
- 16 x 1 synchronous RAM.
- 16-bit shift register.

Two LUT:
- 16 x 2 synchronous RAM.
- 32 x 1 synchronous RAM.
- 16 x 1-bit dual-port synchronous RAM



Block RAM

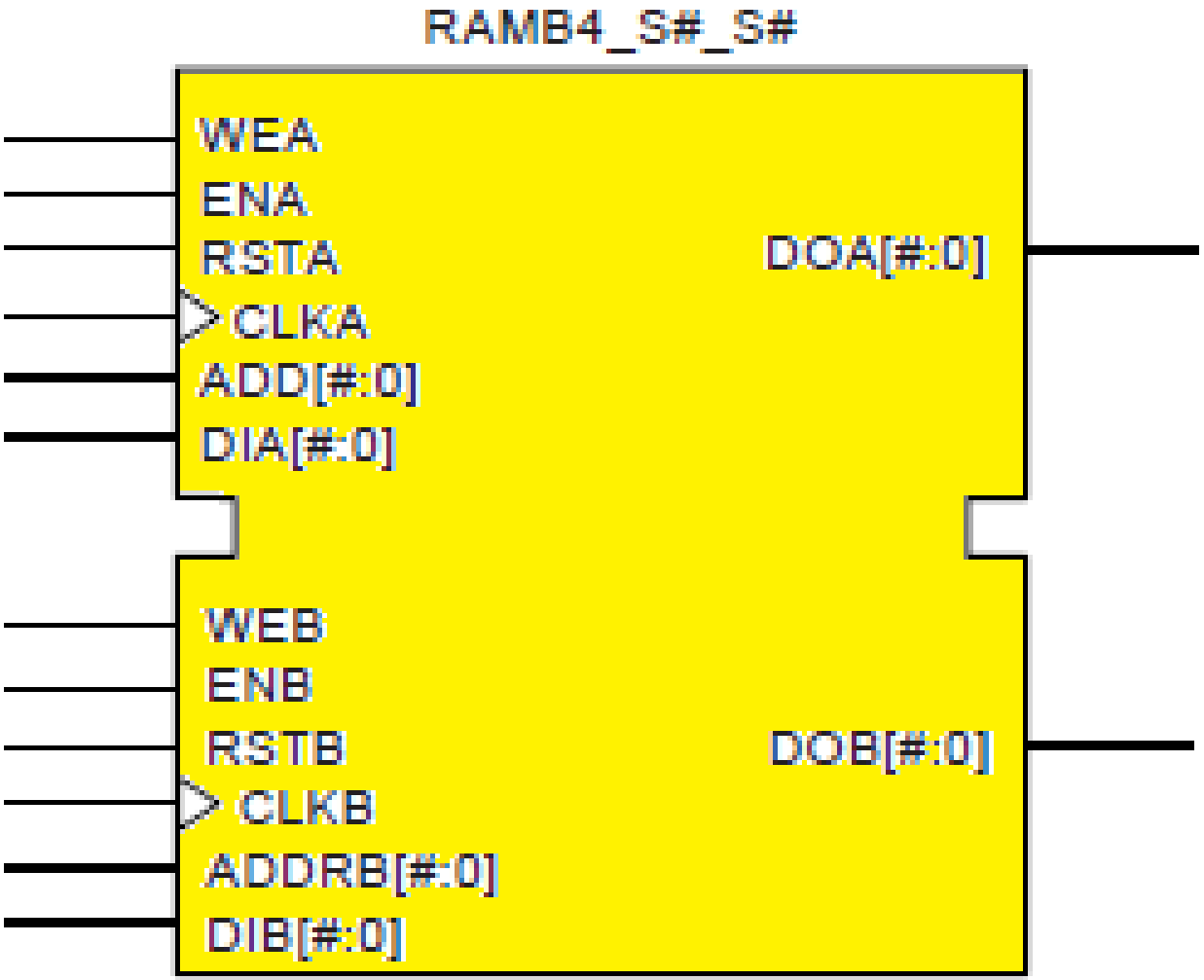


Block RAM

Spartan-IIE Block RAM Amounts

Spartan-IIE Device	# of Blocks	Total Block RAM Bits
XC2S50E	8	32K
XC2S100E	10	40K
XC2S150E	12	48K
XC2S200E	14	56K
XC2S300E	16	64K
XC2S400E	40	160K
XC2S600E	72	288K

Block RAM Cont.



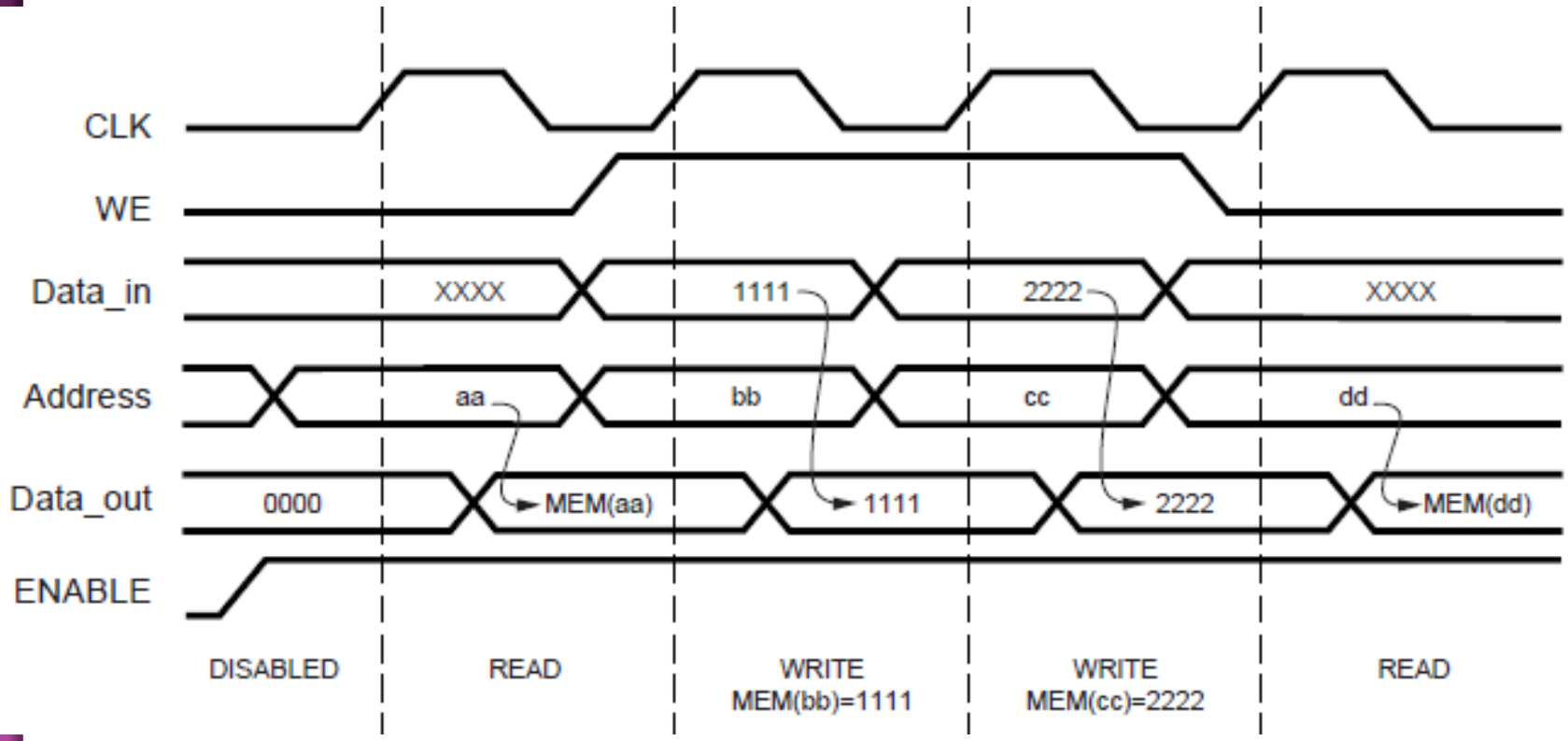
Dual-Port Block RAM

Block RAM Cont.

Block RAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

WRITE FIRST



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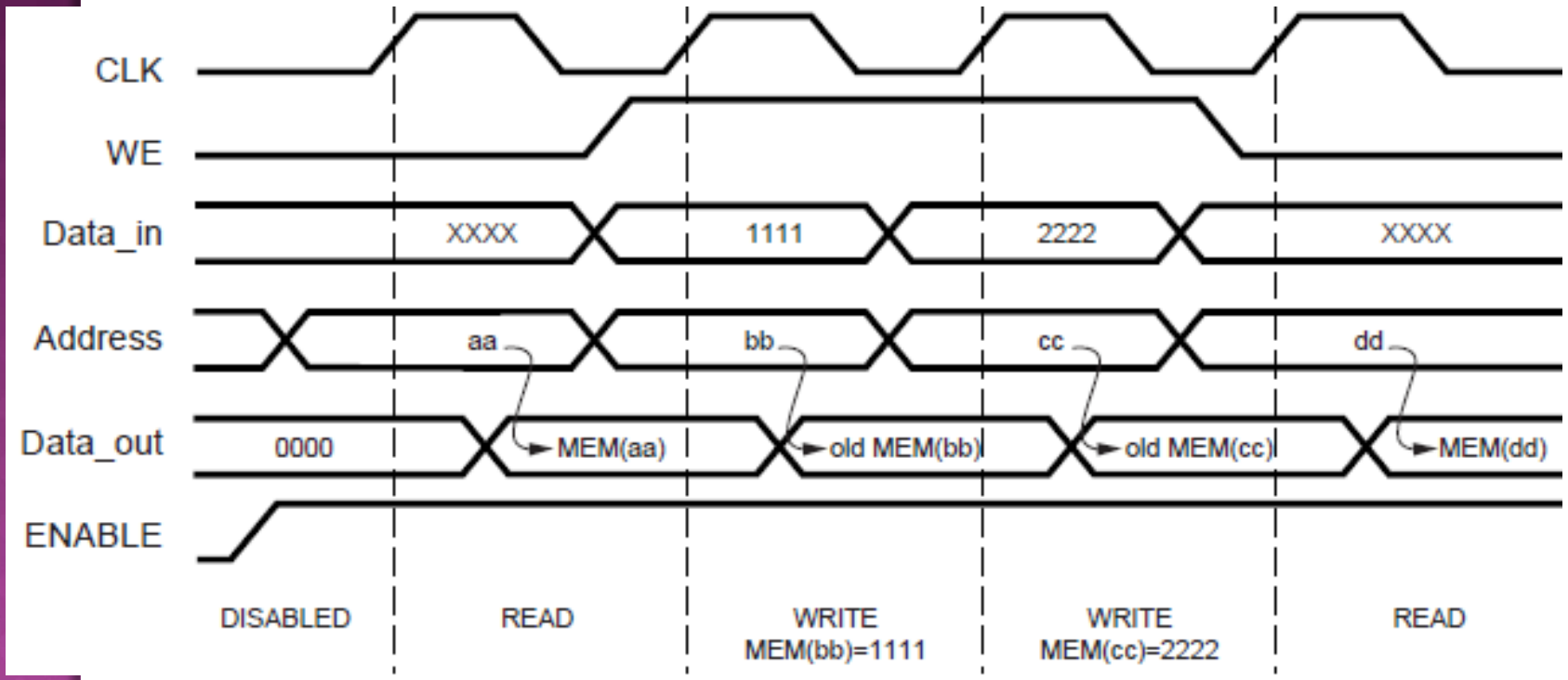
READ FIRST



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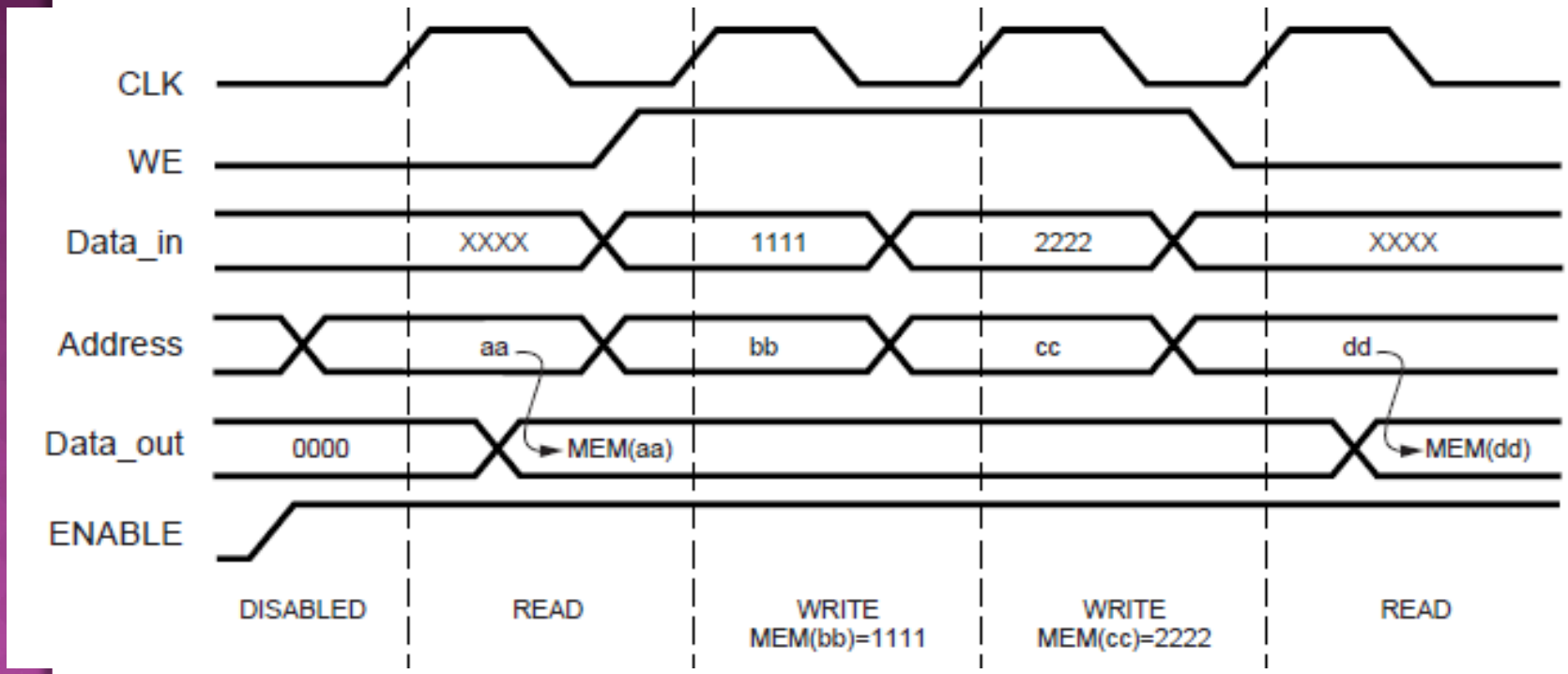
NO CHANGE



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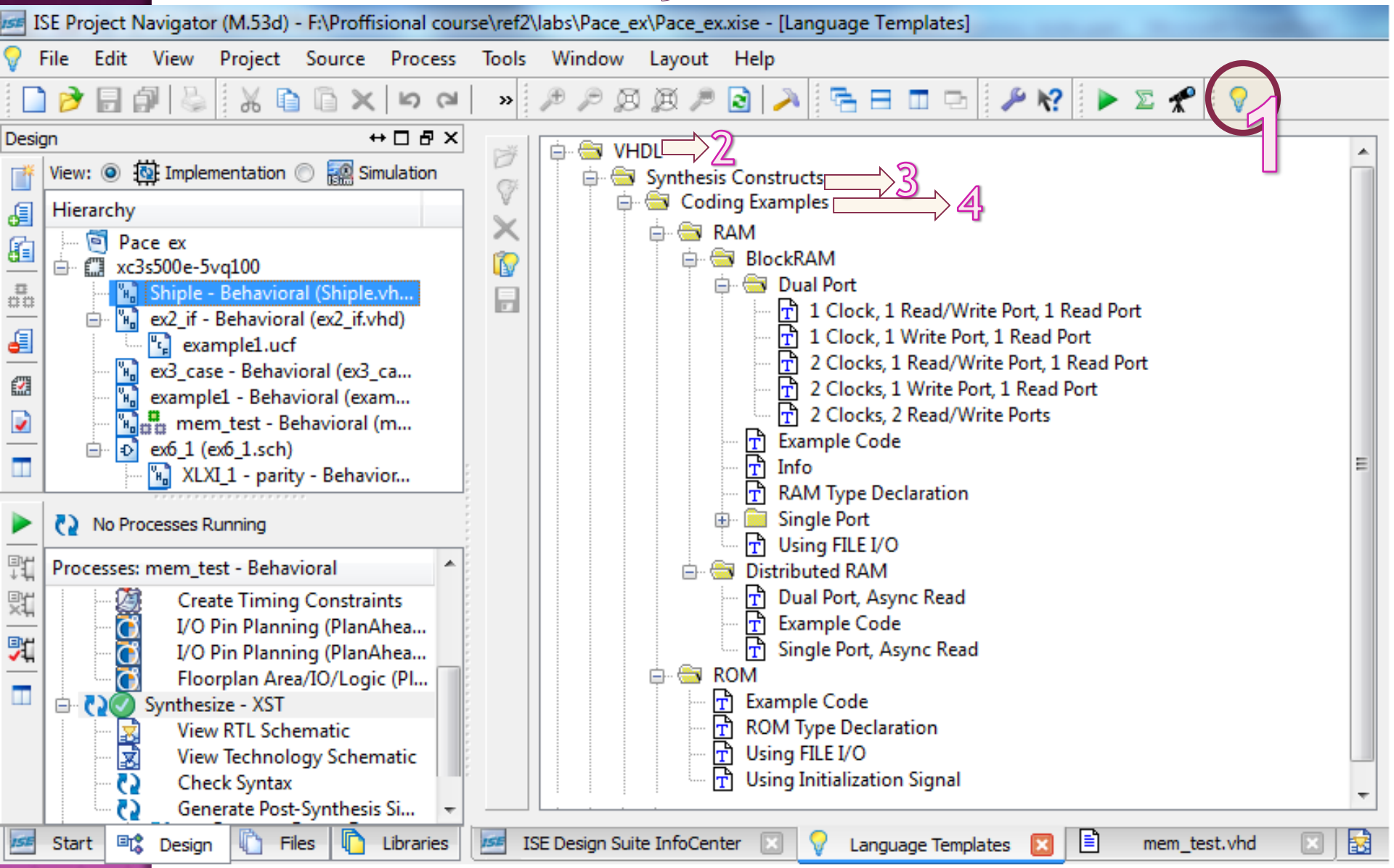
VHDL Code Style



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1- DEFINE SIZE OF MEMORY

```
type <ram_type>
   is
        array (2**ADDR_WIDTH-1 downto 0)
    of
        std_logic_vector (DATA_WIDTH-1 downto 0);
signal RAM: <ram_type>;
```

2- DEFINE TYPE OF IMPLEMENTATION

```
attribute ram_style: string;
attribute ram_style of ram  : signal is "block";
                            : signal is “distributed";
```

3- DEFINE LIBERARY

```
use IEEE.std_logic_unsigned.all;
```