# Introduction to Logic Array

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Advanced Microprocessor (EEC 209), 2017

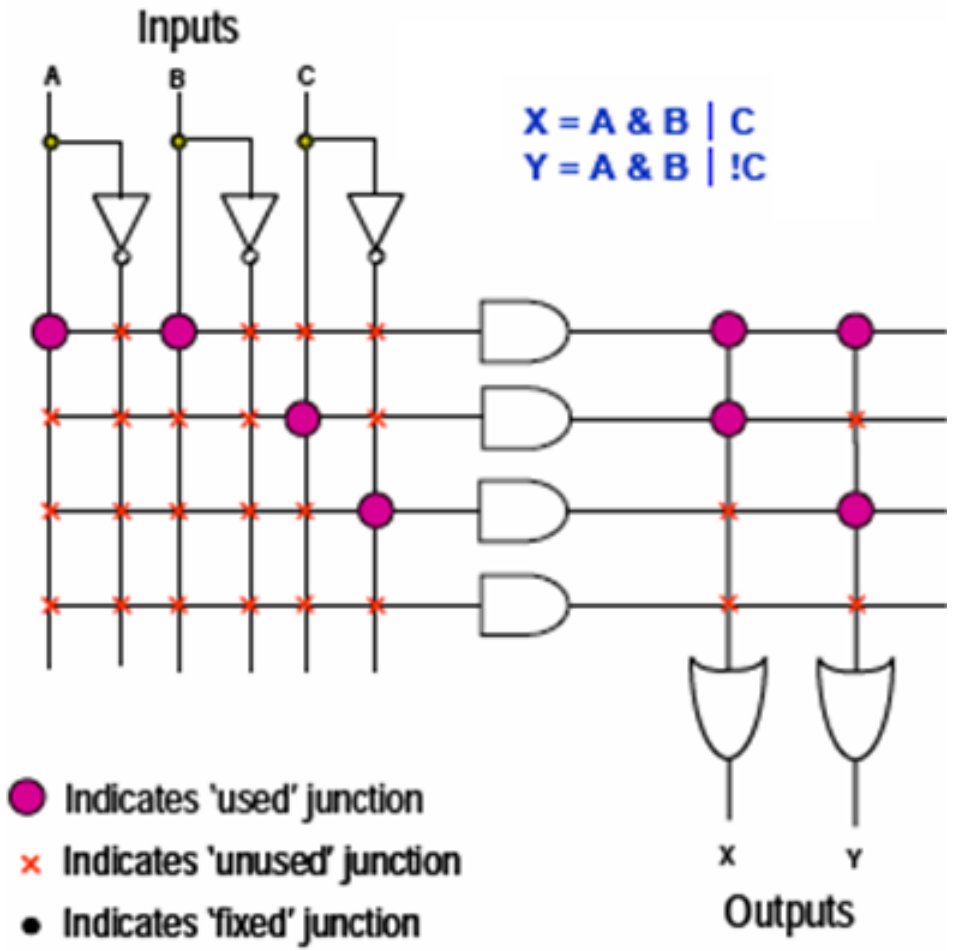
# Outline

# History of Programmable Logic


ليس سقوط المرء فشلاً وإنما الفشل أن يبقى حيث سقط
I can accept failure, Everyone fails at something.
But I cannot accept not trying.
- Michael Jordan

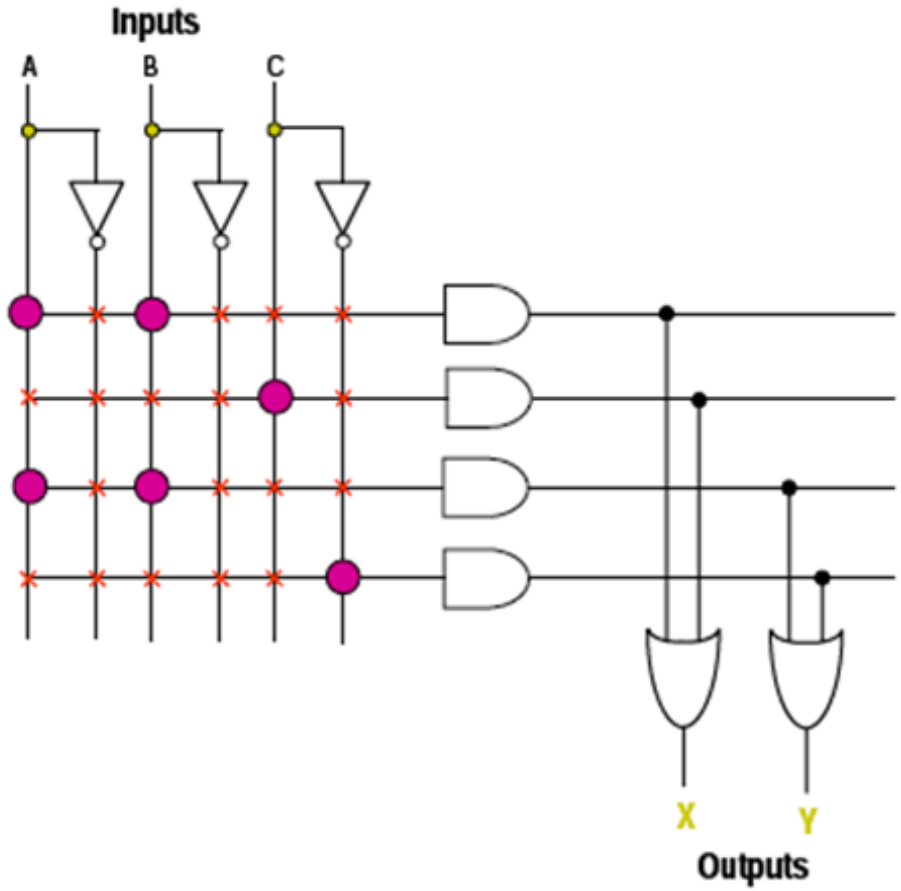
# Simple PLA

- Any combination of ANDs/ORs
- High Input-to-output delay (or propagation delay)
- Wafer geometries of 10$\mu m$ technology

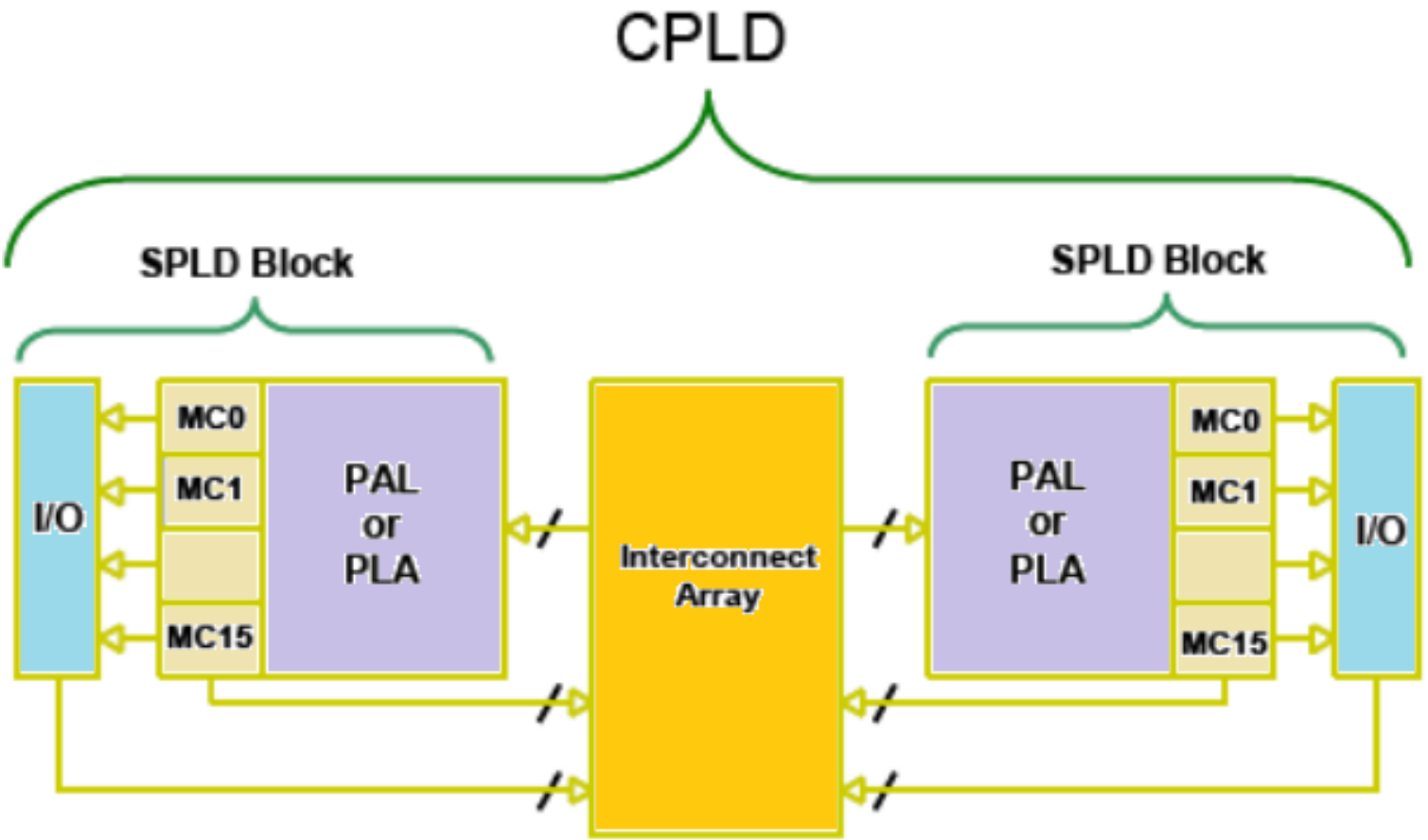


# Single Programmable Logic Device(SPLD)

- $t_{PD}$ being better
- Less complex software
- Output plan is fixed
- Medium logic density available to user



# Complex Programmable Logic Device(CPLD)




- PLD blocks (macrocells)
- Central global interconnect

# XC95 CPLD chip


Part marking for non-chip scale package

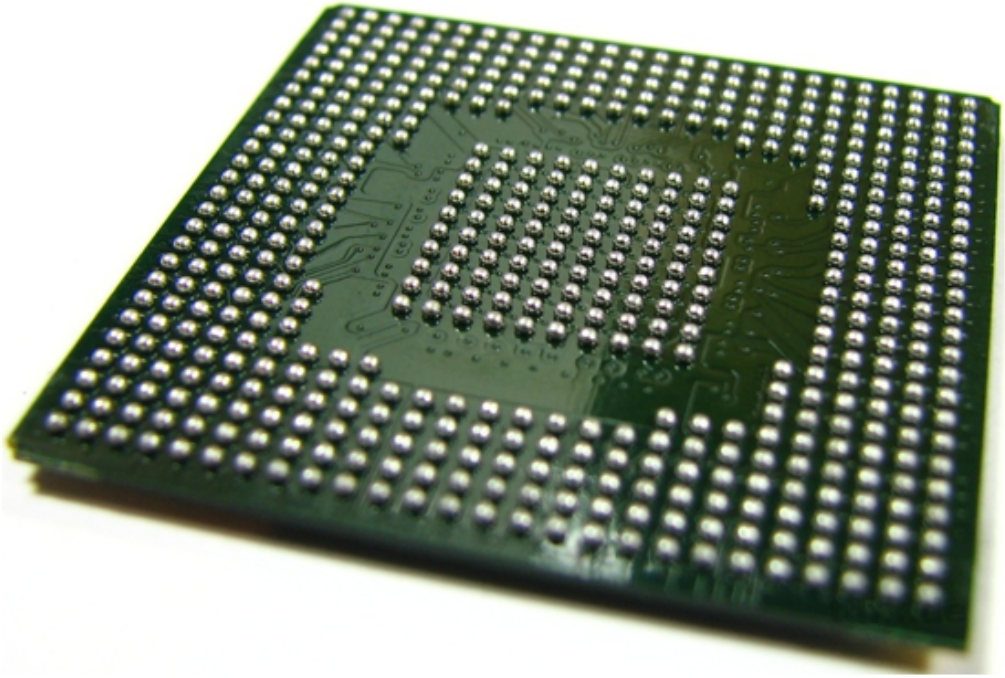
| Device |
|---|
| XC2S50E |
| XC2S100E |
| XC2S150E |
| XC2S200E |
| XC2S300E |
| XC2S400E |
| XC2S600E |

| Speed Grade | |
|---|---|
| -6 | Standard Performance |
| -7 | Higher Performance(1) |

| Package Type / Number of Pins | |
|---|---|
| TQ(G)144 | 144-pin Plastic Thin QFP |
| PQ(G)208 | 208-pin Plastic QFP |
| FT(G)256 | 256-ball Fine Pitch BGA |
| FG(G)456 | 456-ball Fine Pitch BGA |
| FG(G)676 | 676-ball Fine Pitch BGA |

| Temperature Range ($T_J$)(2) | |
|---|---|
| C = Commercial | 0°C to +85°C |
| I = Industrial | –40°C to +100°C |

# BGA vs QFP




BGA: Ball Grid Array
QFP: Quad Flat Pack

| Package Type / Number of Pins | |
|---|---|
| TQ(G)144 | 144-pin Plastic Thin QFP |
| PQ(G)208 | 208-pin Plastic QFP |
| FT(G)256 | 256-ball Fine Pitch BGA |
| FG(G)456 | 456-ball Fine Pitch BGA |
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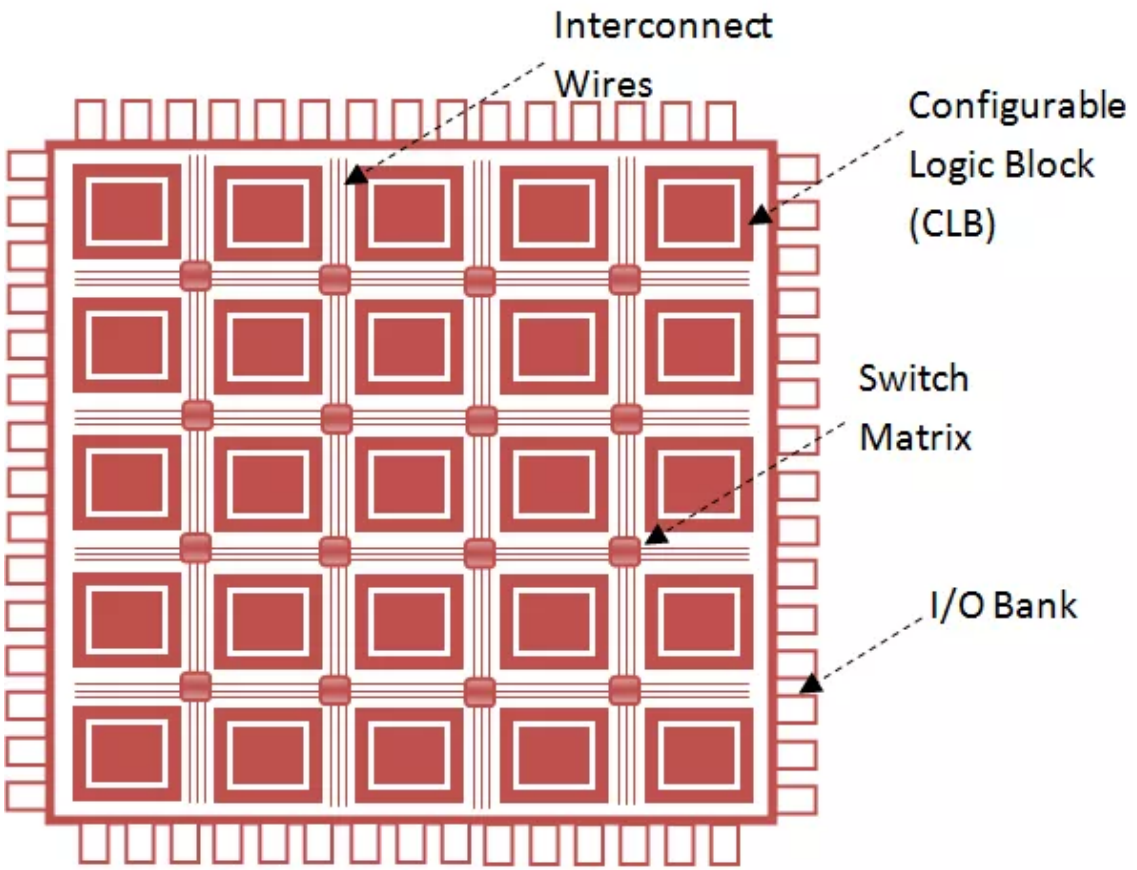
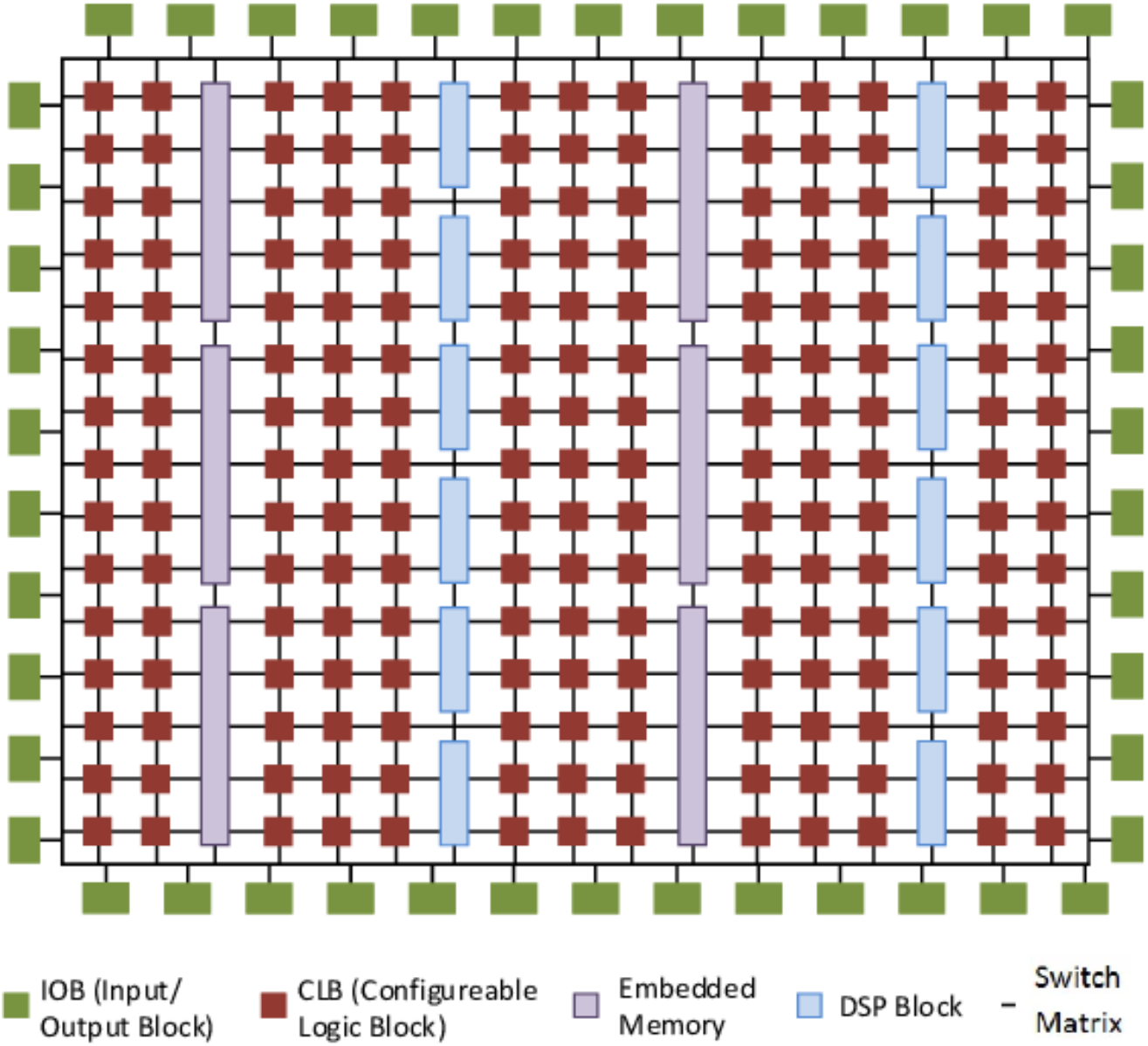
# History of FPGA

# Field Programmable Gate Arrays (FPGA)




- Post layout timing (*importance of placement).
- Fast register pipelining.
- exceeding the 10 million gate.
- Wafer 90 nm technology, eight- layer metal process technology.

# FPGA Architecture components



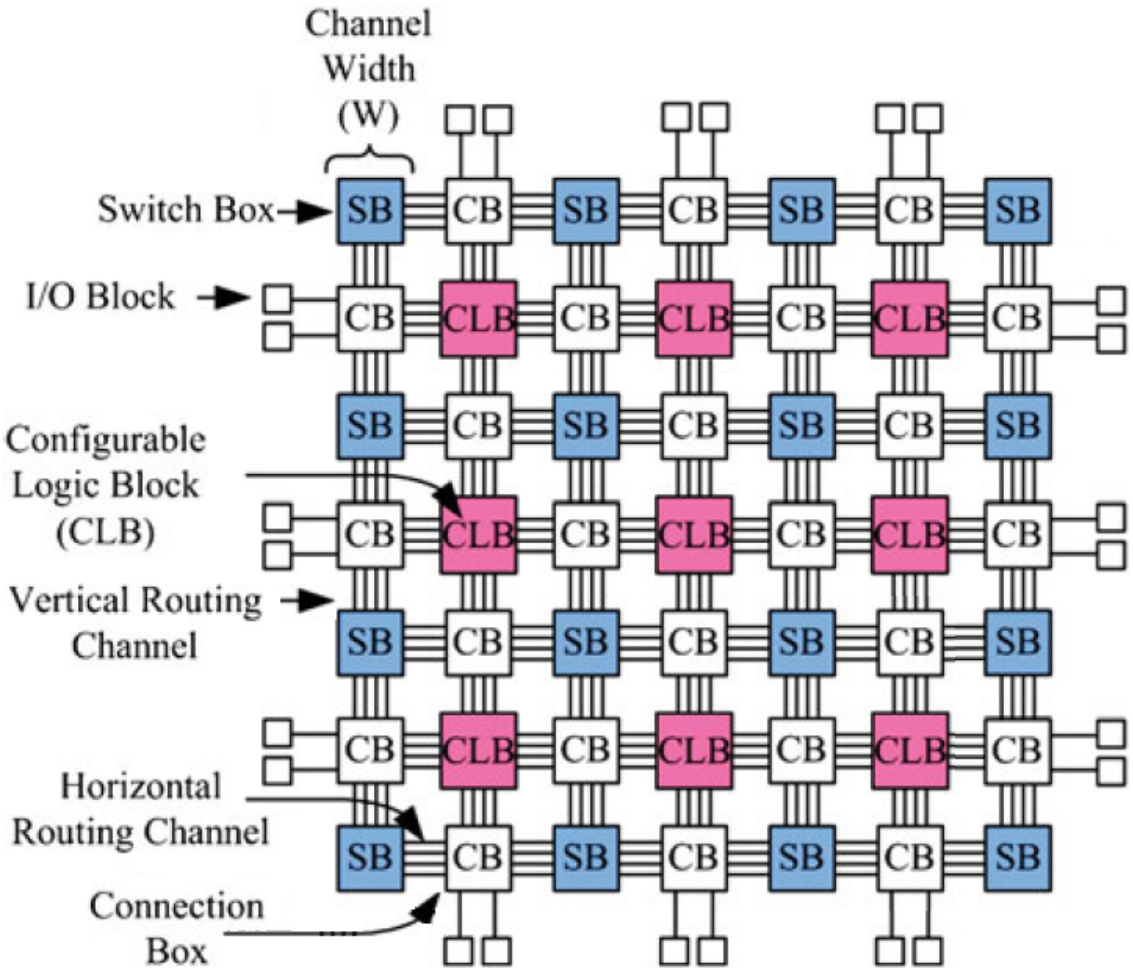
# FPGA architecture components

# Definition

The routing interconnect of an FPGA consists of wires[1] and programmable switch[2].

FPGA architectures:

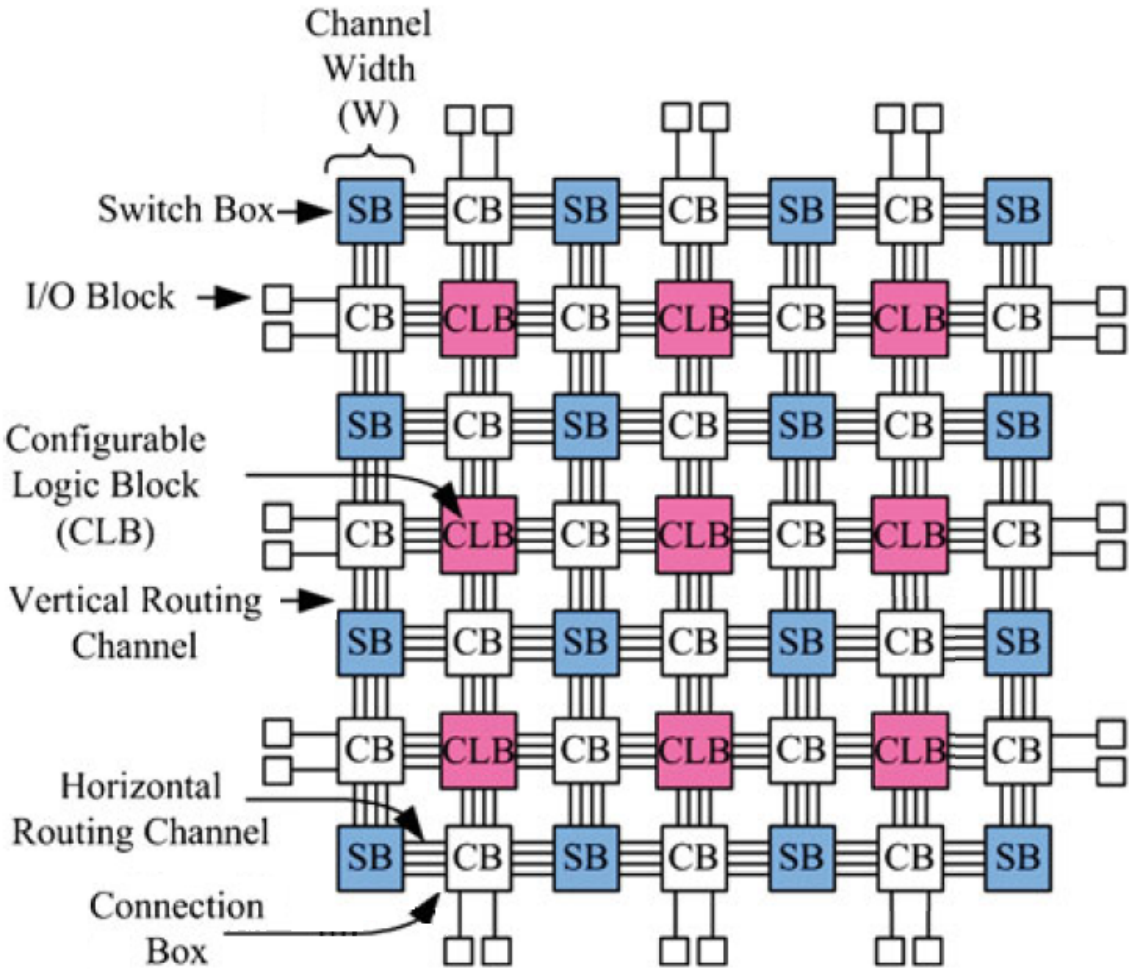
- Island-Style Routing Architecture.
- hierarchical.



# Island-Style Routing Architecture

FPGA architectures:

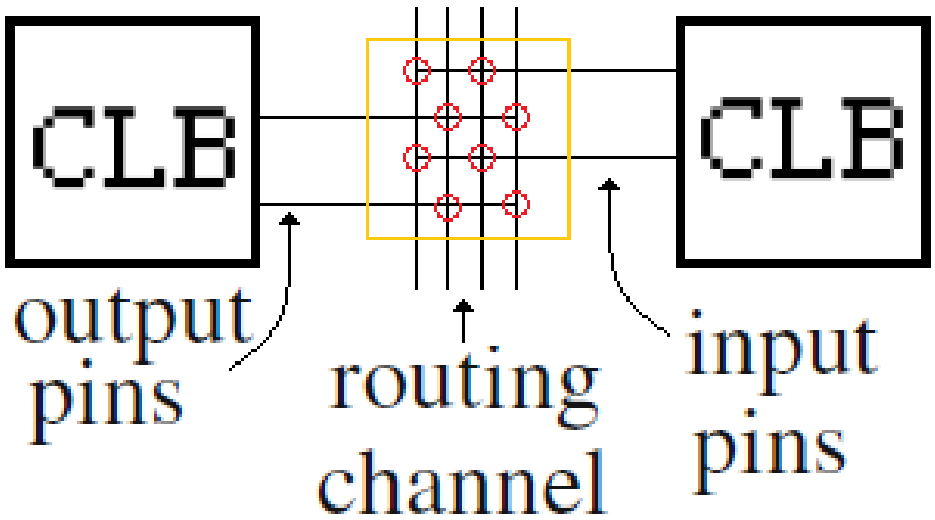
- The most commonly used architecture.
- (CLBs) are arranged on a 2D grid.
- Pre-fabricated wiring segments.
- Programmable switches.
- Routing network occupies 80?90% of total area/ 20-10% CLB.



# Connection Box

Connection box: connects the adjacent Logic blocks. Fc(in):The ratio of connectivity between input pins and routing channel. Fc(out):The ratio of connectivity between output pins and routing channel

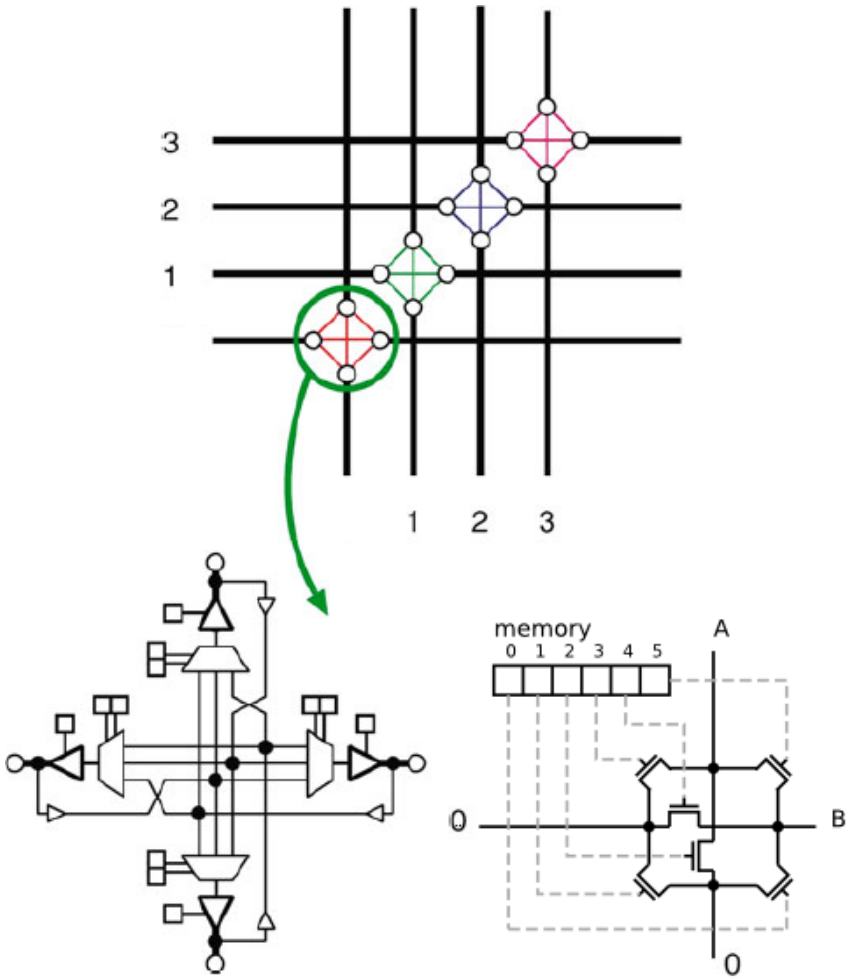
Example:Fc(in) equal to 1.0 means that all the tracks of adjacent routing channel are connected to the input pin of the logic block.




Fc(in)=0.5

# Switching Box (Bidirectional)

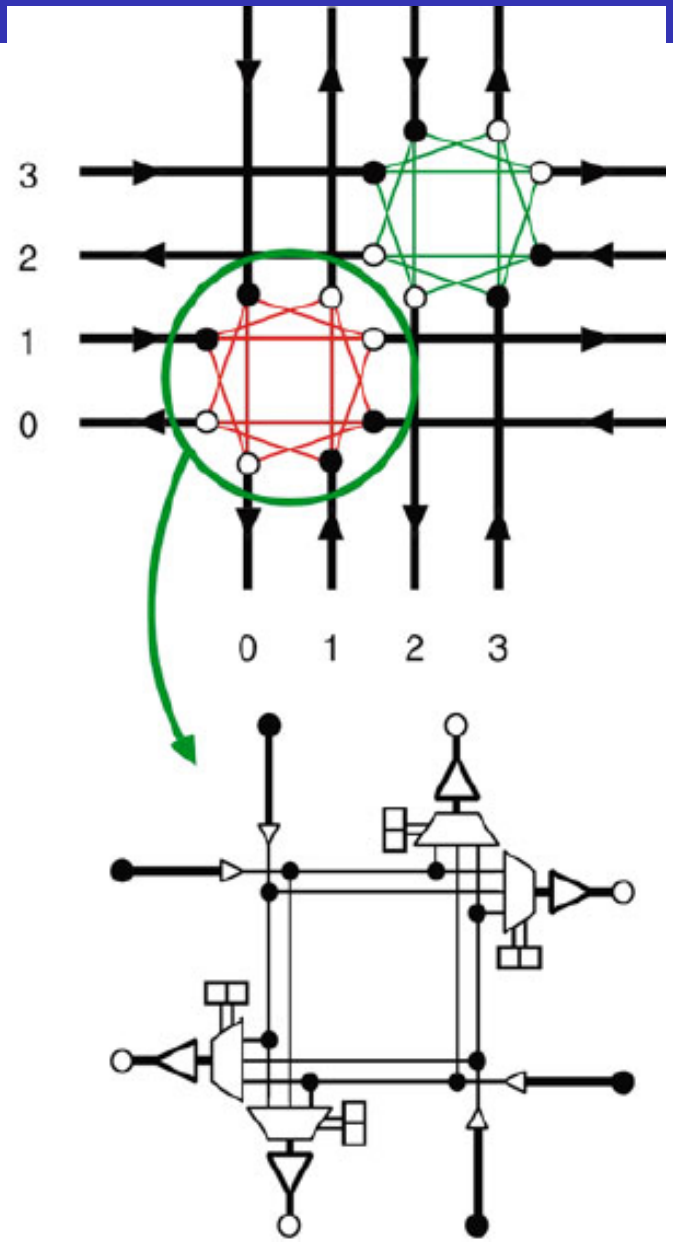
Switching Box: connects the vertical and horizontal routing tracks. Fs(in):how many track could be attached to each entering track.




Fc(in)=3

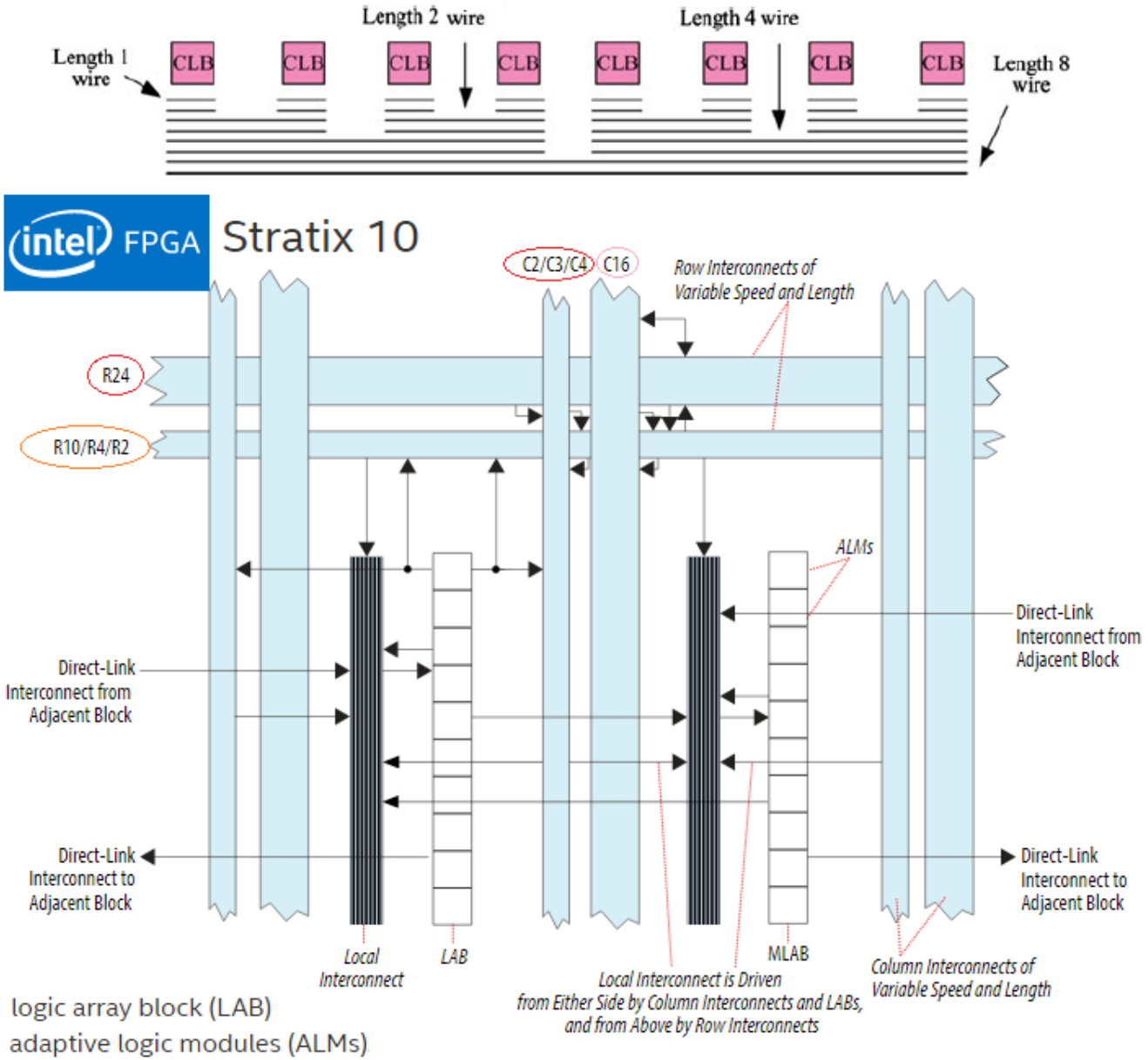
# Switching Box (Directional)

Switching Box: connects the vertical and horizontal routing tracks. Fs(in):how many track could be attached to each entering track.



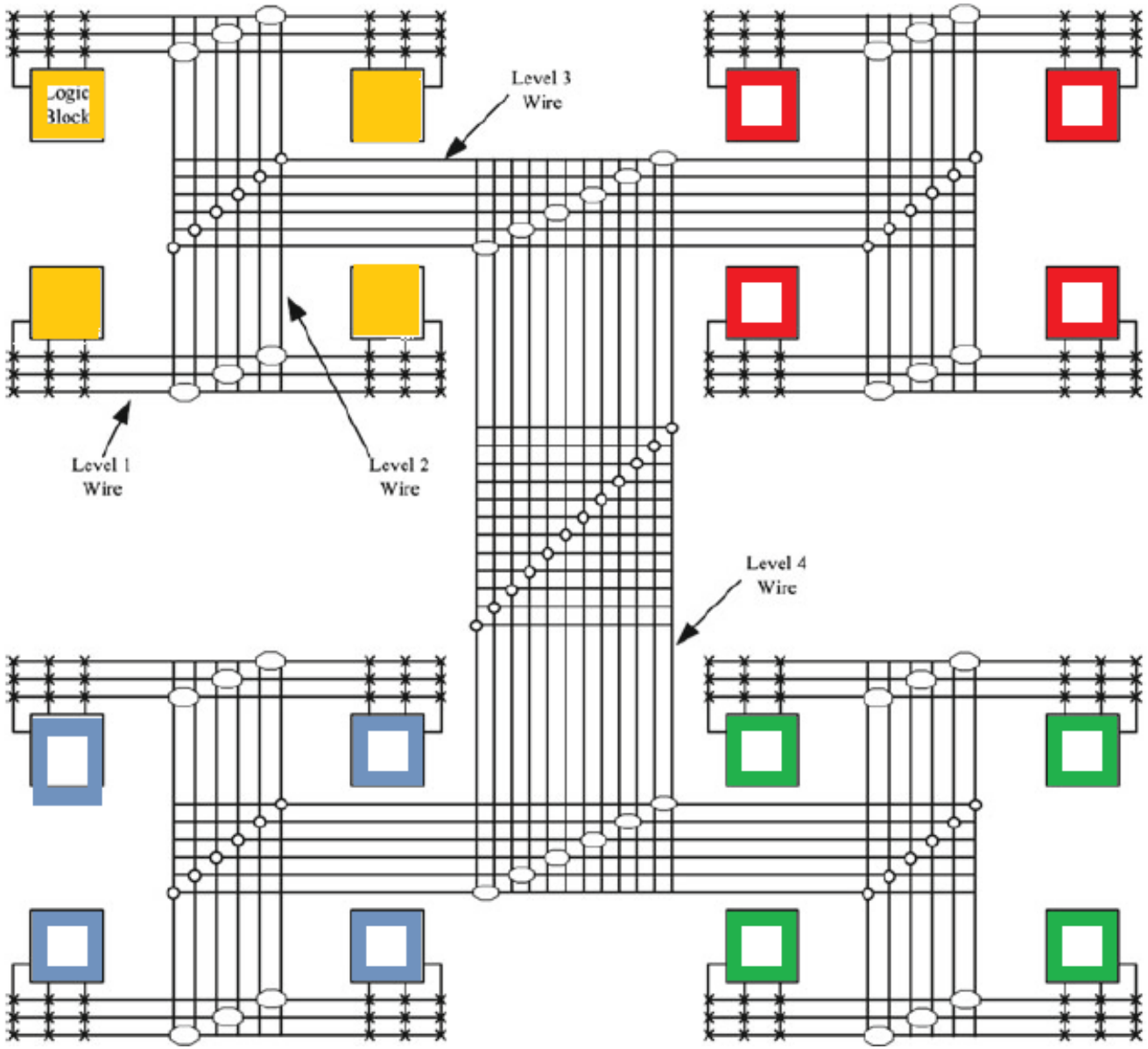
# Channel segment distribution

Flexibility Vs. Delay
In mesh-based FPGAs, multi-length wires are created to reduce delay.



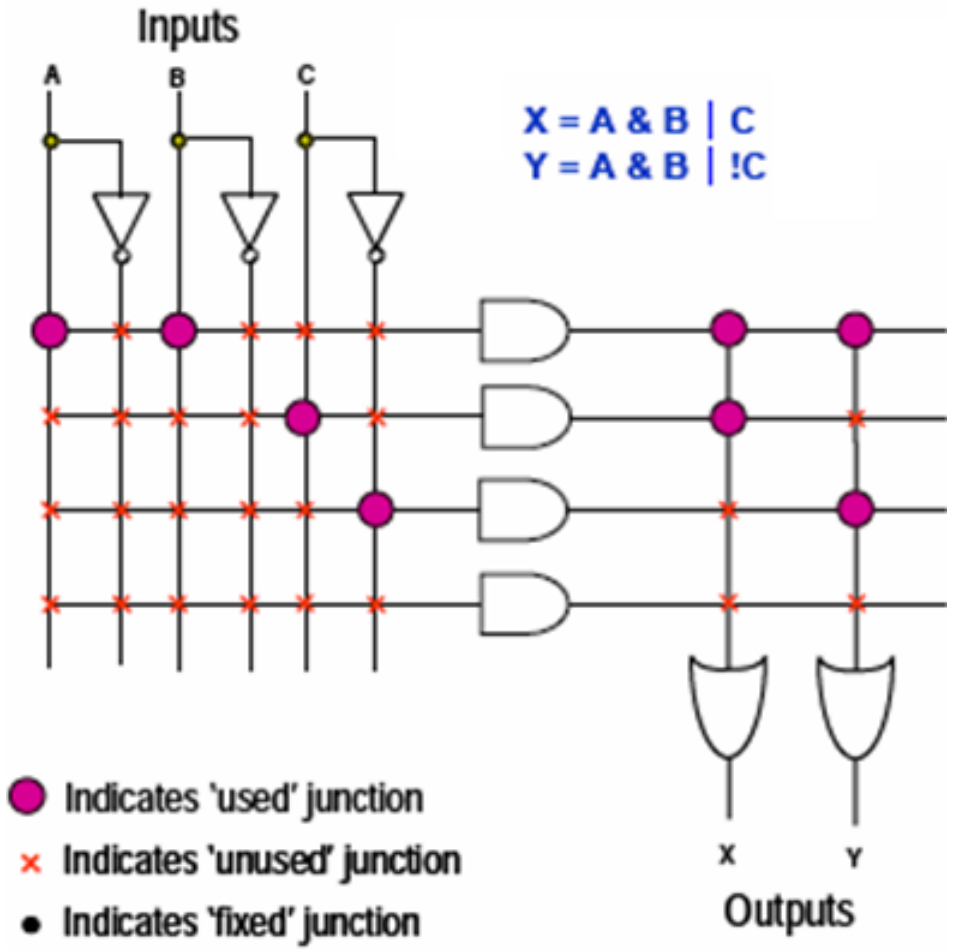
# Hierarchical Routing Architecture

In the hierarchical FPGA called HFPGA, LBs are grouped into clusters. Clusters are then grouped recursively together

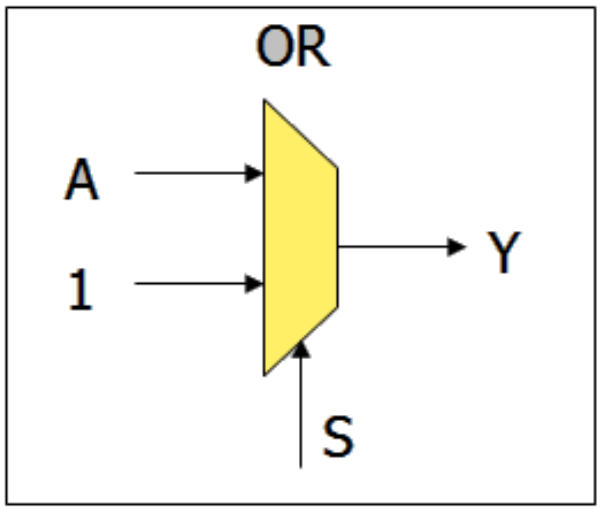


# CLB:PAL style wide input gates

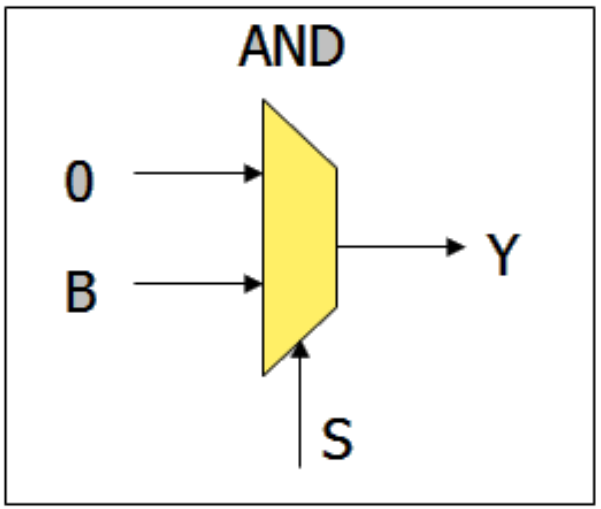
- Fine-grained logic block.
- Large amounts of programmable interconnect.
  1. Area-inefficiency(High routing), ,.
  2. Low performance (delay).
  3. High power consumption(high interconnect capacitance)



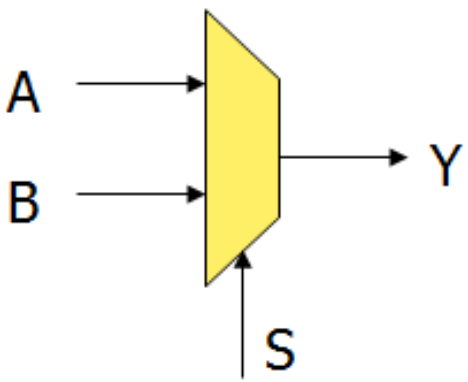
# CLB:Multiplixers

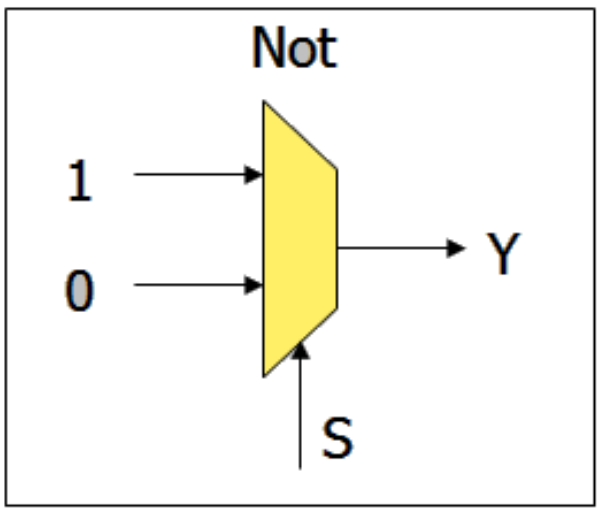



| A | S | Y |
|---|---|---|
| 0 | 0 | A |
| 0 | 1 | 1 |
| 1 | 0 | A |
| 1 | 1 | 1 |




| B | S | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | B |
| 1 | 0 | 0 |
| 1 | 1 | B |




| S | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

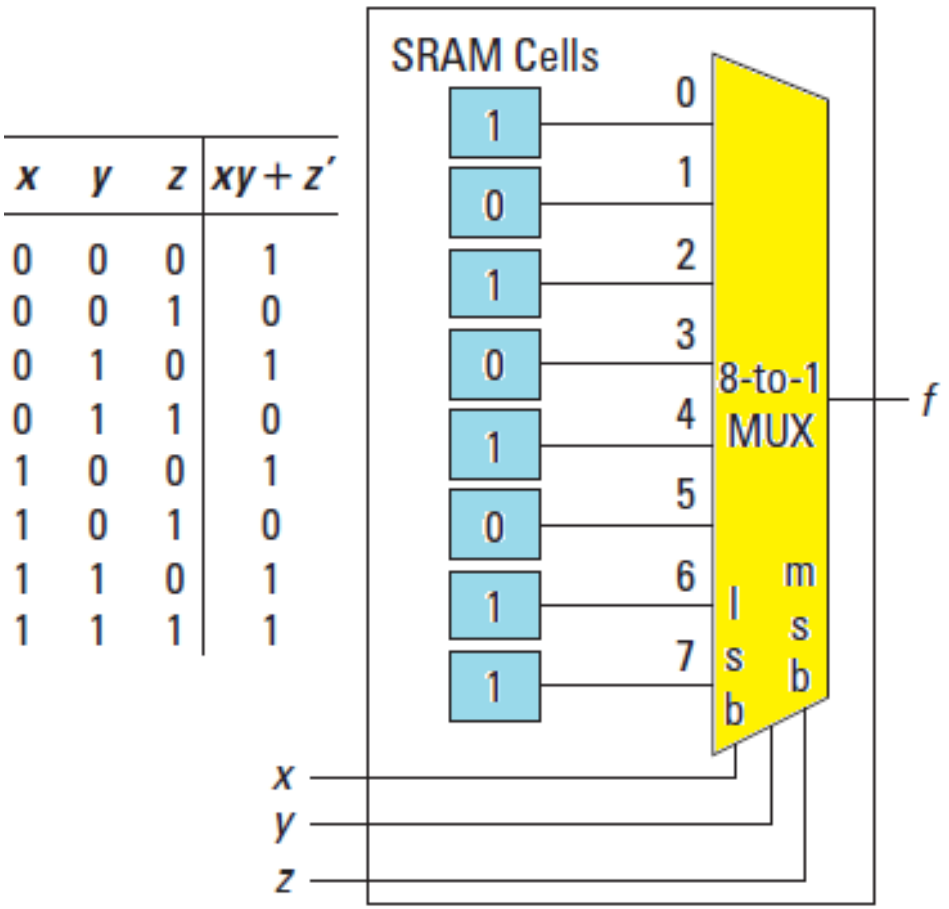
# CLB:look-up table (LUT)

CLB:Configurable Logic Block

$f(x, y, z) = xy + \bar{z}$

1. Function's output bits connected as inputs to an 8x1 multiplexer (MUX).
2. Inputs (x,y,z) would be the select lines for the MUX.
3. Regardless of the complexity, single LUT.

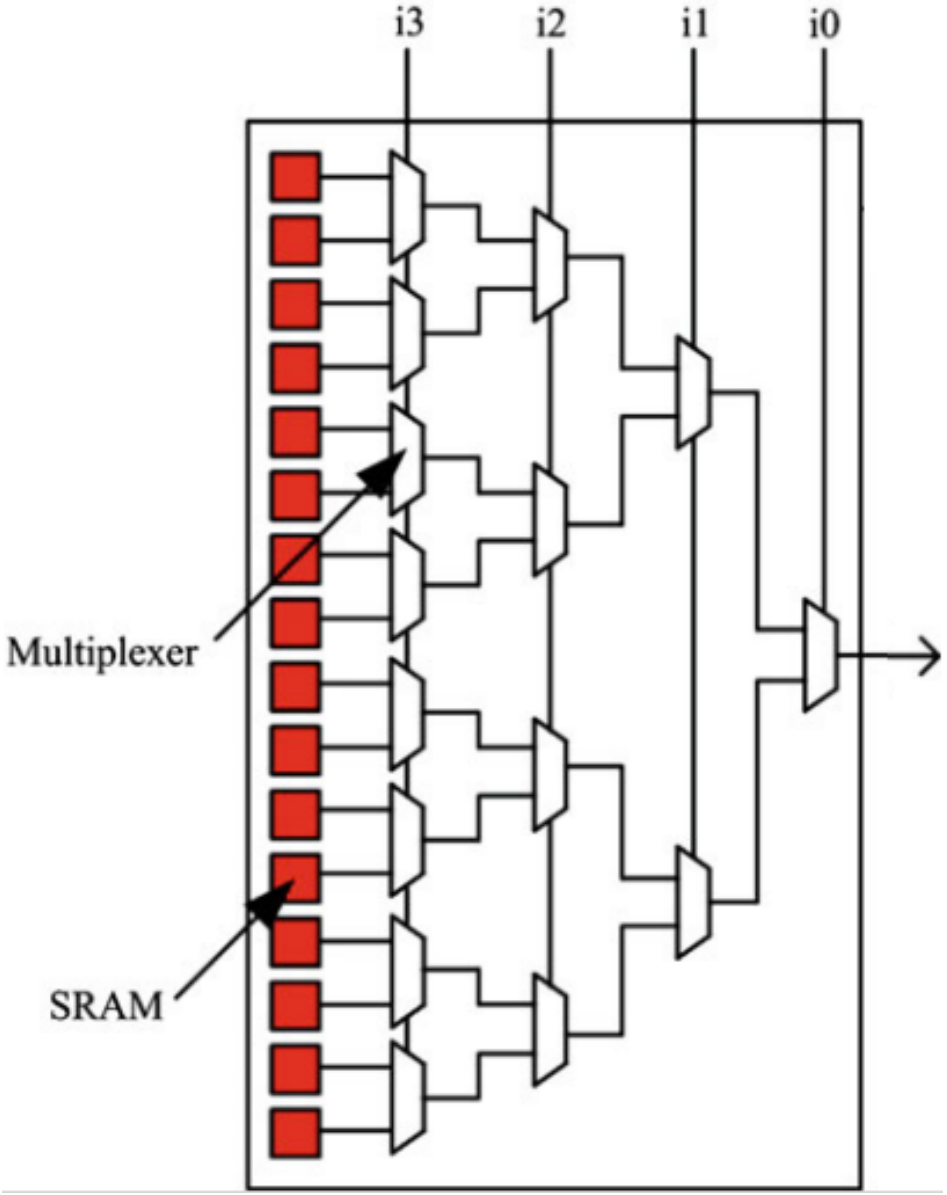
| x | y | z | xy + z′ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |



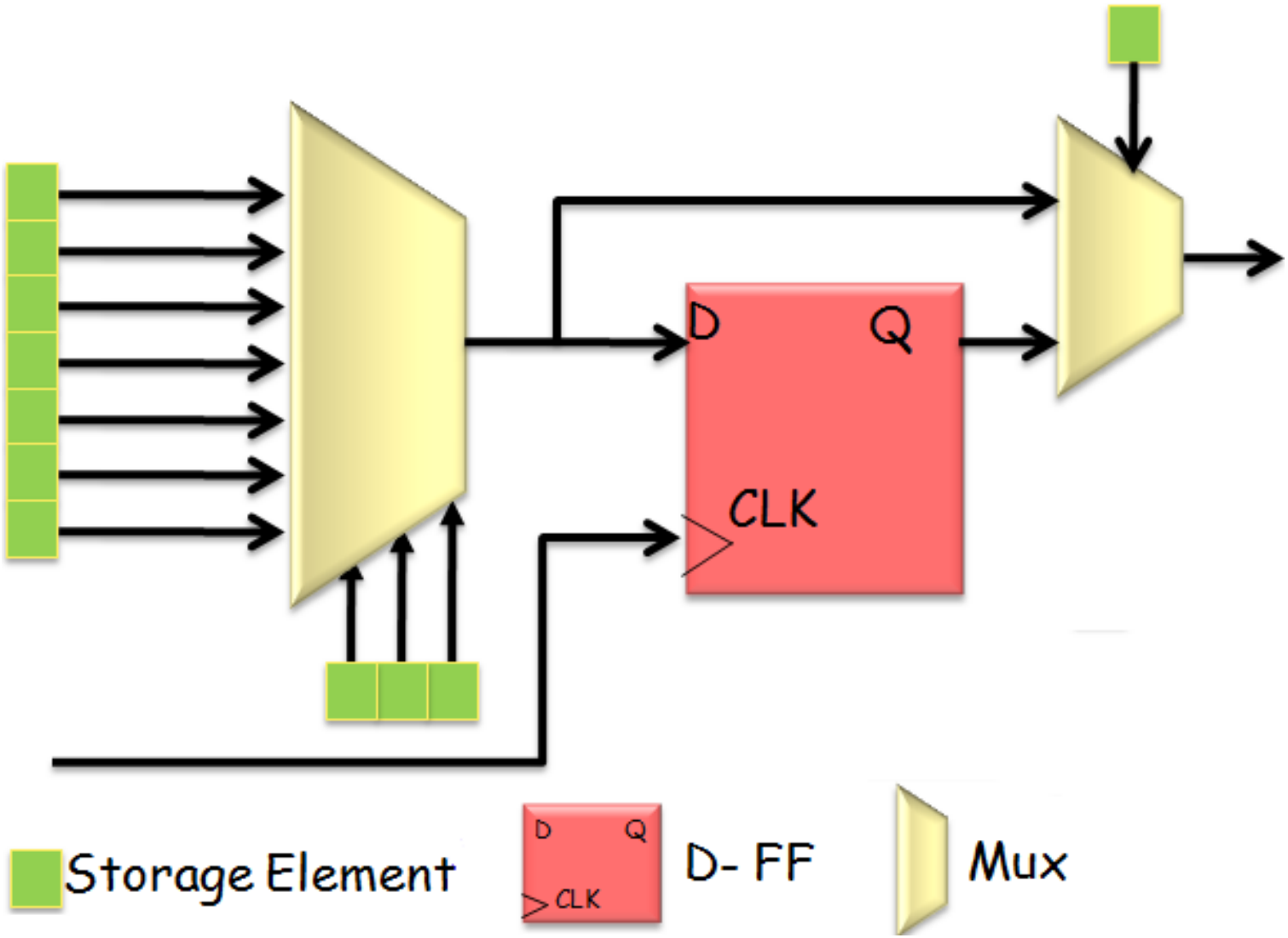
# CLB:look-up table (LUT)

4 input LUT (LUT-4)

1. Coarse-grained logic block.
2. n_input function generator consists of a $2^n$-to-1 multiplexer (MUX).
3. Called n-MUX
4. Delay depends on the number of LUTs

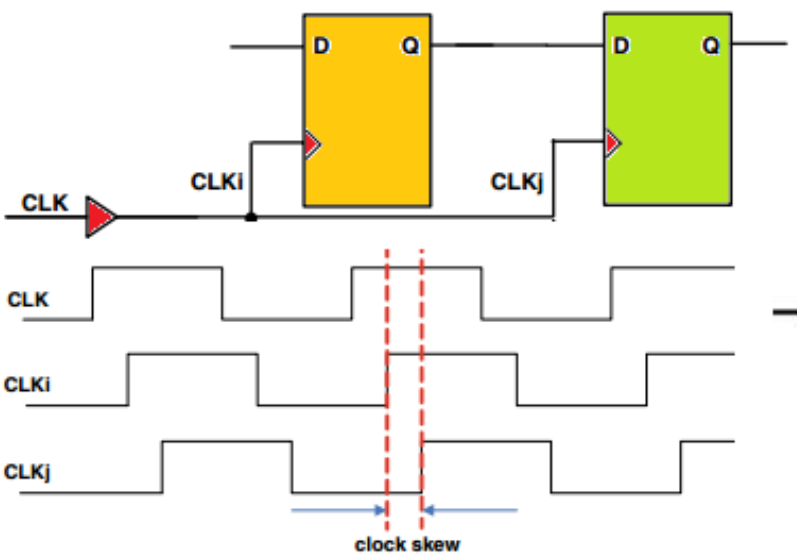


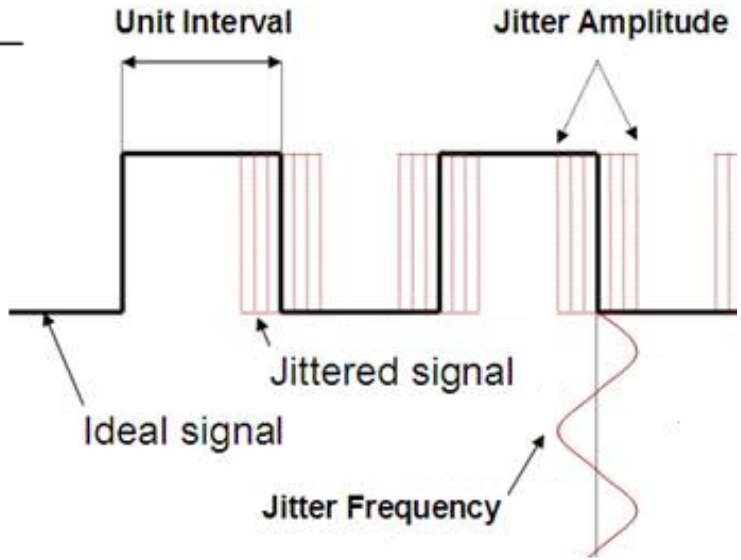
# CLB:Syncronous Vs. Asyncrouns



# Definition

Digital Clock Manager (DCM): provides different clock periods (frequency synthesizer multiply/divide input clock), and eliminates clock deskewing, jitter, and Phase shifting. definition



# ref

Ron Sass Andrew G. Schmidt, "Embedded Systems Design with Platform FPGAs Principles and Practices", chapter 2-2 Umer Farooq, et al ,"Tree-Based Heterogeneous FPGA Architectures",2012 Springer, Chapter 2