

Digital Clock Manager (DCM) and Static Time Analysis (STA)

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Advanced Microprocessor (EEC 209), 2017

Outline

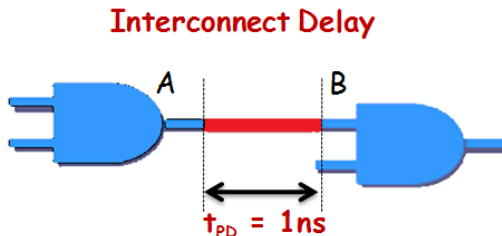
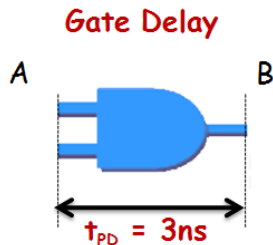
- 1 Paths and Delays
- 2 Metastability
- 3 Clock Skew
 - Minimizing the clock skew
- 4 References

Paths and Delays



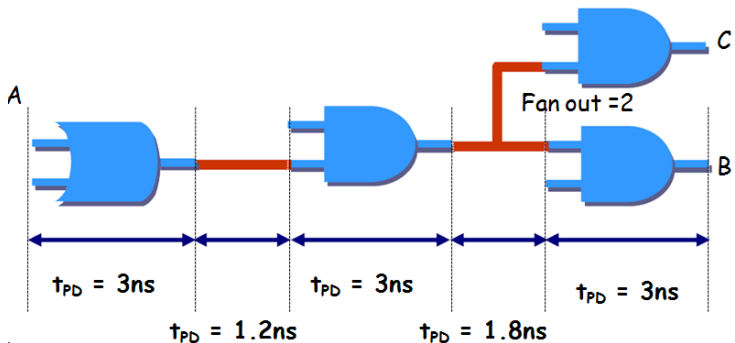
Propagation Delay

Propagation Delay: The time required for a signal to travel from A to B, measured in nanoseconds (ns).



Path Delay

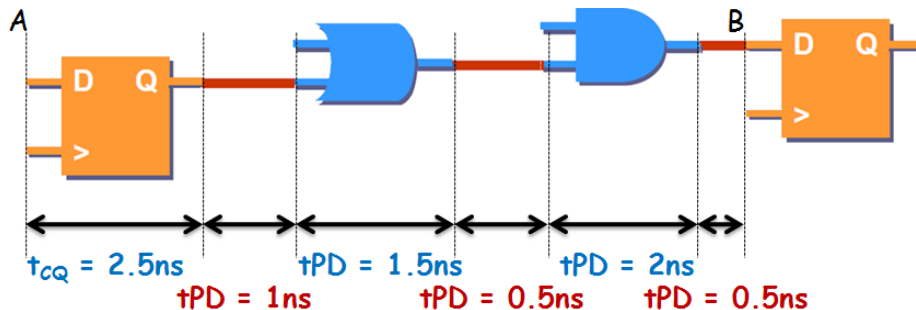
Path Delay: The sum of all the gate and net delays from starting to ending point.



Path Delay "A" to "B" = sum of all gate + net delays
 $3\text{ns} + 1.2\text{ns} + 3\text{ns} + 1.8\text{ns} + 3\text{ns} = 12\text{ns}$

Maximum Frequency / Critical path

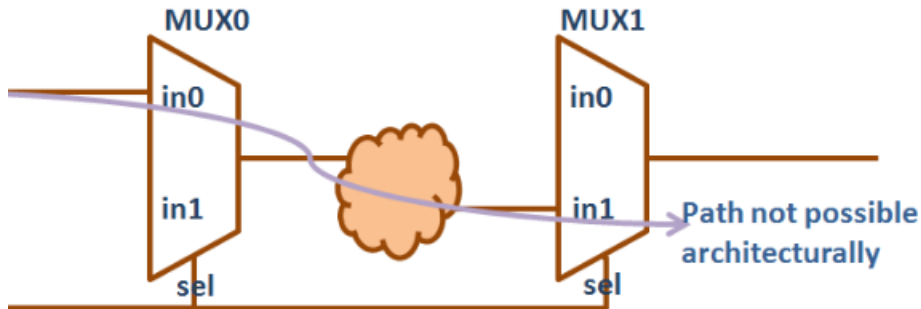
Maximum Frequency: The fastest speed a circuit containing flip-flops can operate.



$$\begin{aligned}
 f_{MAX} &= \frac{1}{\text{ff delay} + \text{gate delays} + \text{net delays}} \\
 &= \frac{1}{(2.5 + 1 + 1.5 + 0.5 + 2 + 0.5)ns} \\
 &= 125MHz
 \end{aligned}$$

False path

false paths: There are some timing paths that are never possible to occur.



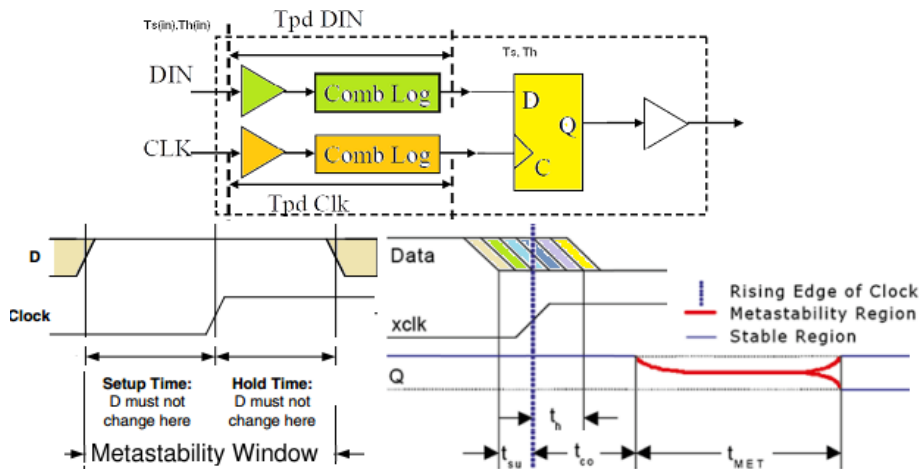
Metastability



Setup Time and Hold Time

- Metastability: Result of violation of setup and hold times of a flip flop.
- Setup Time: The time required for data input to remain stable prior to arrival of clock pulse.
- Hold Time: The time required for data input to remain stable after the arrival of clock pulse.

Setup Time and Hold Time

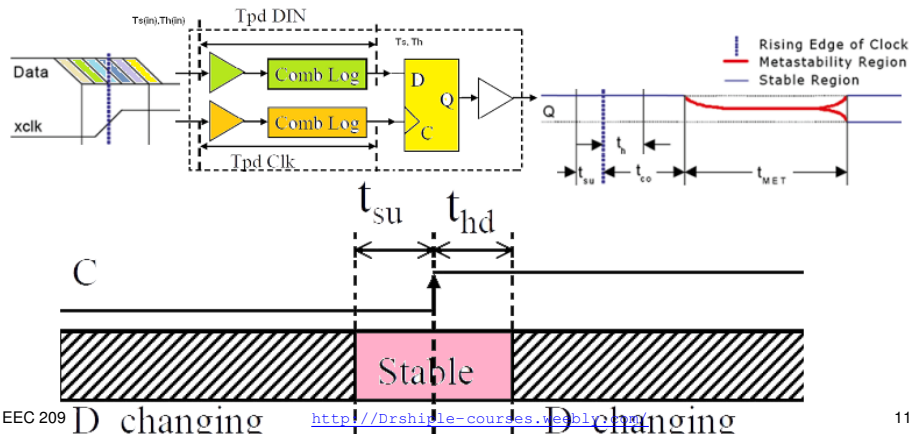


Calculations

$$T_{Set} \leq (T_{pdCLK})_{min} - (T_{pdDin})_{max}$$

$$T_{Hold} \leq (T_{pdDin})_{min} - (T_{pdCLK})_{max}$$

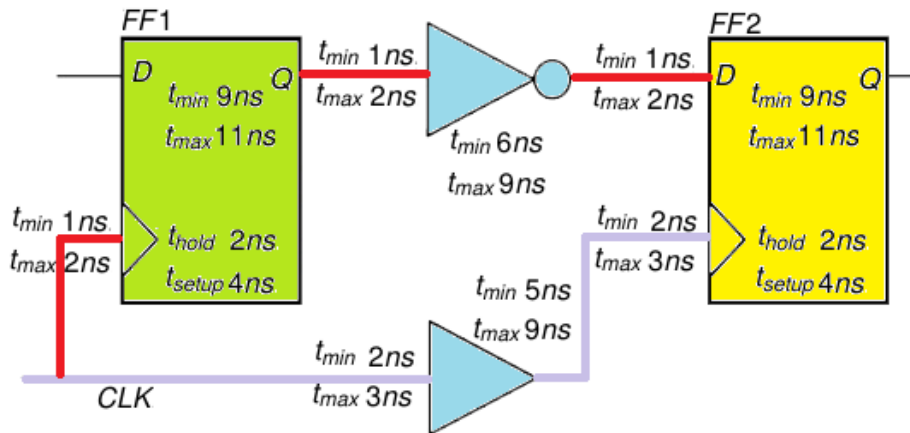
calculation



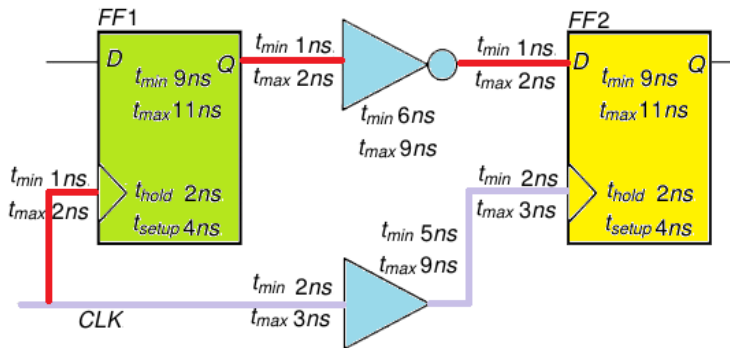
Example 2:

Calculate

System setup and hold times, for given path delays



Example 2:

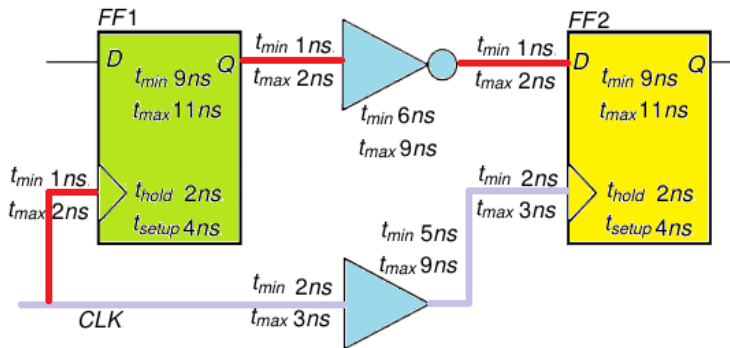


$$Data_path(max) = 2 + 11 + 2 + 9 + 2 + 4 = 30ns$$

$$Clock_period(min) = 30ns$$

$$Max_Frequency = 1/30 = 33.3MHz$$

Example 2:



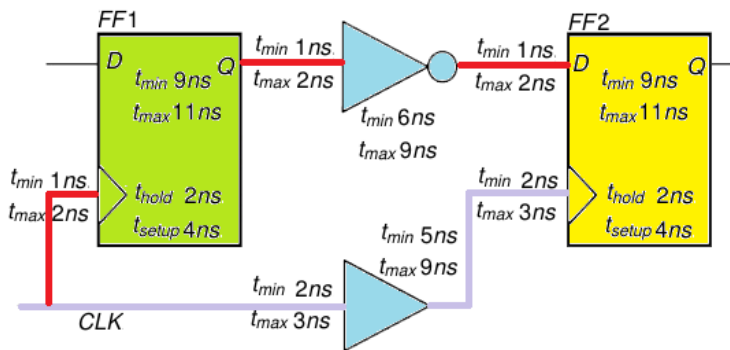
$$Data_path(max) = 2 + 11 + 2 + 9 + 2 + 4 = 30ns$$

$$Clock_period(min) = 15ns + 2 + 5 + 2 = 24$$

$$clk\ period=15$$

data lag clock by 6 ns (violation)

Example 2:



$$Data_path(min) = 1 + 9 + 1 + 6 + 1 = 18\text{ns}$$

$$Clock_period(max) = 3 + 9 + 3 + 2 = 17\text{ns}$$

data lag clock by 1 ns (no hold violation)

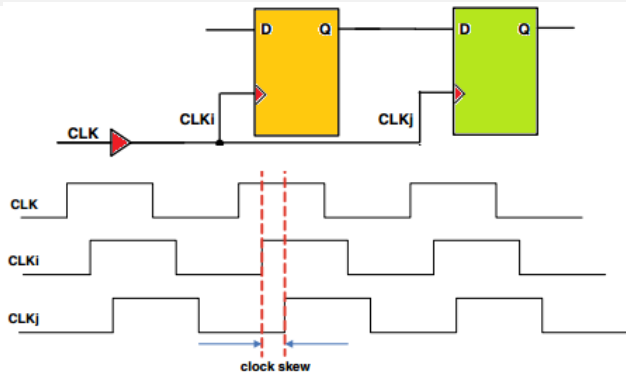
Avoiding Metastability

- When the input signal is an asynchronous signal.
- When the clock skew/slew (rise/fall times) is higher than the tolerable limit.
- When signals cross the domains working at two different frequencies or with same frequency but different phase and skew.
- When the combinational delay is such that the Flip Flop data input changes in the Metastability Window.

Clock Skew



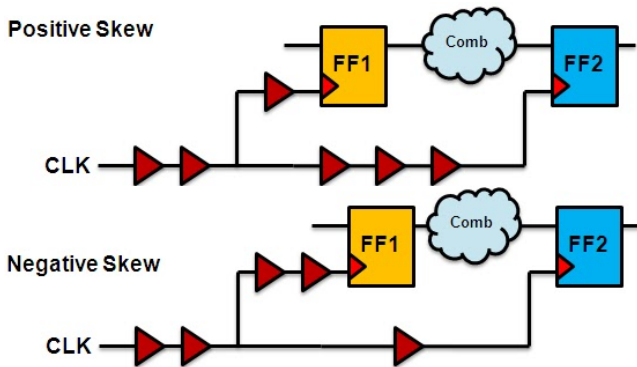
Definition



Clock skew is a phenomenon in synchronous circuits in which the clock signal arrives at different components at different times. Due to:

- Wire-interconnect length
- Temperature variations
- Capacitive coupling
- Material imperfections and differences in input capacitance on the clock inputs

Positive vs Negative Skew



$$CLK, D, Q, t_{hold} = 2ns, t_{setup} = 4ns$$

Adding Delay in Data Path

File: TDI_C: Dd1.wcp to 30.18213mm - Interactive Length Tuning ...

Target Length: 10.000mm

Based on the center of the conductor and the pad center position. Units: Layer 122, 2600 mils

Layer	Prep
1	1000 mils
2	1000 mils
3	1000 mils
4	1000 mils
5	1000 mils
6	1000 mils
7	1000 mils
8	1000 mils
9	1000 mils
10	1000 mils
11	1000 mils
12	1000 mils
13	1000 mils
14	1000 mils
15	1000 mils
16	1000 mils
17	1000 mils
18	1000 mils
19	1000 mils
20	1000 mils
21	1000 mils
22	1000 mils
23	1000 mils
24	1000 mils
25	1000 mils
26	1000 mils
27	1000 mils
28	1000 mils
29	1000 mils
30	1000 mils
31	1000 mils
32	1000 mils
33	1000 mils
34	1000 mils
35	1000 mils
36	1000 mils
37	1000 mils
38	1000 mils
39	1000 mils
40	1000 mils
41	1000 mils
42	1000 mils
43	1000 mils
44	1000 mils
45	1000 mils
46	1000 mils
47	1000 mils
48	1000 mils
49	1000 mils
50	1000 mils

Style: New Style Max Gap Width: 2.000mm

Gap: 1.000mm

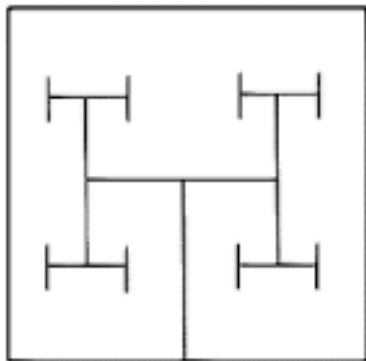
Amplitude Increment: 0.2 mm Gap Increment: 0.2 mm



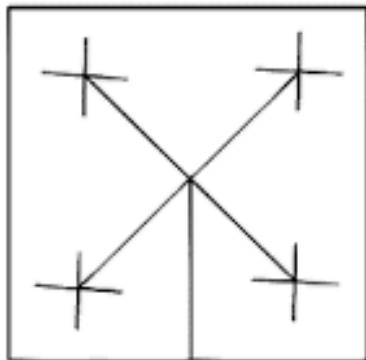
45.779mm

<http://Drshiplab.com/resources/pcb/11.html>

H-Tree

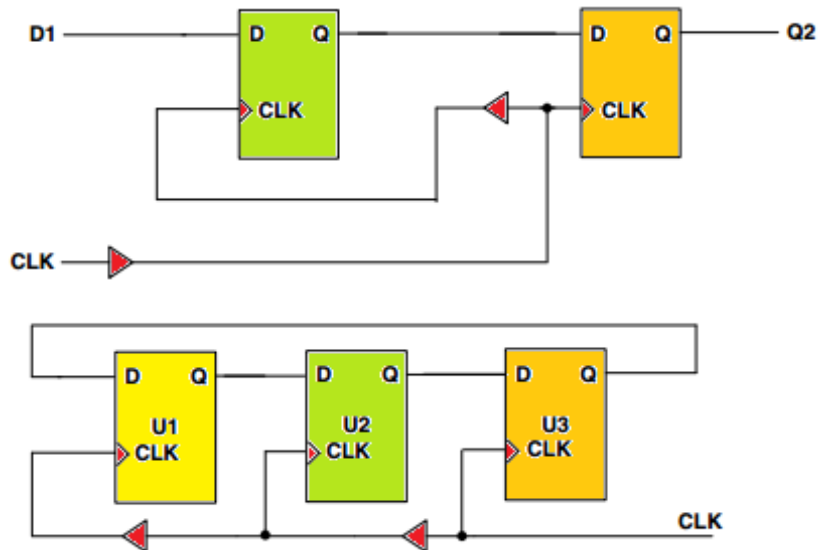


H - Tree

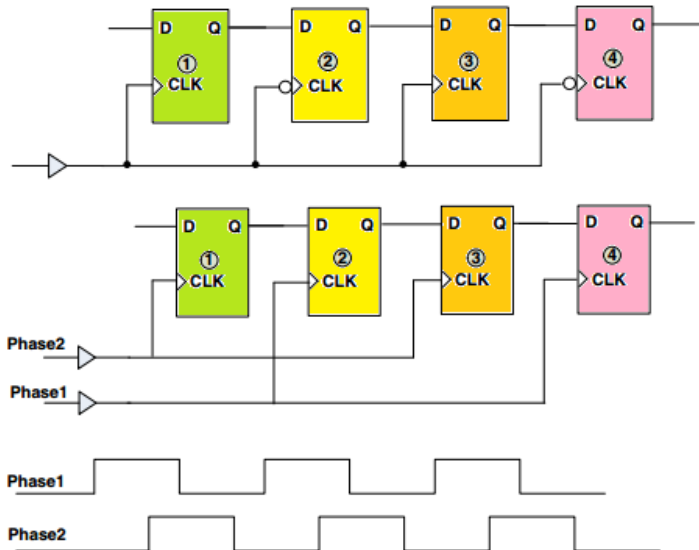


X - Tree

Clock Reversing



Clocking on Alternate Edges/Alternate Phases



Digital Clock Manager (DCM)

DCMs have the following applications:

- Multiplying or dividing an incoming clock (which can come from outside the FPGA or from a Digital Frequency Synthesizer).
- Making sure the clock has a steady duty cycle(50%).
- Adding a phase shift with the additional use of a Delay-locked loop.
- Eliminating clock skew within an FPGA design.

References



Ref.

- static time analysis

<http://www.vlsi-expert.com/2011/03/static-timing-a>