Digital Clock Manager (DCM) and Static Time Analysis (STA)

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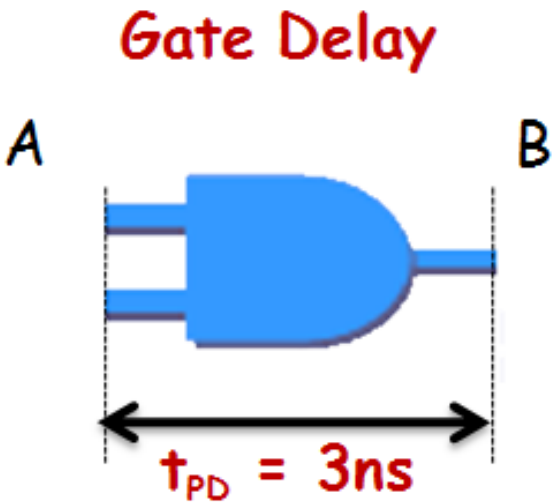
Advanced Microprocessor (EEC 209), 2017

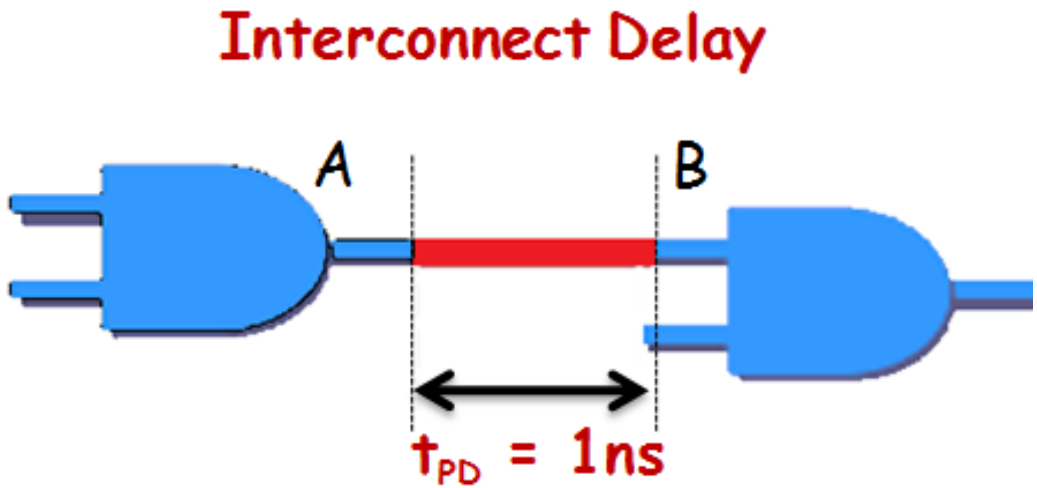
Outline

Paths and Delays

Propagation Delay

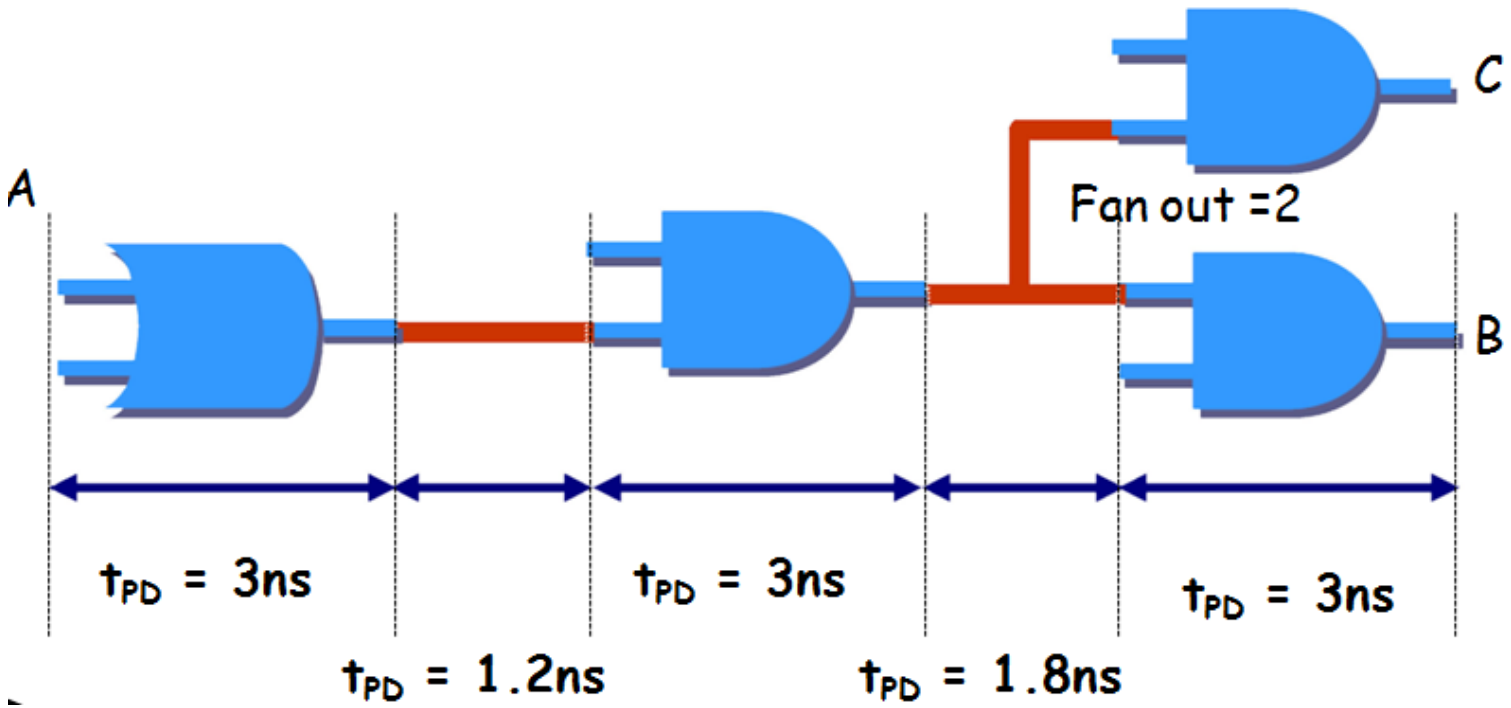
Propagation Delay: The time required for a signal to travel from A to B, measured in nanoseconds (ns).





Path Delay

Path Delay: The sum of all the gate and net delays from starting to ending point.

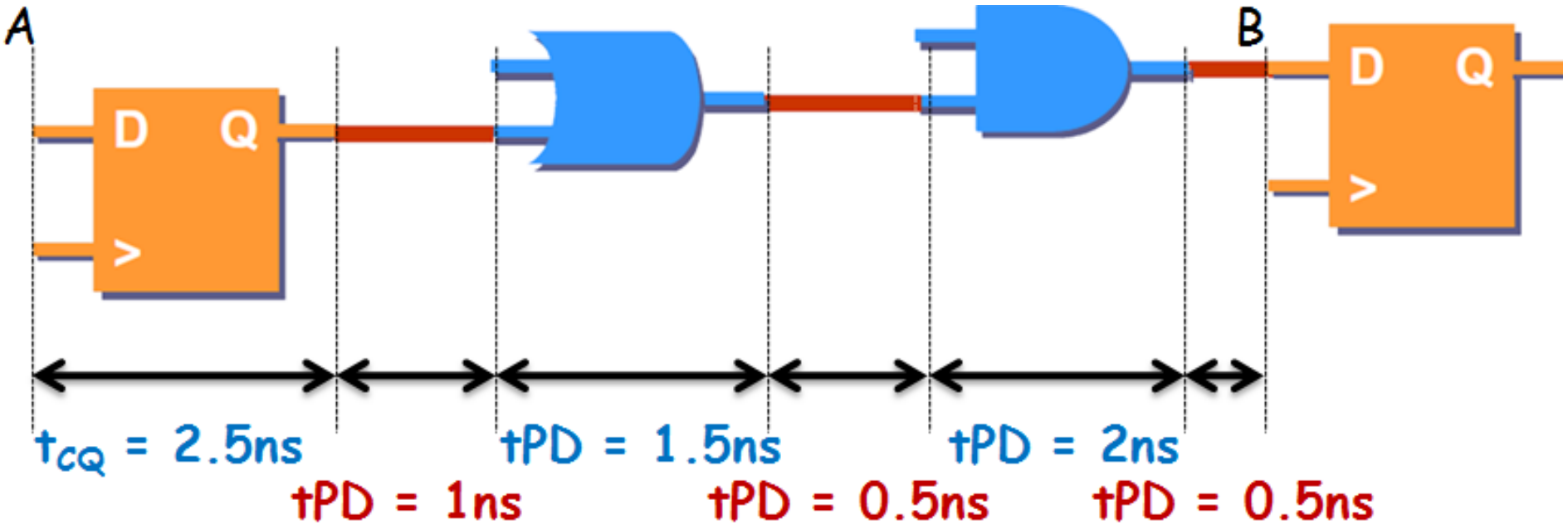


Path Delay "A" to "B" = sum of all gate + net delays

3ns + 1.2ns + 3ns + 1.8ns + 3ns = 12ns

Maximum Frequency / Critical path

Maximum Frequency: The fastest speed a circuit containing flip-flops can operate.



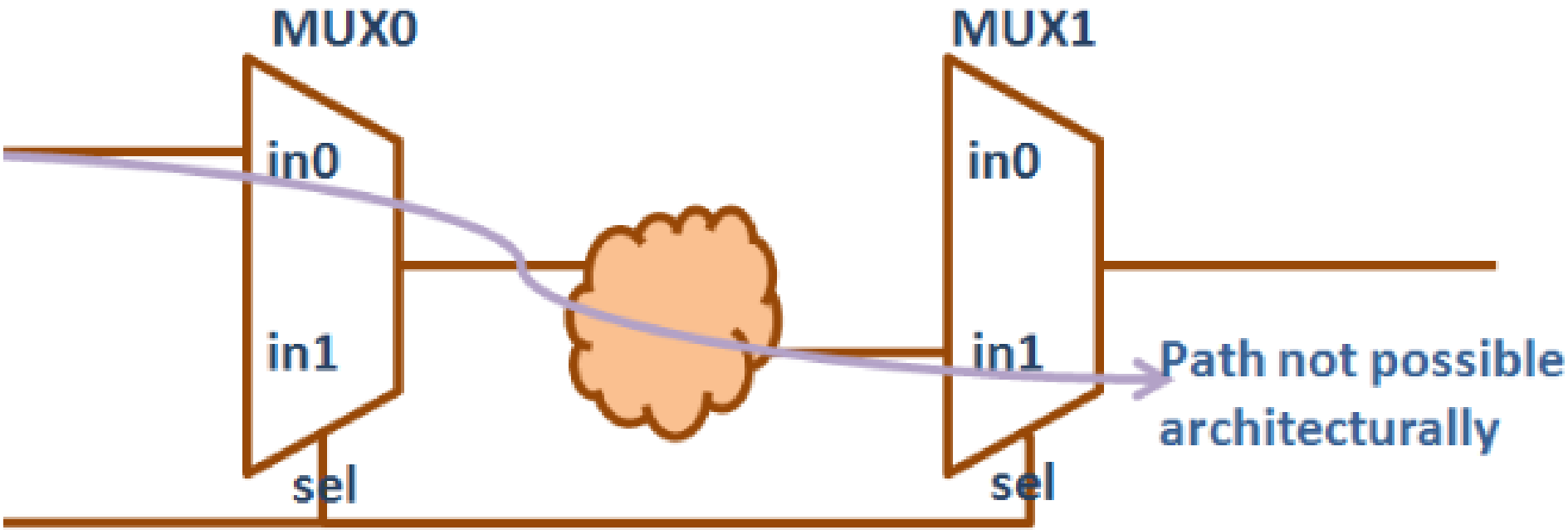
$$f_{MAX} = \frac{1}{\text{ff delay} + \text{gate delays} + \text{net delays}}$$

$$= \frac{1}{(2.5 + 1 + 1.5 + 0.5 + 2 + 0.5)ns}$$

$$= 125MHz$$

False path

false paths: There are some timing paths that are never possible to occur.

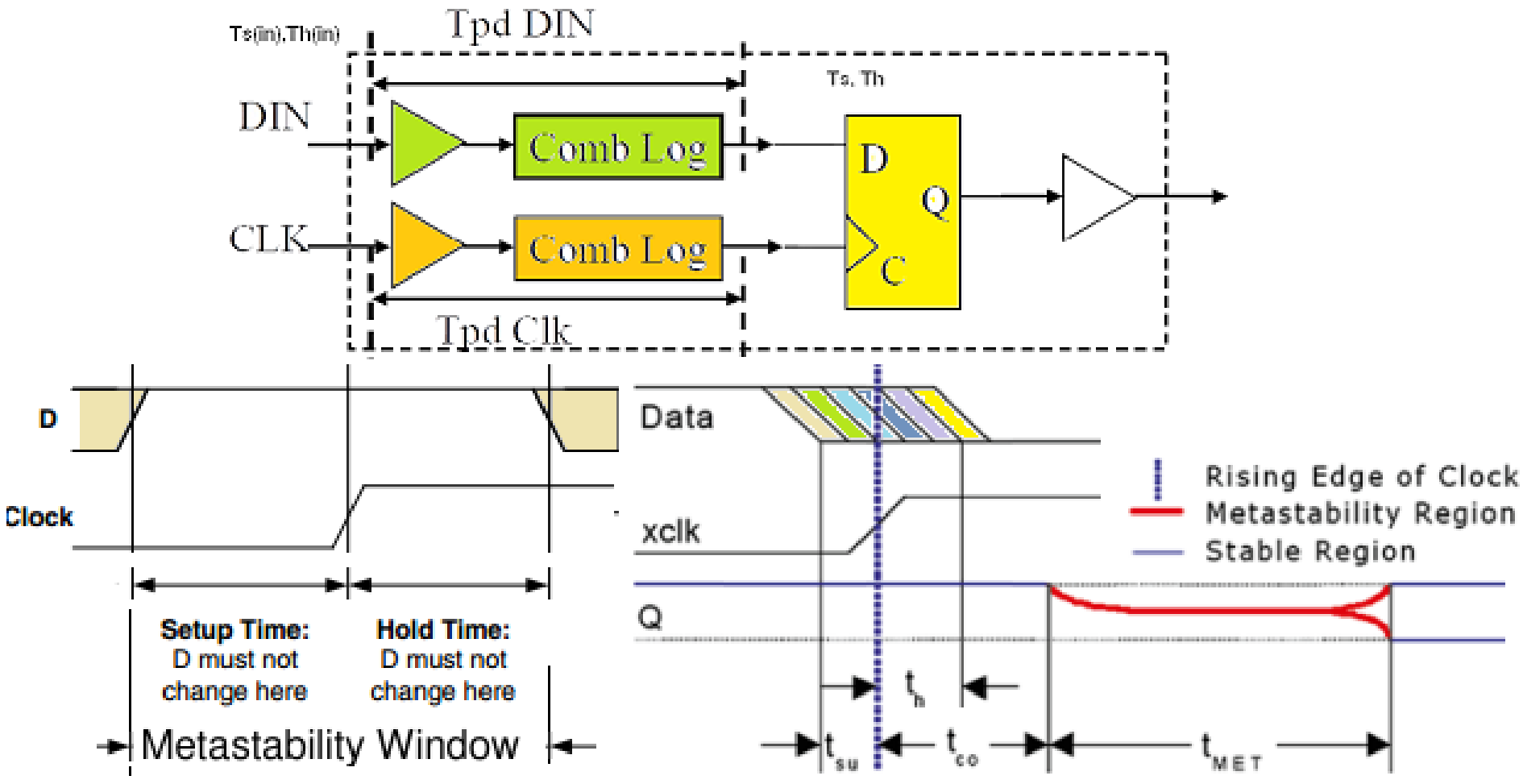


Metastability

Setup Time and Hold Time

- Metastability:Result of violation of setup and hold times of a flip flop.
- Setup Time: The time required for data input to remain stable prior to arrival of clock pulse.
- Hold Time: The time required for data input to remain stable after the arrival of clock pulse.

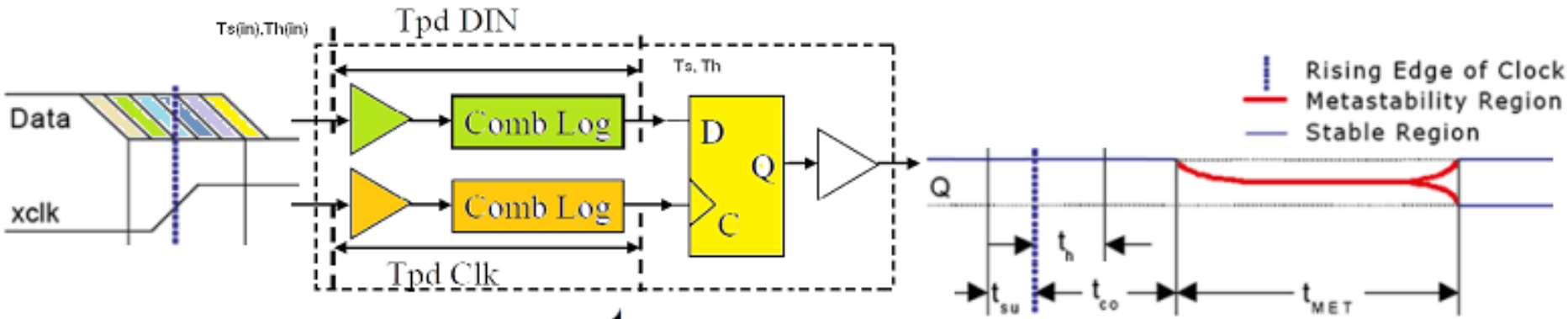
Setup Time and Hold Time

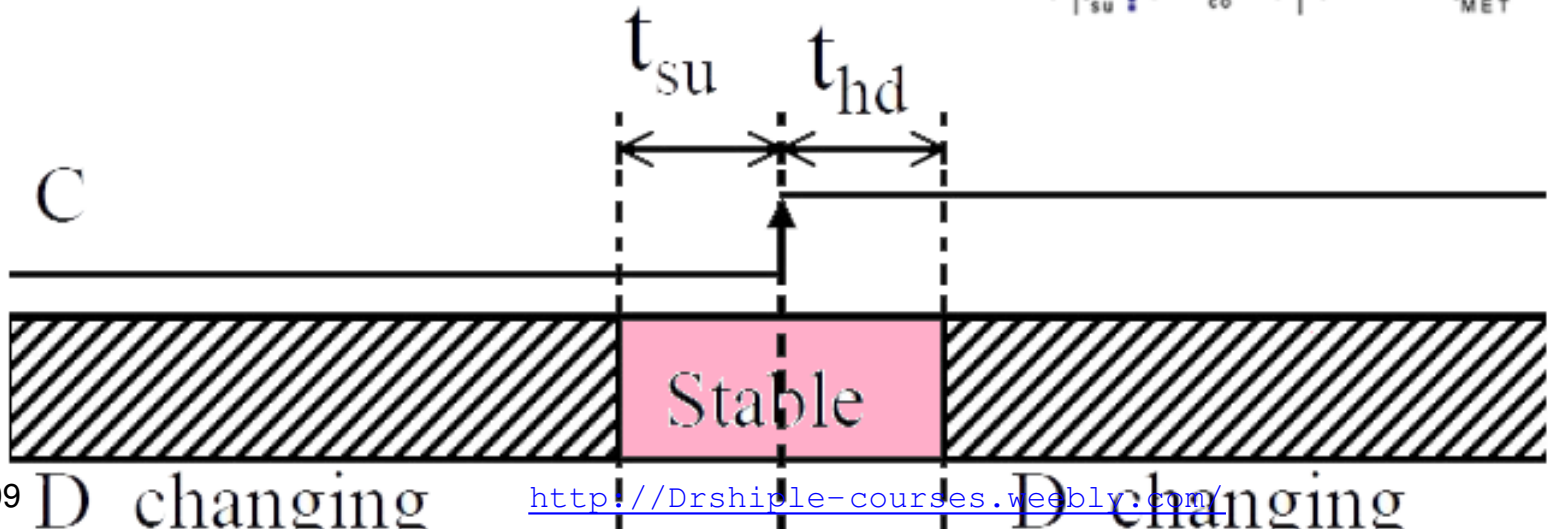


Calculations

$$T_{Set} \leqslant (T_{pdCLK})_{min} - (T_{pdDin})_{max}$$
$$T_{Hold} \leqslant (T_{pdDin})_{min} - (T_{pdCLK})_{max}$$

calculation

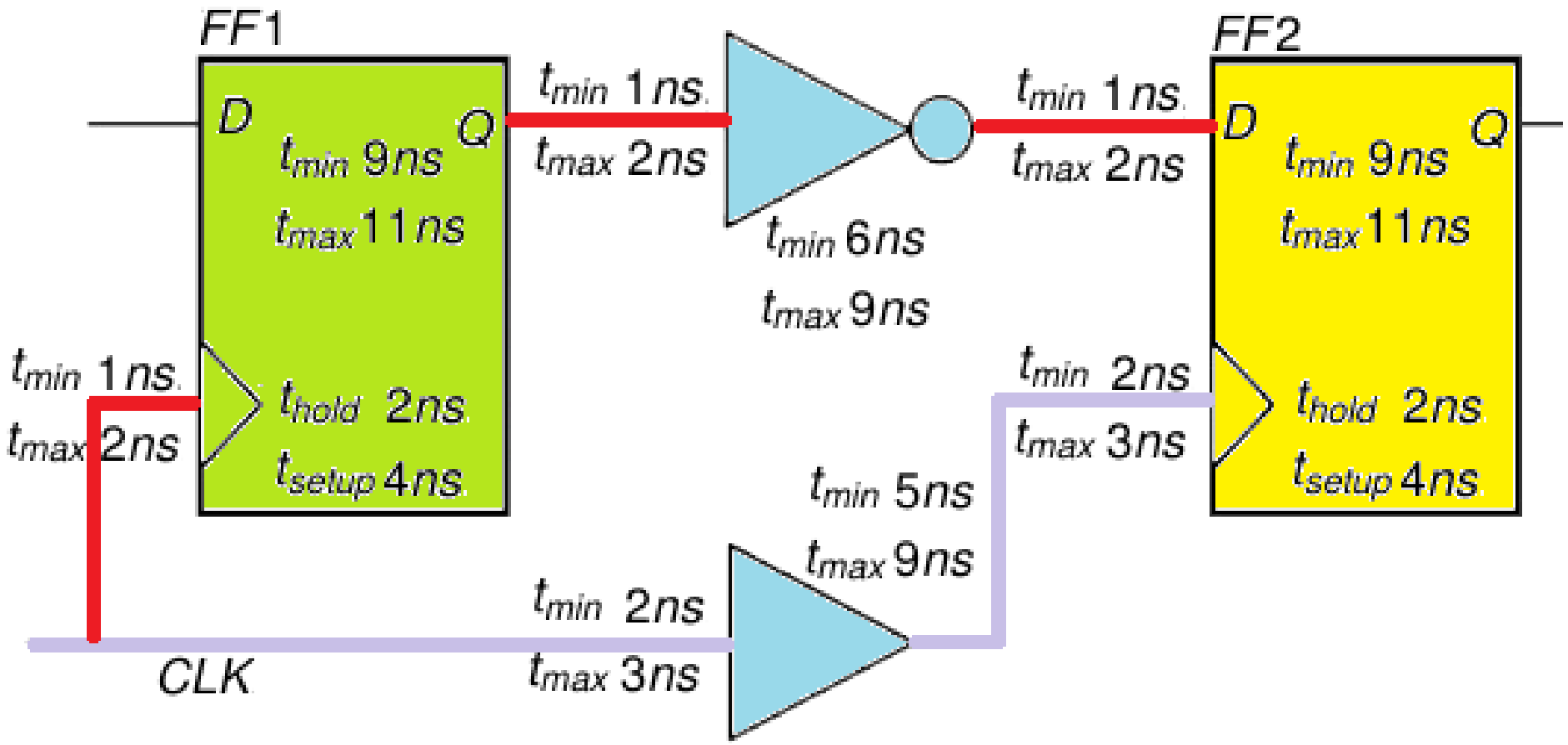




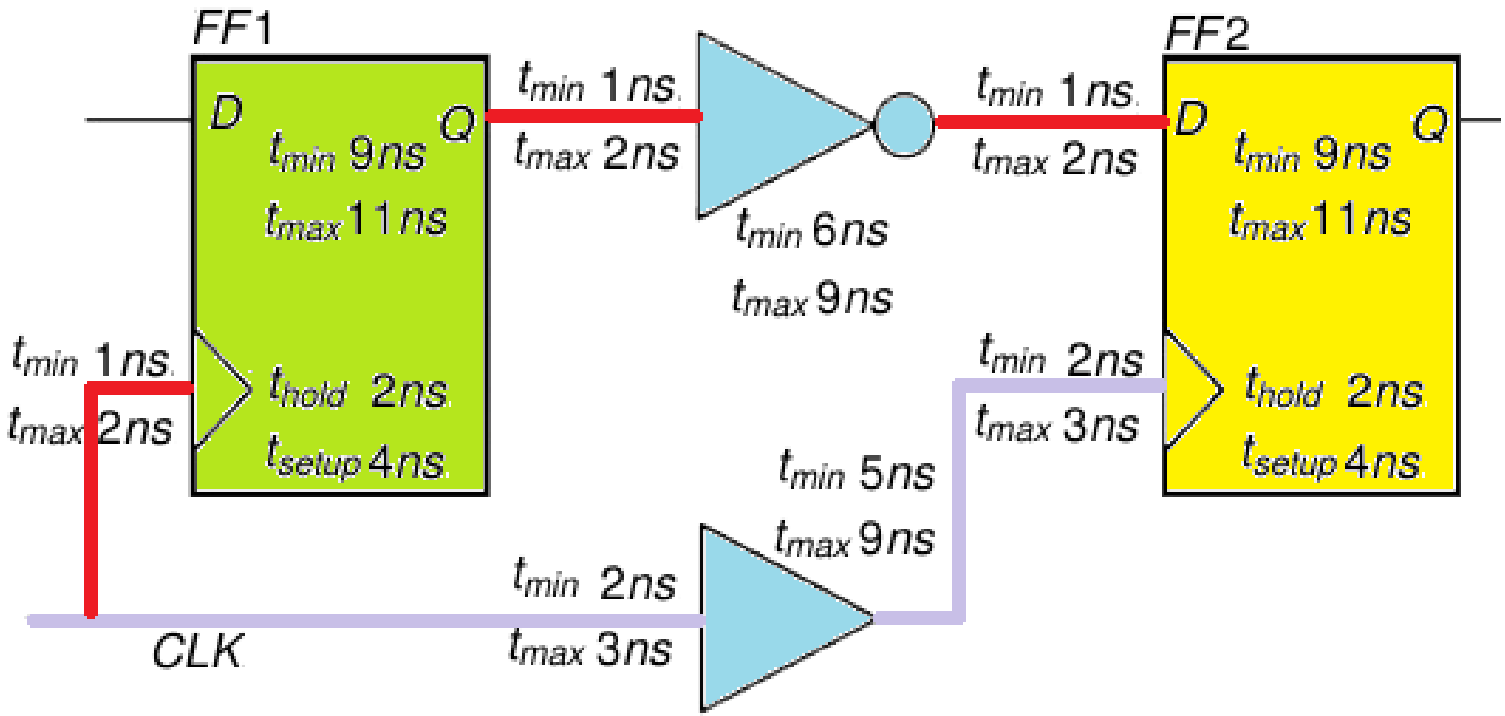
Example 2:

Calculate

System setup and hold times, for given path delays



Example 2:

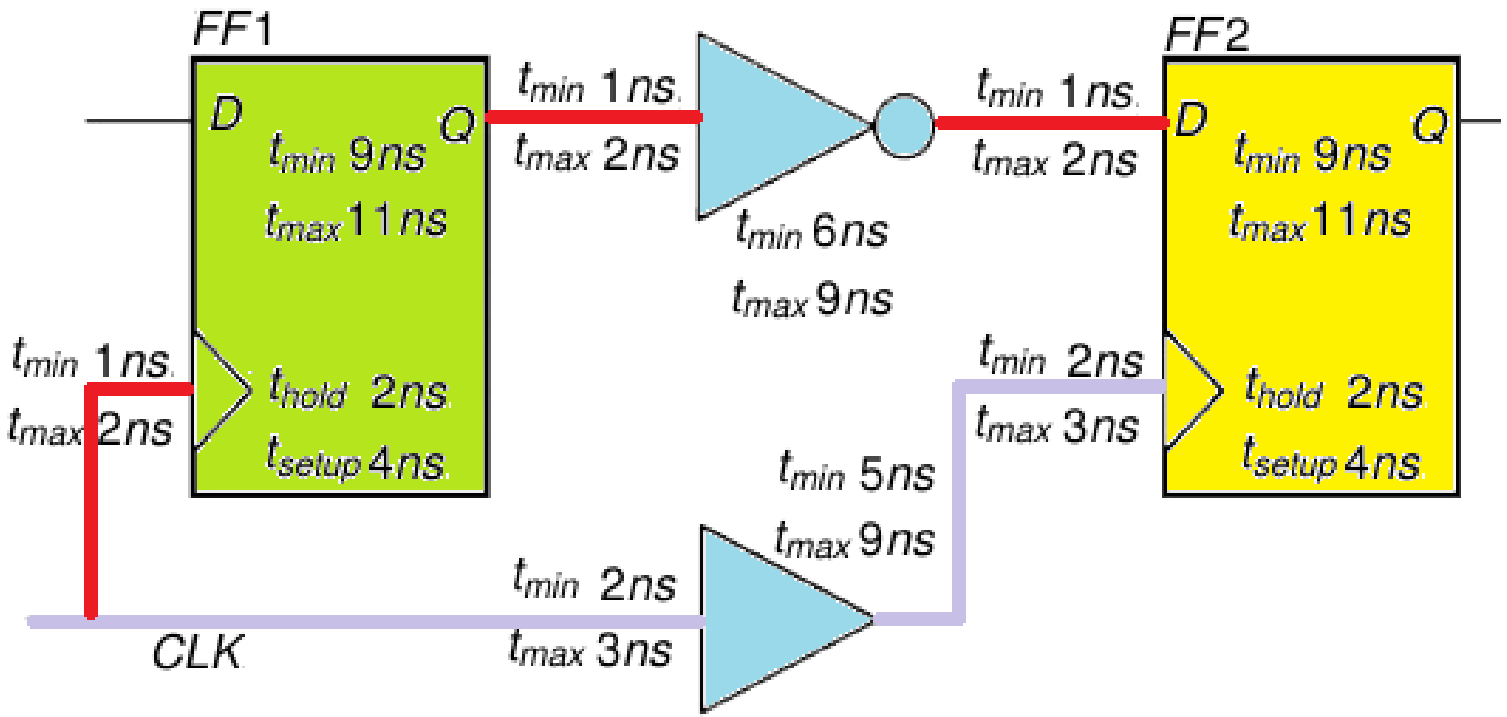


$$Data\_path(max) = 2 + 11 + 2 + 9 + 2 + 4 = 30ns$$

$$Clock\_period(min) = 30ns$$

$$Max\_Frequency = 1/30 = 33.3MHz$$

Example 2:

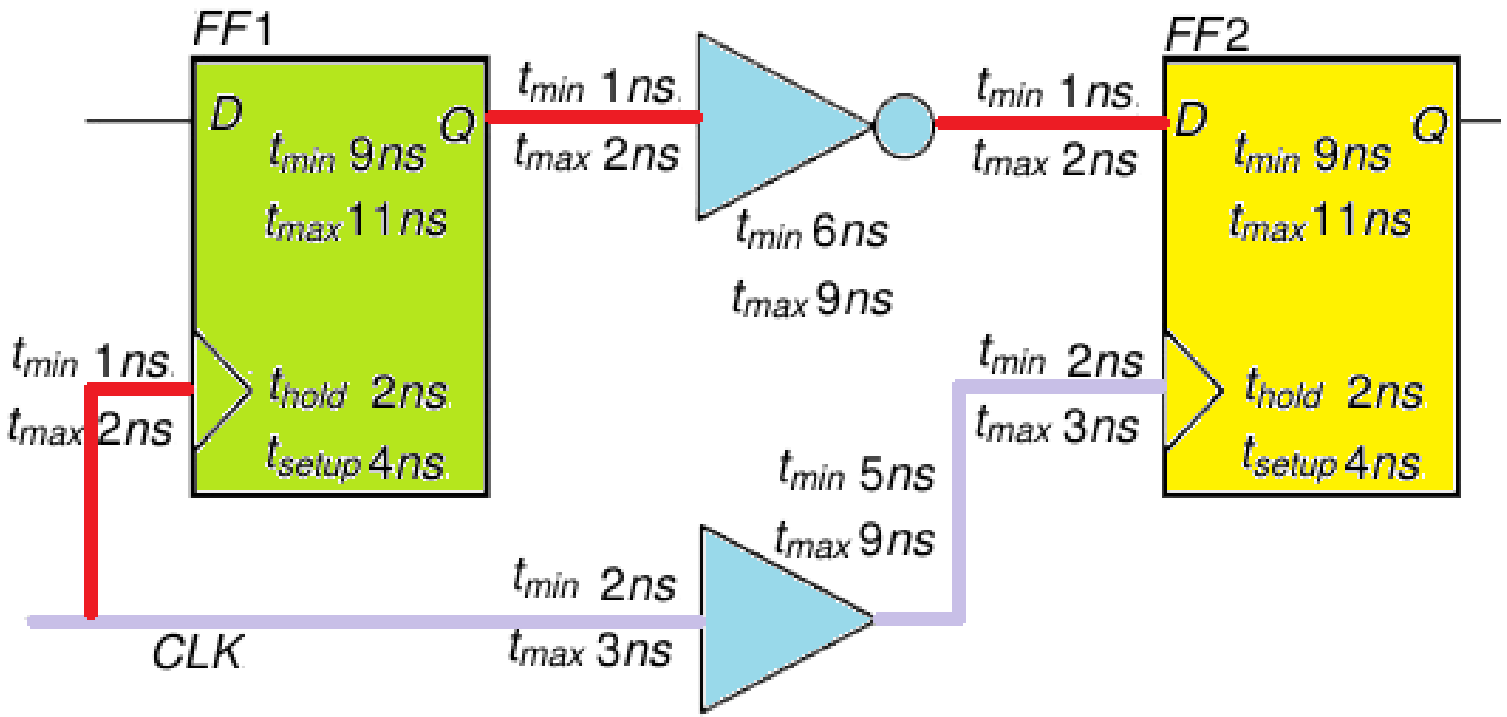


$$Data\_path(max) = 2 + 11 + 2 + 9 + 2 + 4 = 30ns$$

$$Clock\_period(min) = 15ns + 2 + 5 + 2 = 24$$ clk period=15

data lag clock by 6 ns (violation)

Example 2:



$$Data\_path(min) = 1 + 9 + 1 + 6 + 1 = 18nsns$$

$$Clock\_period(max) = 3 + 9 + 3 + 2 = 17ns$$

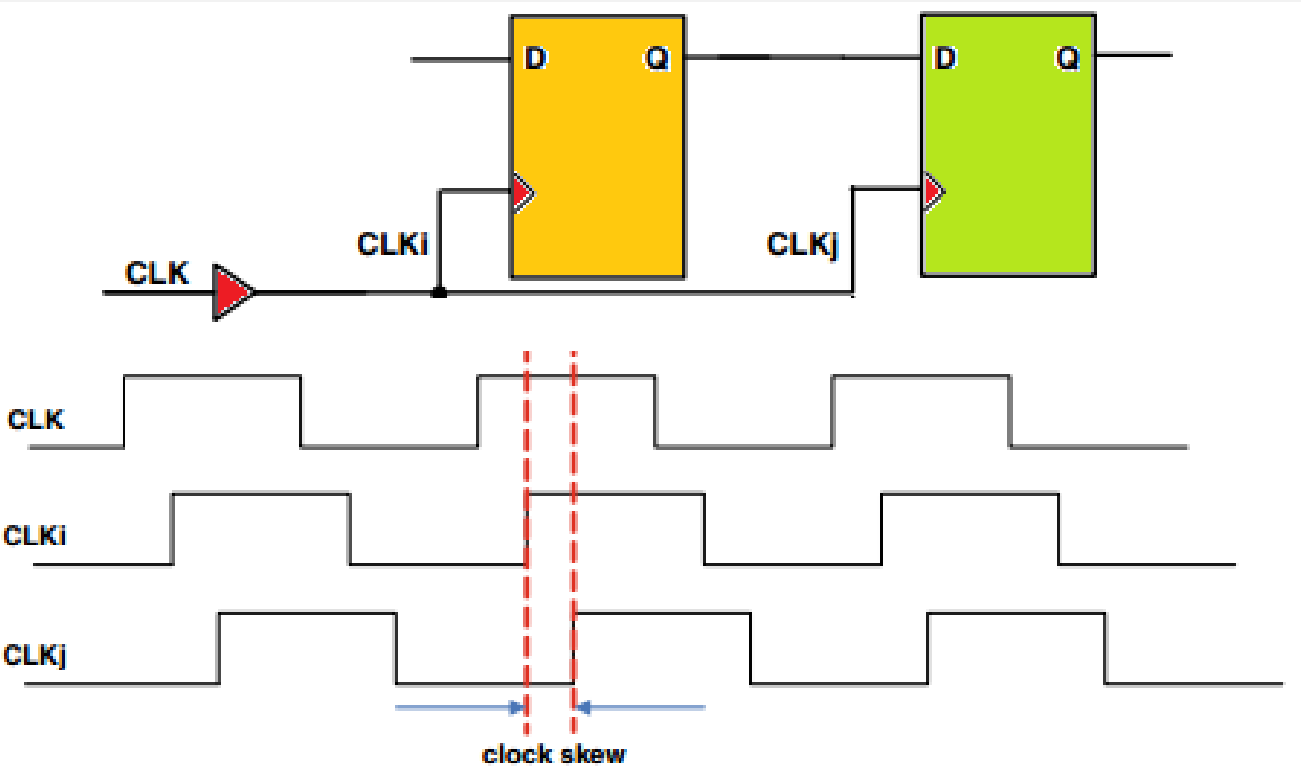
data lag clock by 1 ns (no holdviolation)

Avoiding Metastability

- When the input signal is an asynchronous signal.
- When the clock skew/slew (rise/fall times) is higher than the tolerable limit.
- When signals cross the domains working at two different frequencies or with same frequency but different phase and skew.
- When the combinational delay is such that the Flip Flop data input changes in the Metastability Window.

Clock Skew

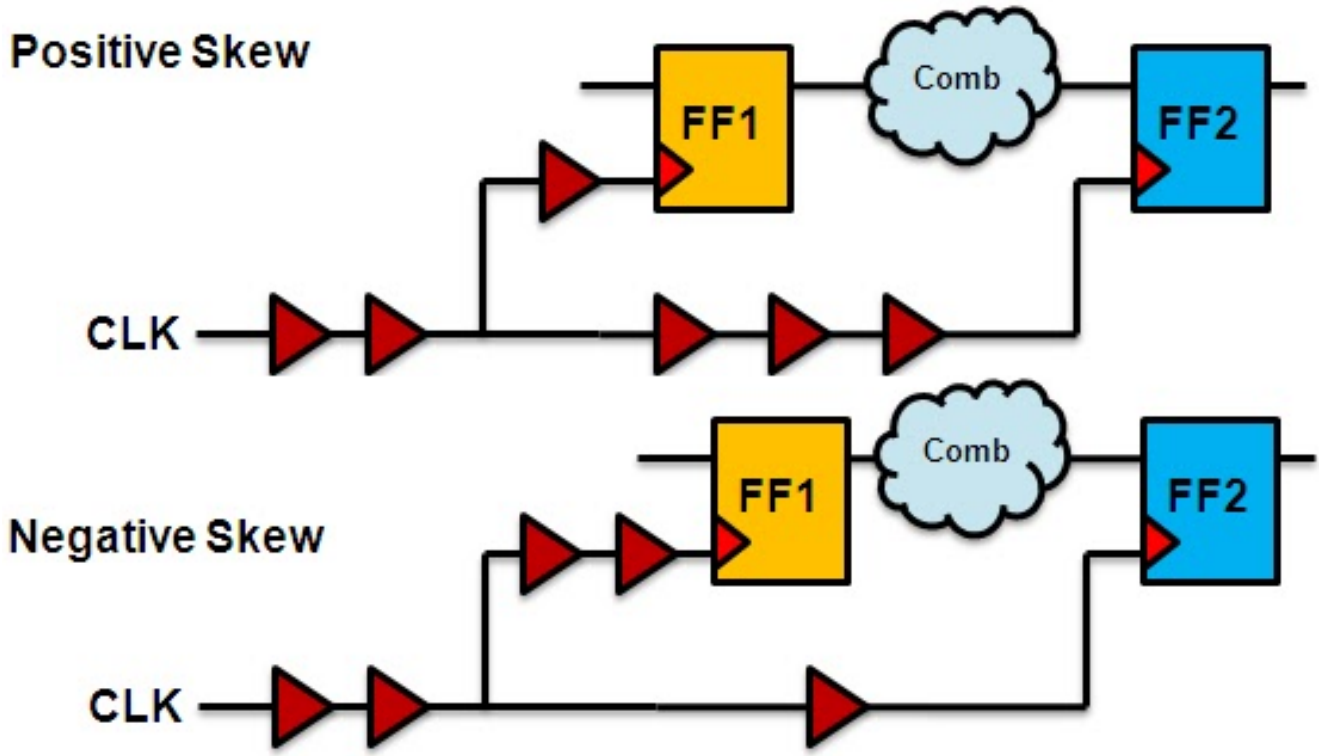
Definition



Clock skew is a phenomenon in synchronous circuits in which the clock signal arrives at different components at different times. Due to:

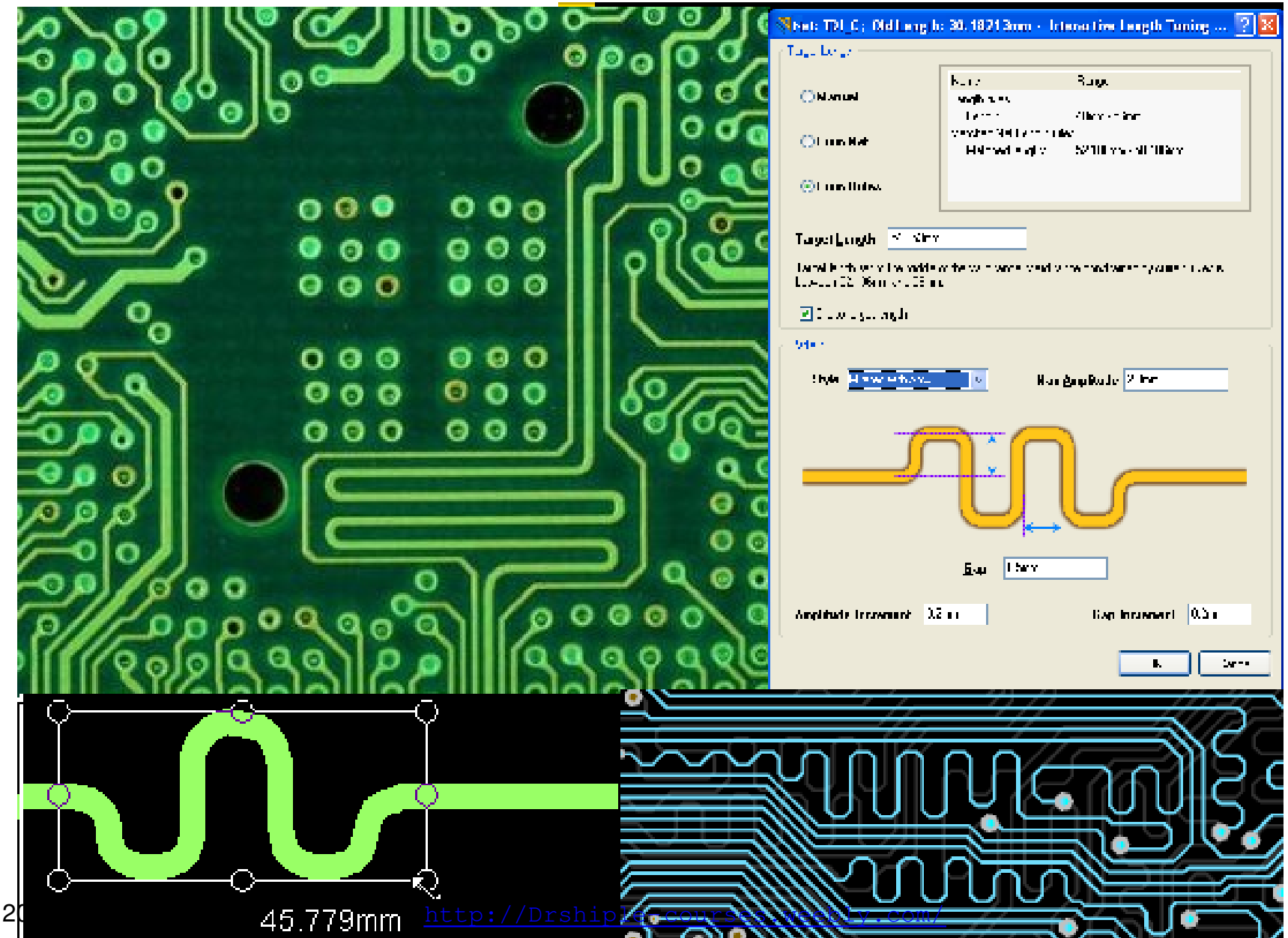
- Wire-interconnect length
- Temperature variations
- Capacitive coupling
- Material imperfections and differences in input capacitance on the clock inputs

Positive vs Negative Skew

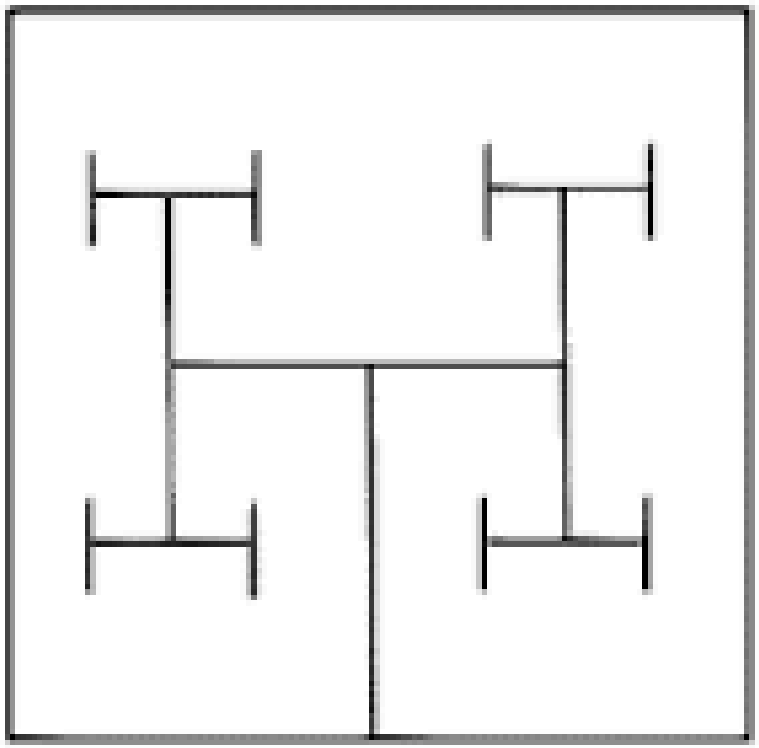


$CLK, D, Q, t_{hold} = 2ns, t_{setup} = 4ns$

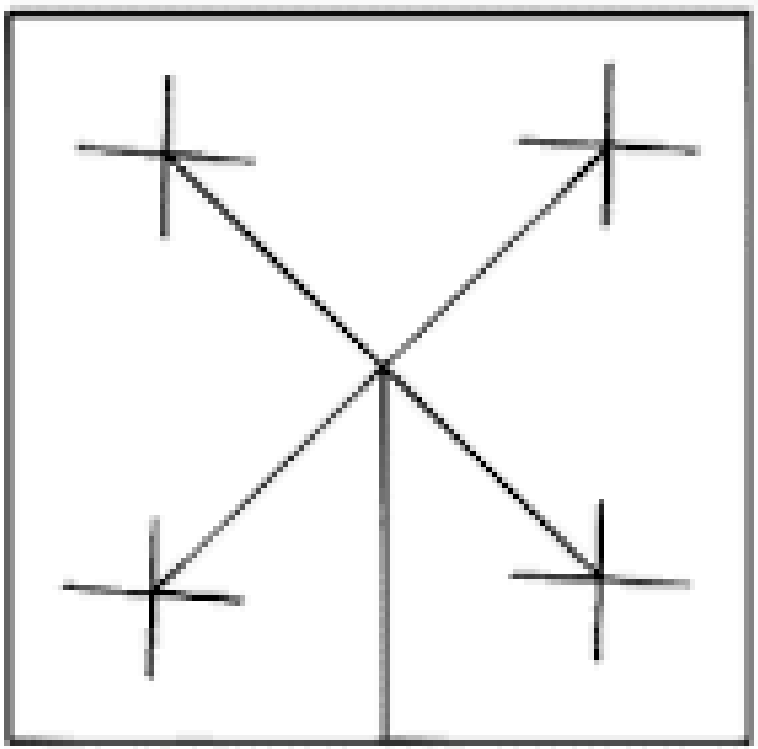
Adding Delay in Data Path



H-Tree

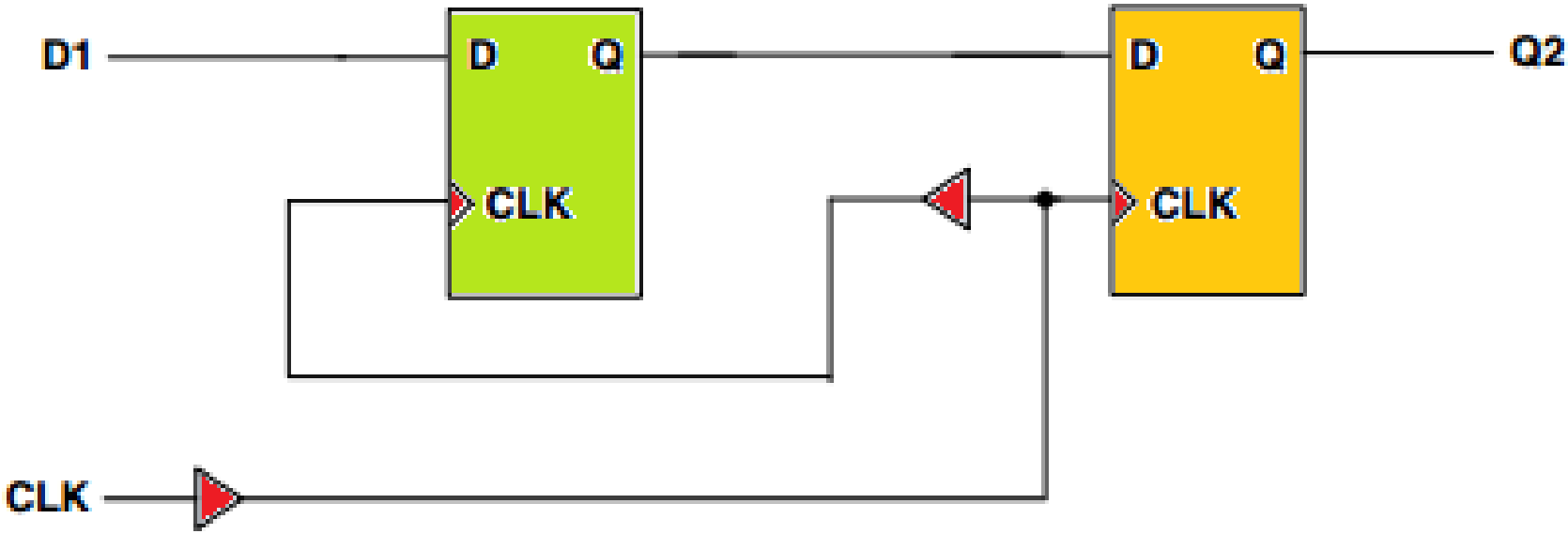


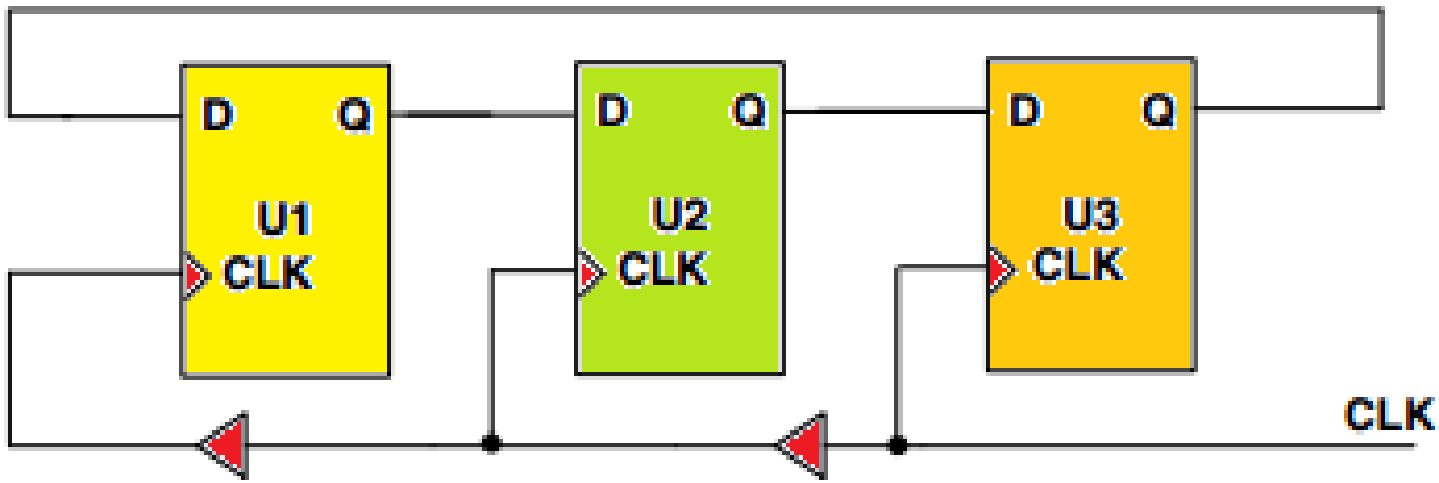
H - Tree



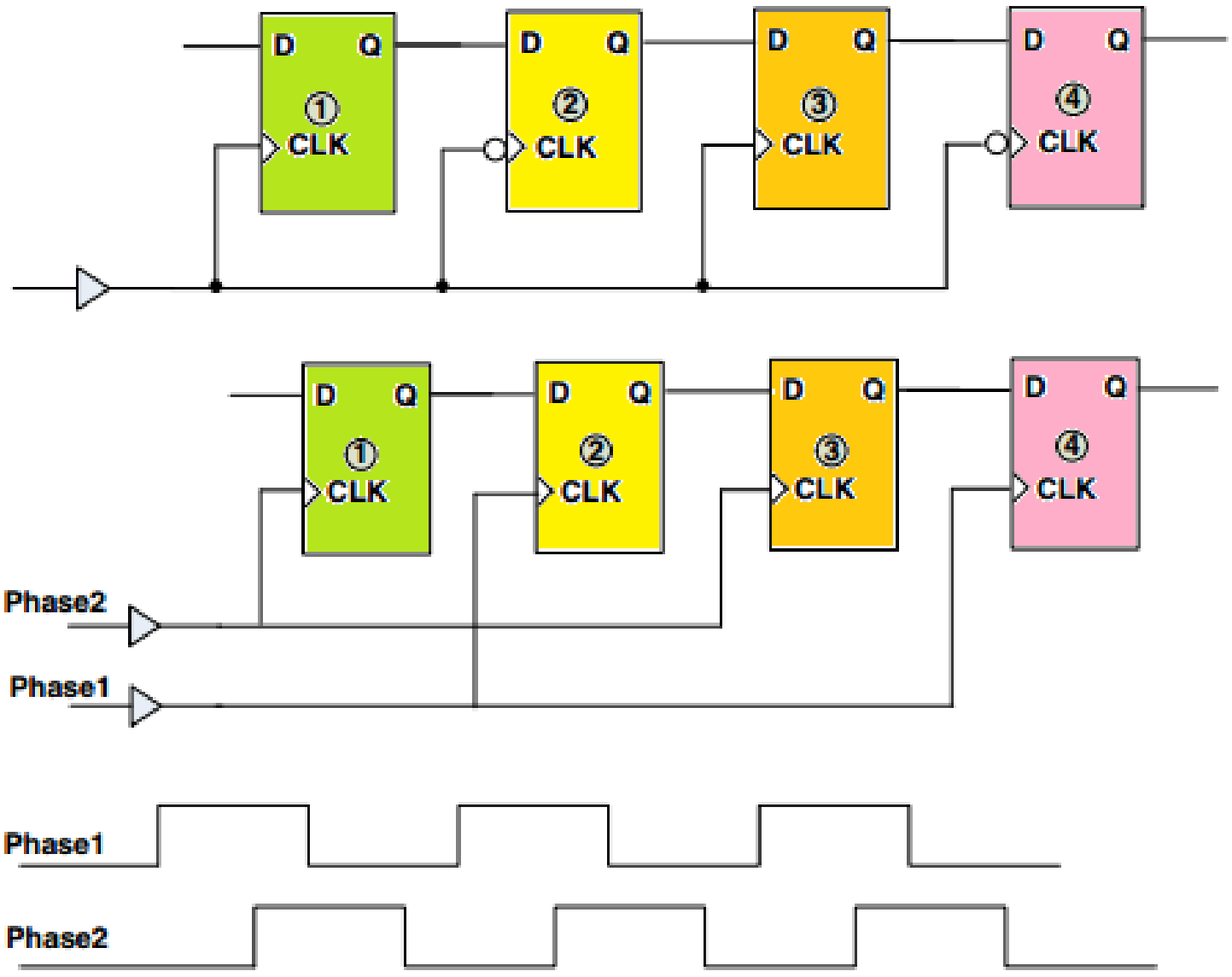
X - Tree

Clock Reversing





Clocking on Alternate Edges/Alternate Phases



Digital Clock Manager (DCM)

DCMs have the following applications:

- Multiplying or dividing an incoming clock (which can come for outside the FPGA or from a Digital Frequency Synthesizer).
- Making sure the clock has a steady duty cycle(50%).
- Adding a phase shift with the additional use of a Delay-locked loop.
- Eliminating clock skew within an FPGA design.

References

Ref.

- static time analysis
  http://www.vlsi-expert.com/2011/03/static-timing-a