Field Programmability

Dr. M. Shiple

Advanced Microprocessor (EEC 209), 2017

Outline

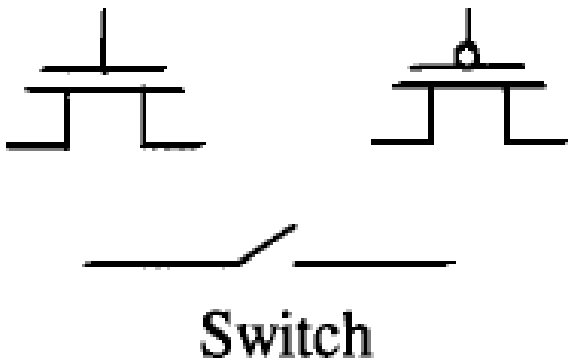
1. **History of programmable Logic**
2. **SRAM**
3. **ROM**
   - One time Programing (OTP)

History of programmable Logic


ليس سقوط المرء فشلاً وإنما الفشل أن يبقى حيث سقط
I can accept failure, Everyone fails at something.
But I cannot accept not trying.
- Michael Jordan

Concepts

- Field programmability is achieved through switches (Transistors controlled by memory elements or fuses)
- Switches control the following aspects:
  - Interconnection among wire segments
  - Configuration of logic blocks
- Distributed memory elements controlling the switches and configuration of logic blocks are together called "Configuration Memory"



Technology of Programmable Elements

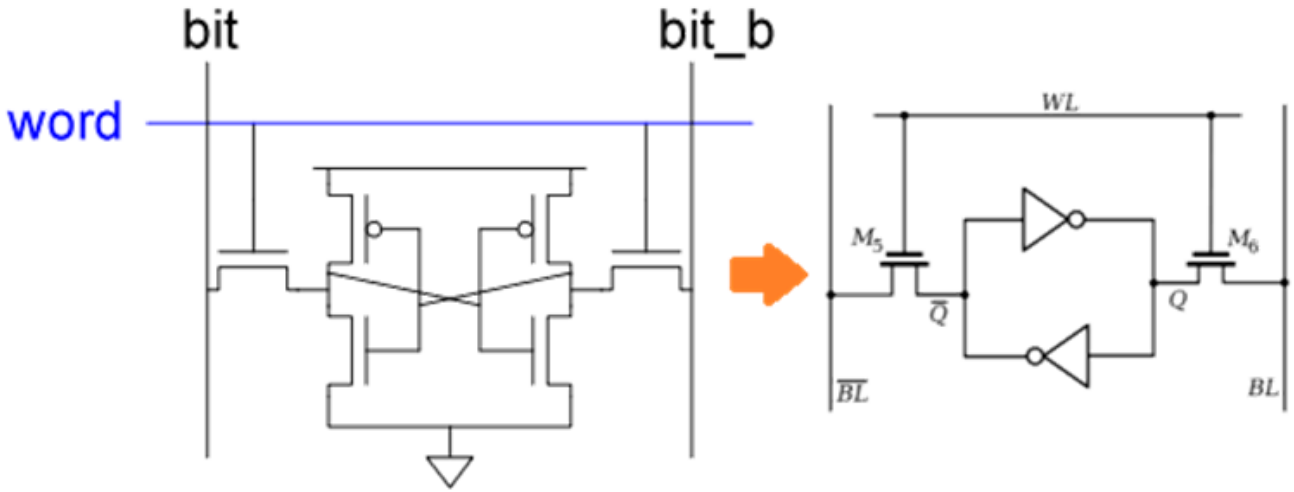
- Vary from vendor to vendor. All share the common property: Configurable in one of the two positions: 'ON' or 'OFF'
- Can be classified into three categories:
  - SRAM
  - Fuse
  - EPROM/EEPROM/Flash

Desired properties:

- Minimum area consumption.
- Low *on* resistance; High *off* resistance.
- Low parasitic capacitance to the attached wire.
- Reliability in volume production.

SRAM

SRAM Programming Technology(6T Cell)



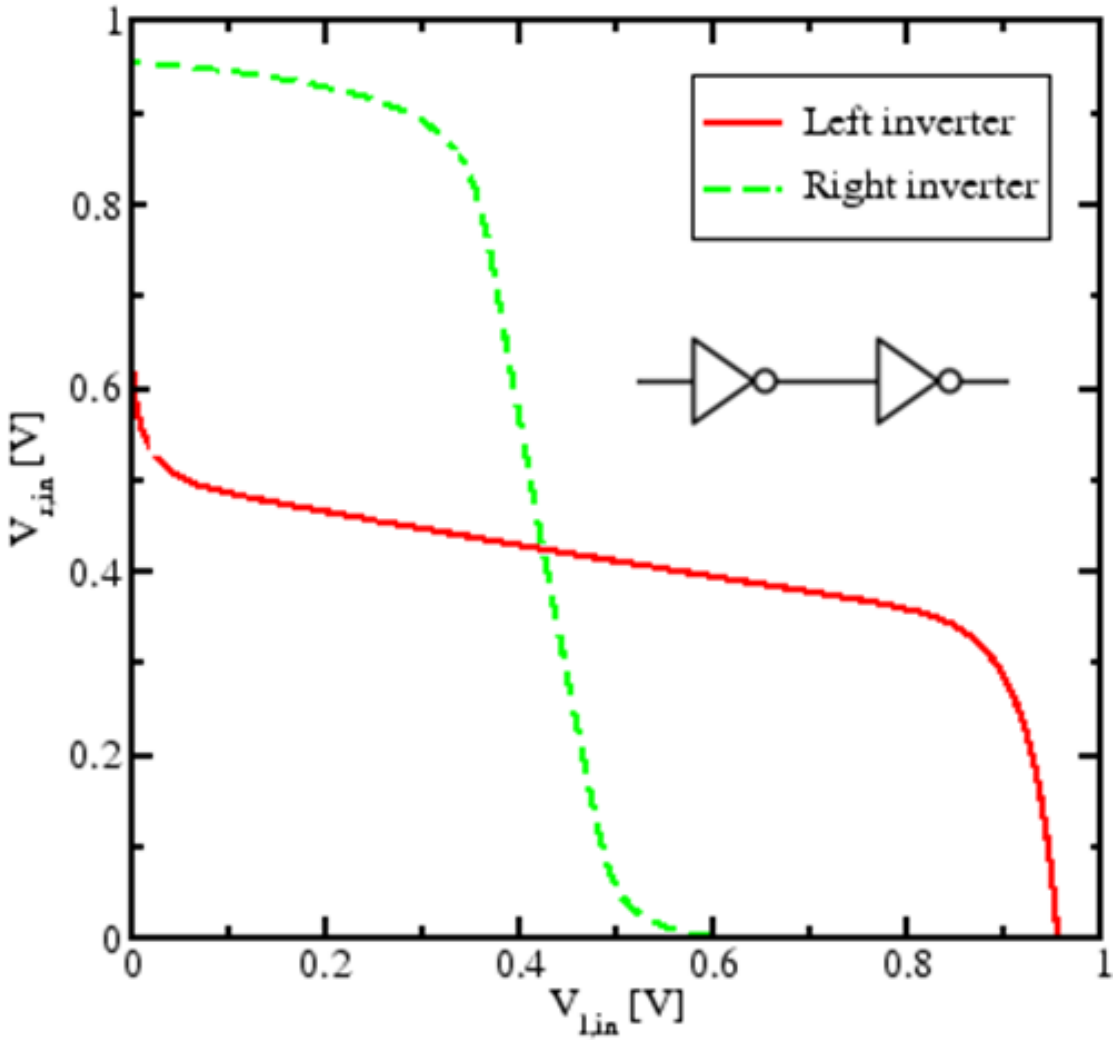
Read:

- Precharge BL, .
- Raise wordline.

Write:

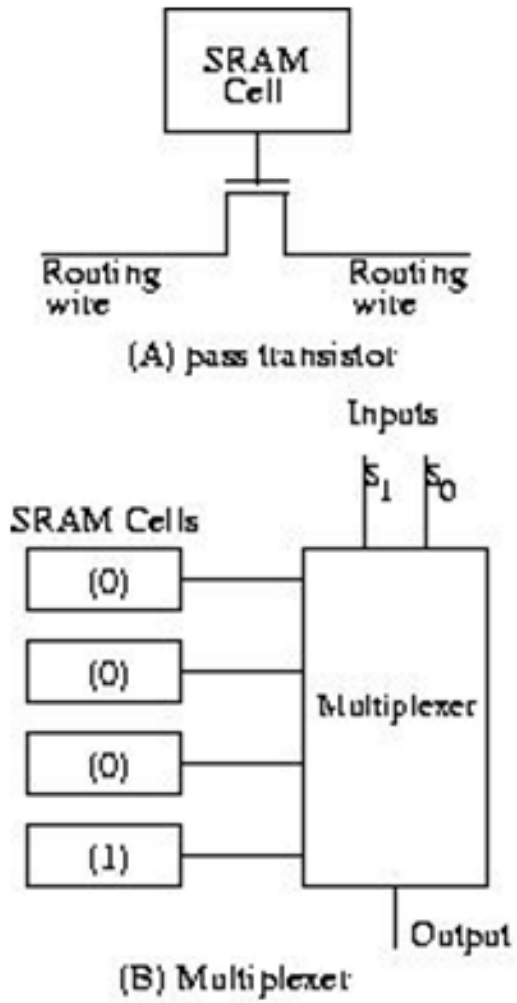
- Drive data onto bit,.
- Raise wordline.

Regenerative property:



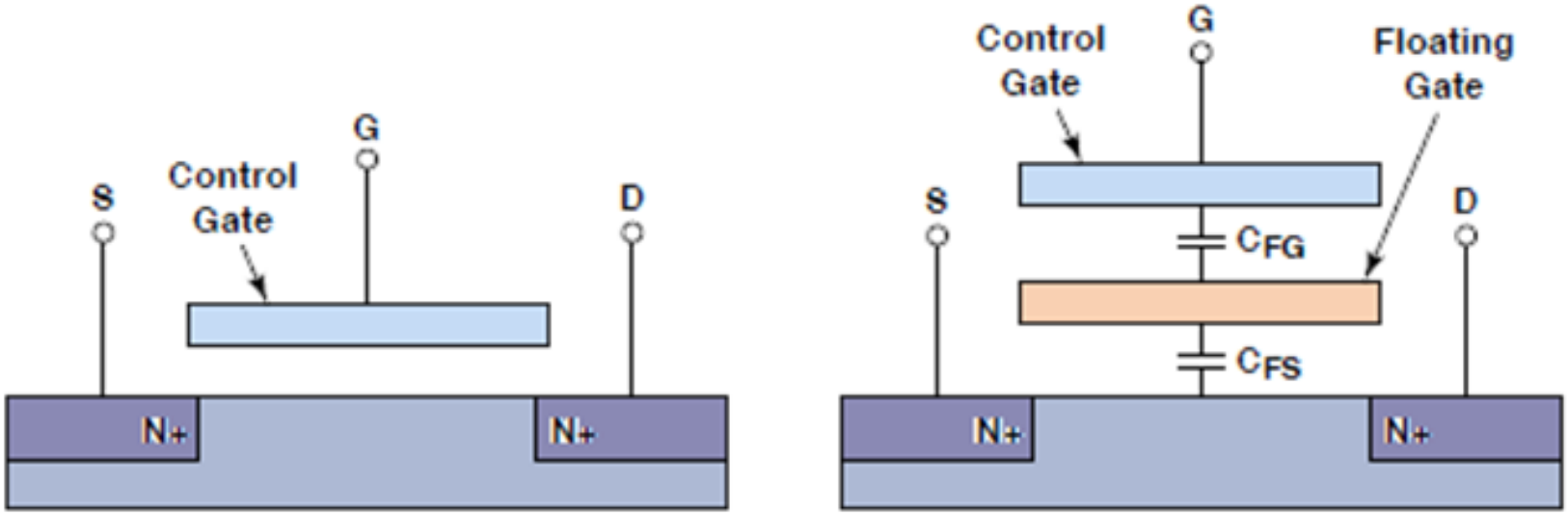
Pros and Cons

- Employs SRAM (Static RAM) cells to control pass transistors and/or transmission gates
- SRAM cells control the configuration of logic block as well
- Volatile:
  - Needs an external storage
  - Needs a power-on configuration mechanism
- In-circuit re-programmable
- Occupies relatively larger area



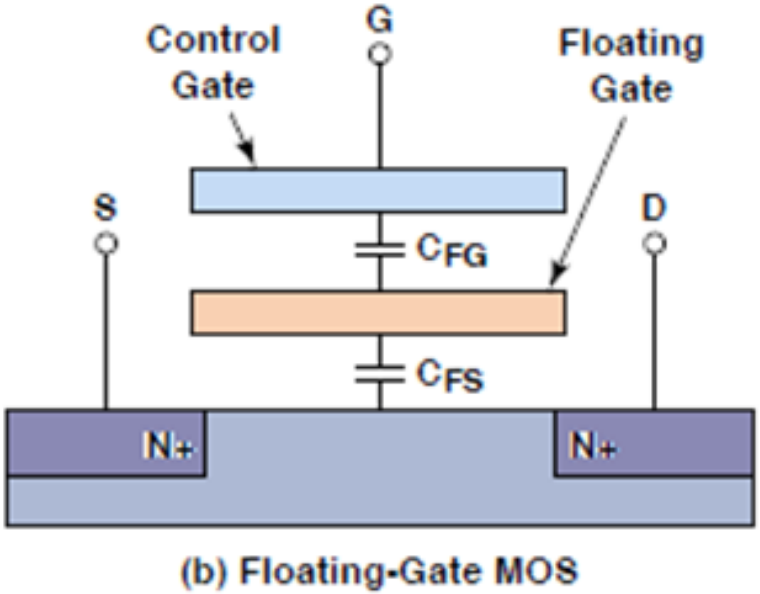
ROM

EPROM - EEPROM - Flash

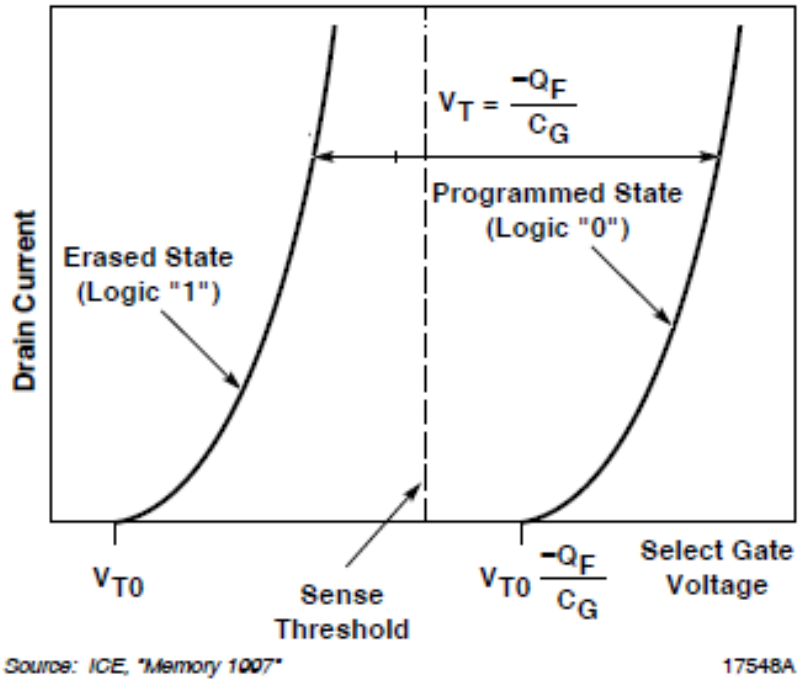


- Two gates: Floating and Select
- Normal mode:
  - No charge on floating gate
  - Transistor behaves as normal n-channel transistor
- Floating gate charged by applying high voltage
  - Threshold of transistor (as seen by gate) increases
  - Transistor turned off permanently
- Re-programmable by exposing to UV radiation

Floating Gate



(b) Floating-Gate MOS

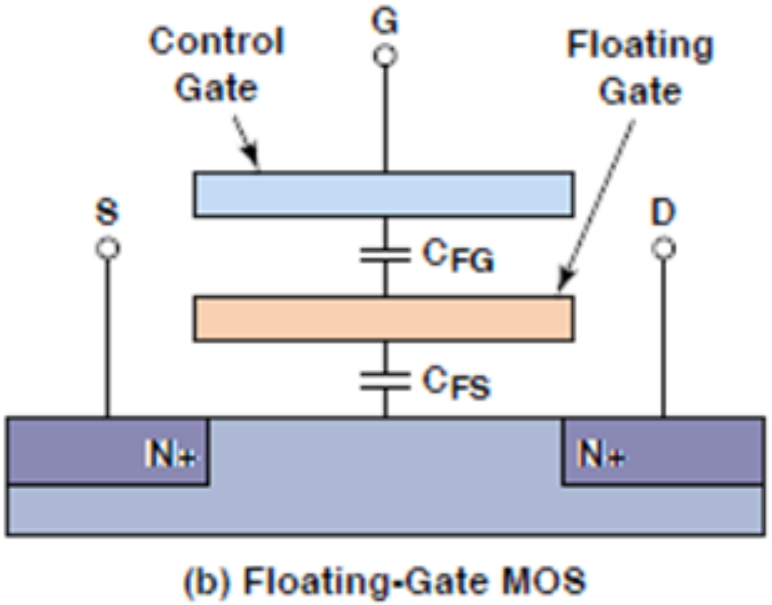


$$(V_G - V_F)C_{FG} + (0 - V_F)C_{FS} - Q_F = 0$$

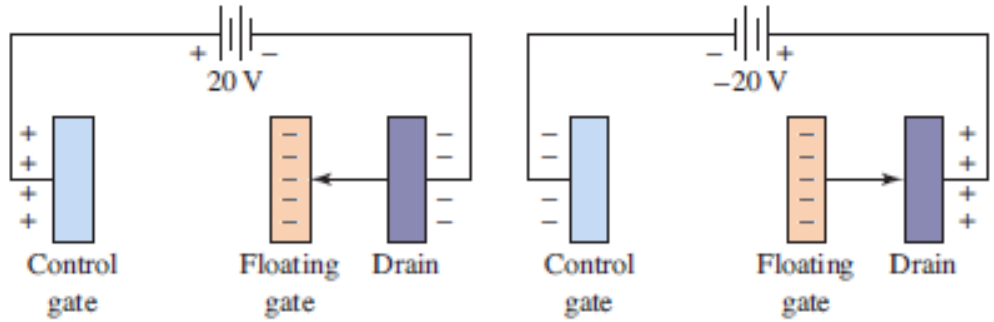
$$V_F = \frac{C_{FG}}{C_{FG}} V_G - \frac{1}{C_{FG} + C_{FS}} Q_F$$

$$\begin{cases} Q_F = 0 & \text{Normal MOSFET = Erased State = Logic 1} \\ Q_F \neq 0 & \text{Float MOSFET = programmed = Logic 0} \end{cases}$$

Floating Gate



(b) Floating-Gate MOS

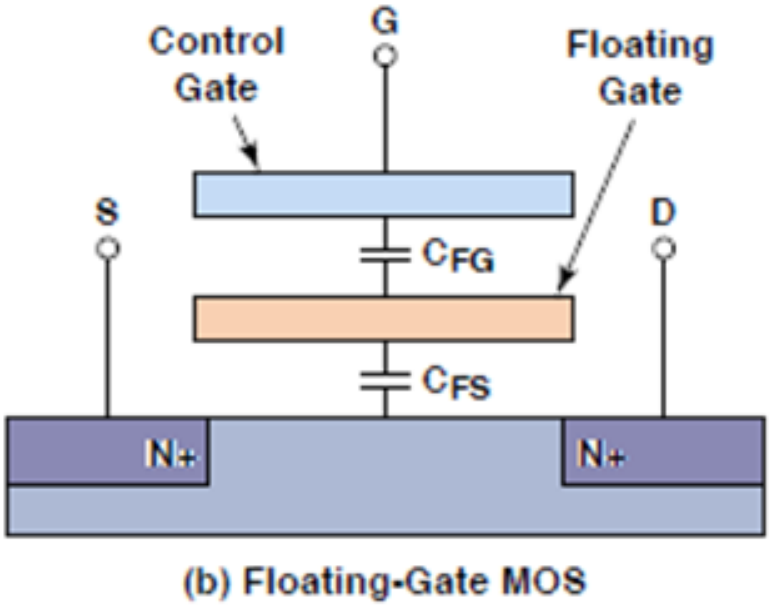


charging the floating gate; discharging the floating gate

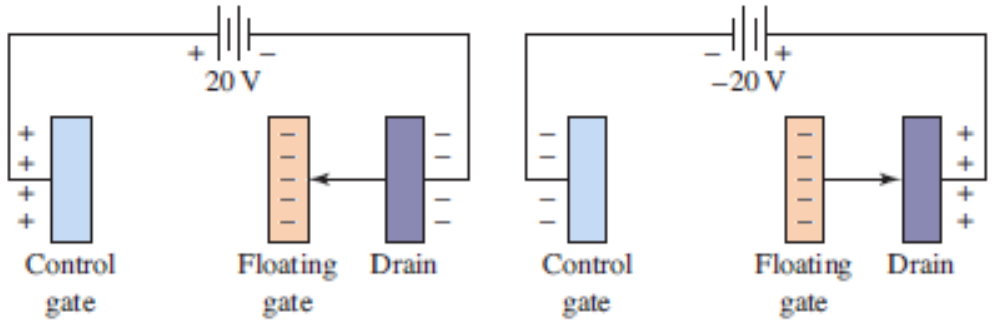
disadvantage:

- The entire memory must be erased before any reprogramming process.
- EPROM must be removed from the circuit during this operation.
- The whole entire memory will be erased by UV (one shot) .

Electrically Erasable Programmable ROM (EEPROM)



(b) Floating-Gate MOS



charging the floating gate; discharging the floating gate

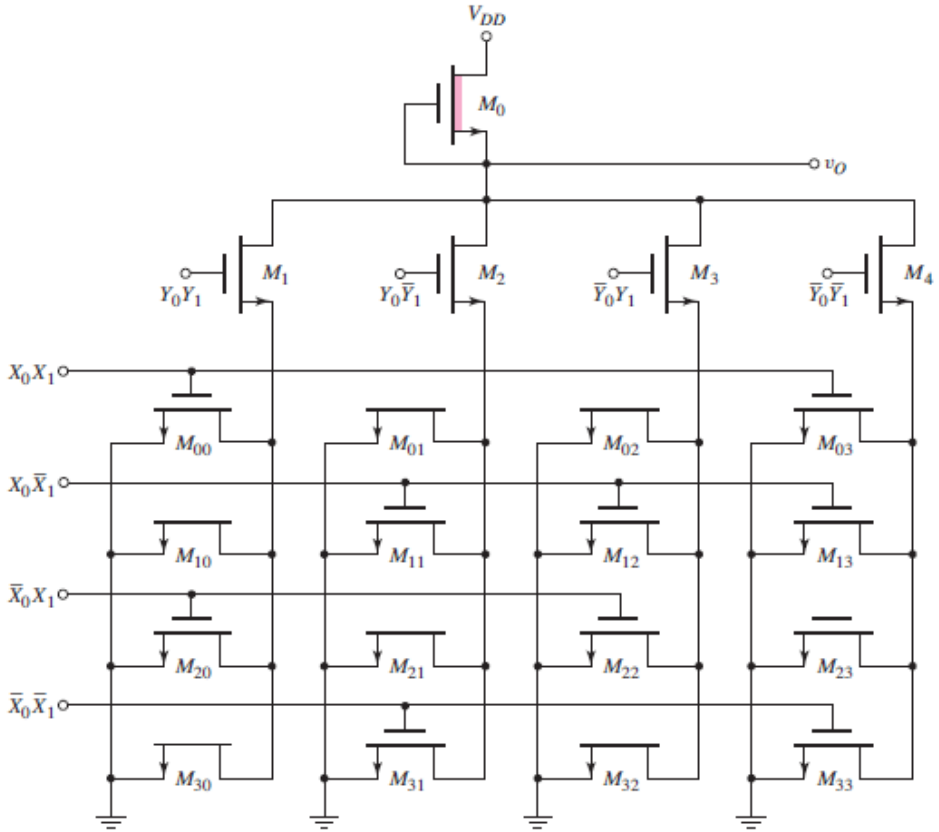
disadvantage:

- Each individual cell can be erased and reprogrammed without disturbing any other cell.
- EPROM must be removed from the circuit during this operation.
- The whole entire memory will be erased by UV (one shot) .

EPROM features

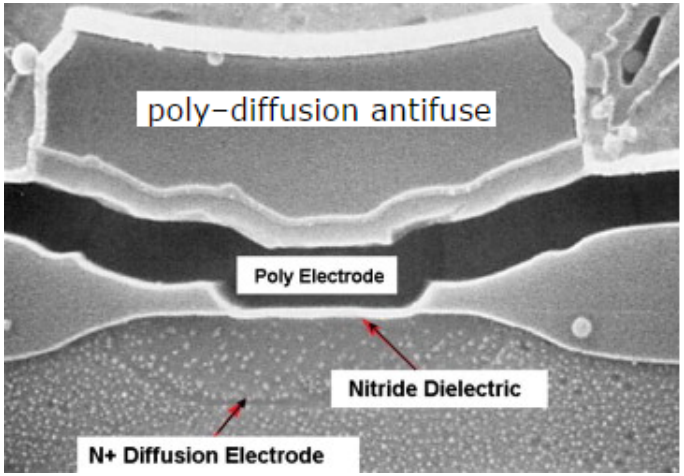
- No external storage mechanism
- Limited number of Re-programming ($\approx 10,000$ times) .
- Re-programming is a time consuming task.
- Uses non-standard CMOS process.

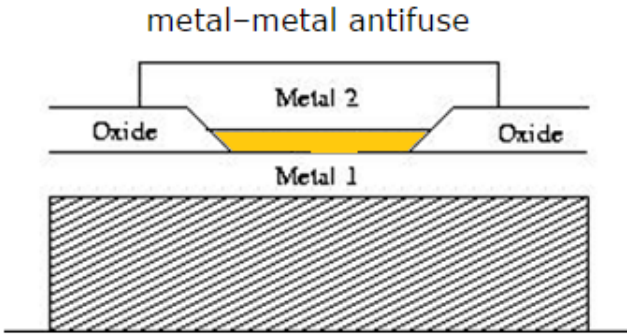
Mask-programmed ROM



Contacts to devices are selectively included or excluded in the final manufacturing process to obtain the desired memory pattern.

Anti-fuse





An antifuse is the opposite of a regular fuse

- Poly-diffusion anti-fuse: the high current density causes a large power dissipation in a small area, which melts a thin insulating dielectric between polysilicon and diffusion electrodes and forms a thin (about 20 nm in diameter), permanent, and resistive silicon link
- QuickLogic metal-metal anti-fuse. The link is an alloy of tungsten, titanium, and silicon with a bulk resistance

poly antifuse vs. metal antifuse

An anti-fuse is the opposite of a regular fuse

- The first is that connections to a metal-metal anti-fuse are direct to metal-the wiring layers.
- Metal layers makes it easier to use larger programming currents to reduce the anti-fuse resistance.
- Metal spacing design rules that limit how closely the anti-fuses may be packed.

ref

Umer Farooq, et al ,"Tree-Based Heterogeneous FPGA Architectures",2012 Springer, Chapter 2