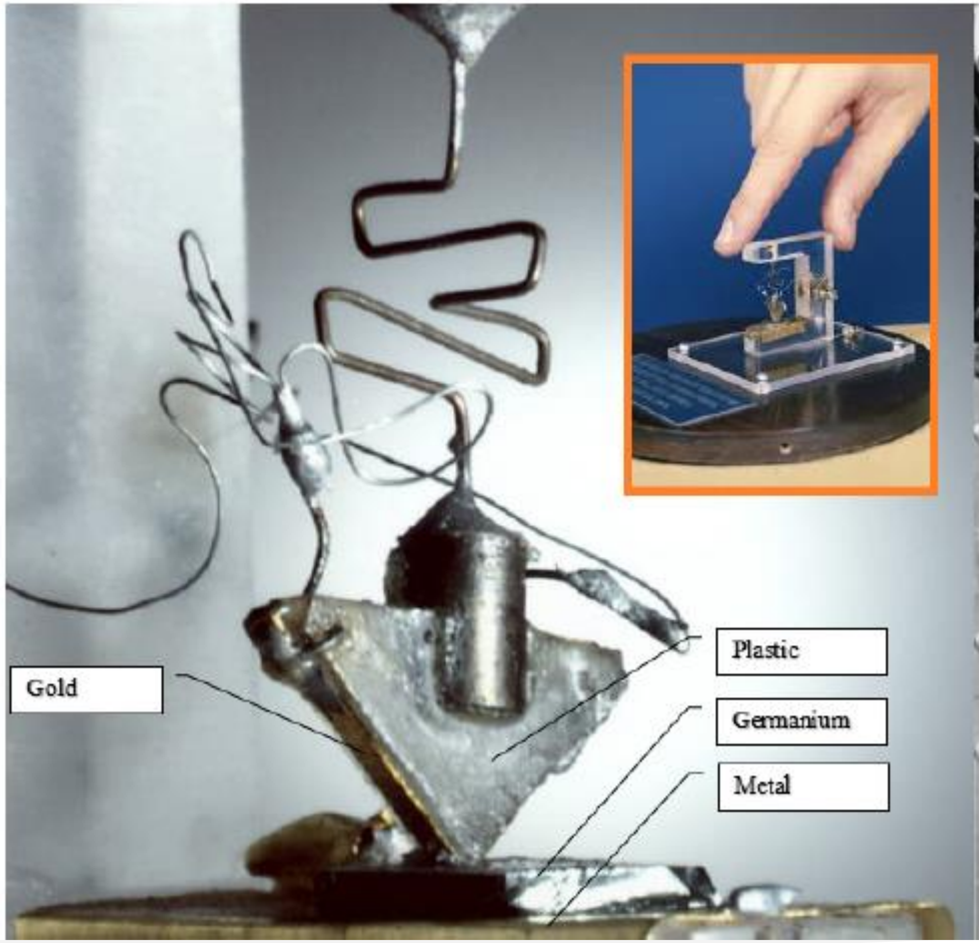
VLSI FABRICATION TECHNOLOGY

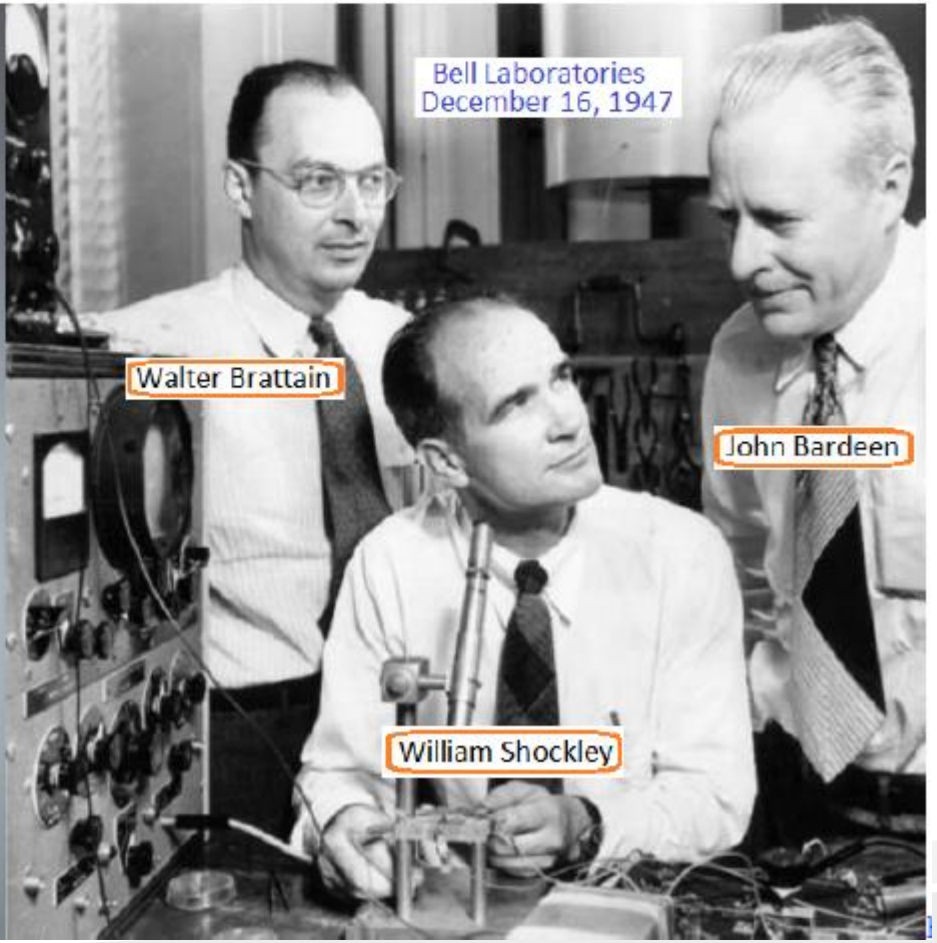
Dr. Mustafa Shiple

Agenda

- **Introduction**
- **Silicon IC processing**
  - Prearrangement
  - Doping Processes
  - Deposition Processes
  - Formation processes

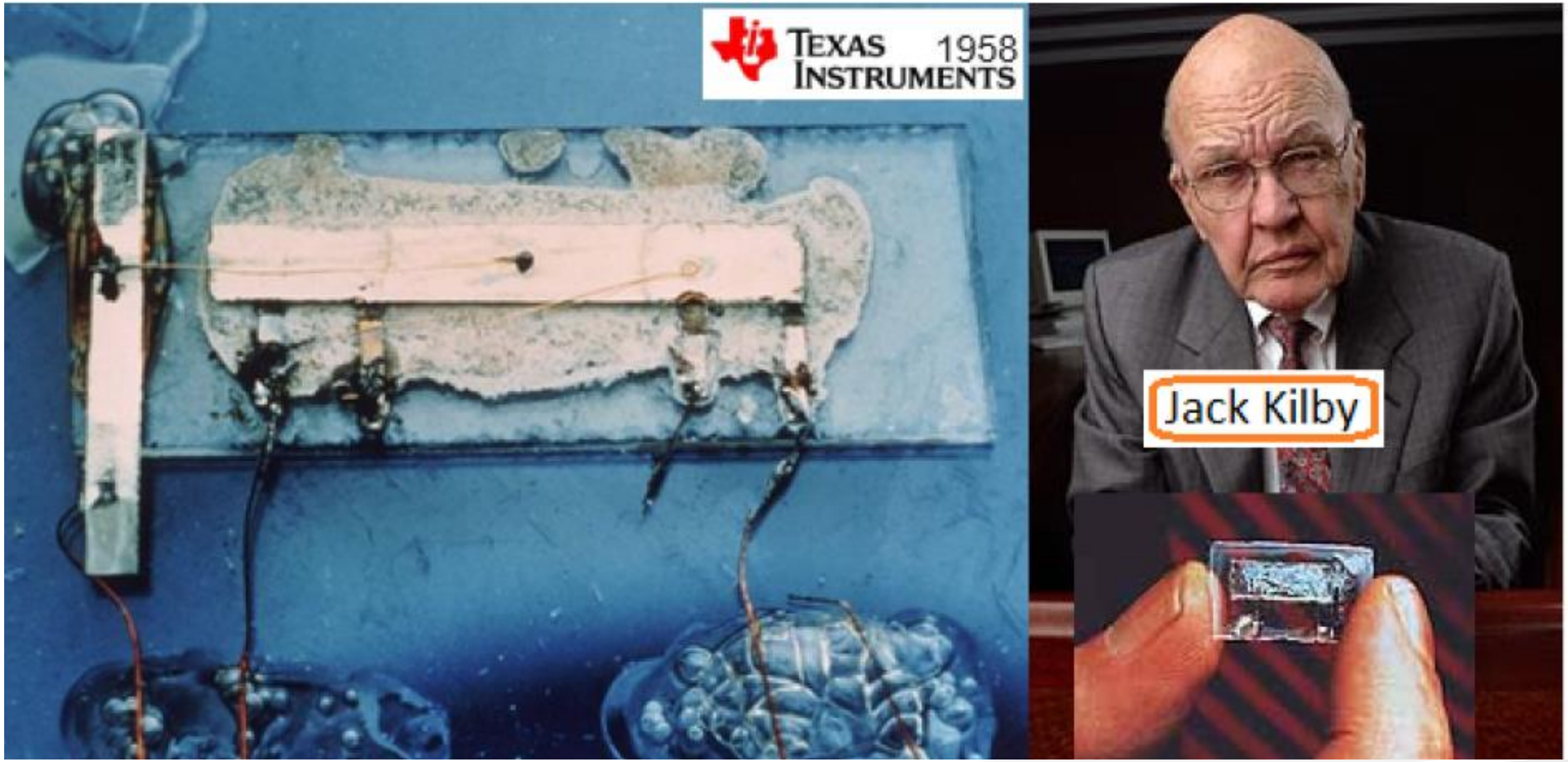
First Point Contact Transistor





www.pbs.org/transistor/science/events/pointctrans.html

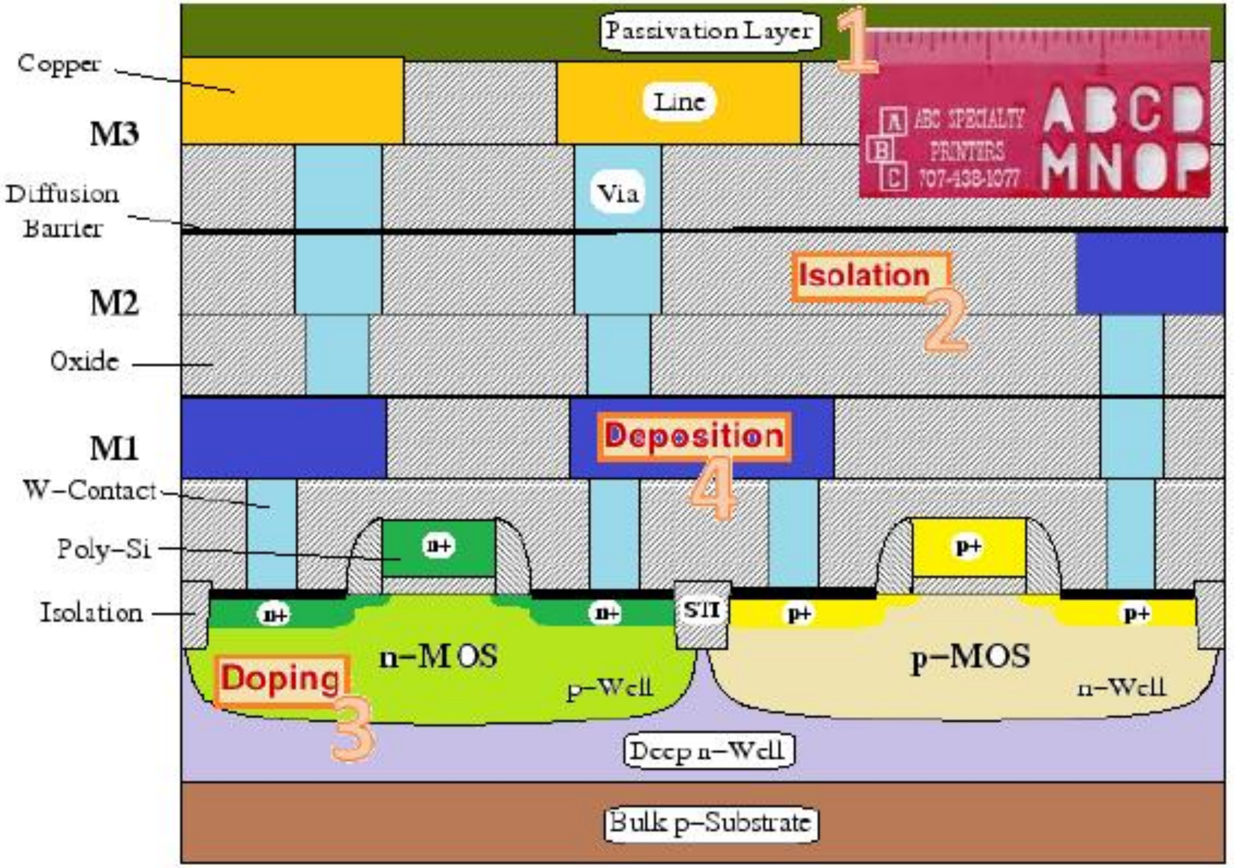
First integrated circuit

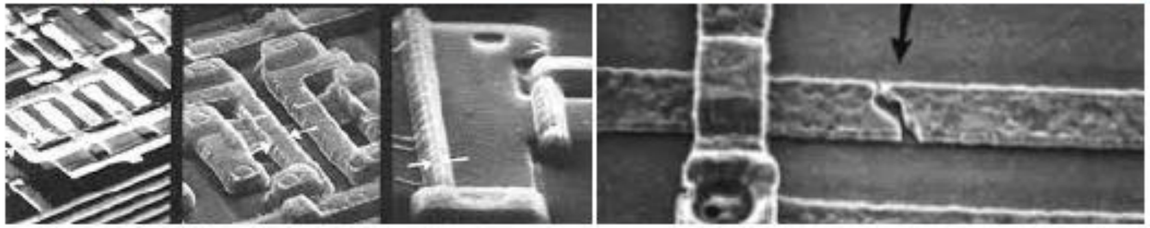


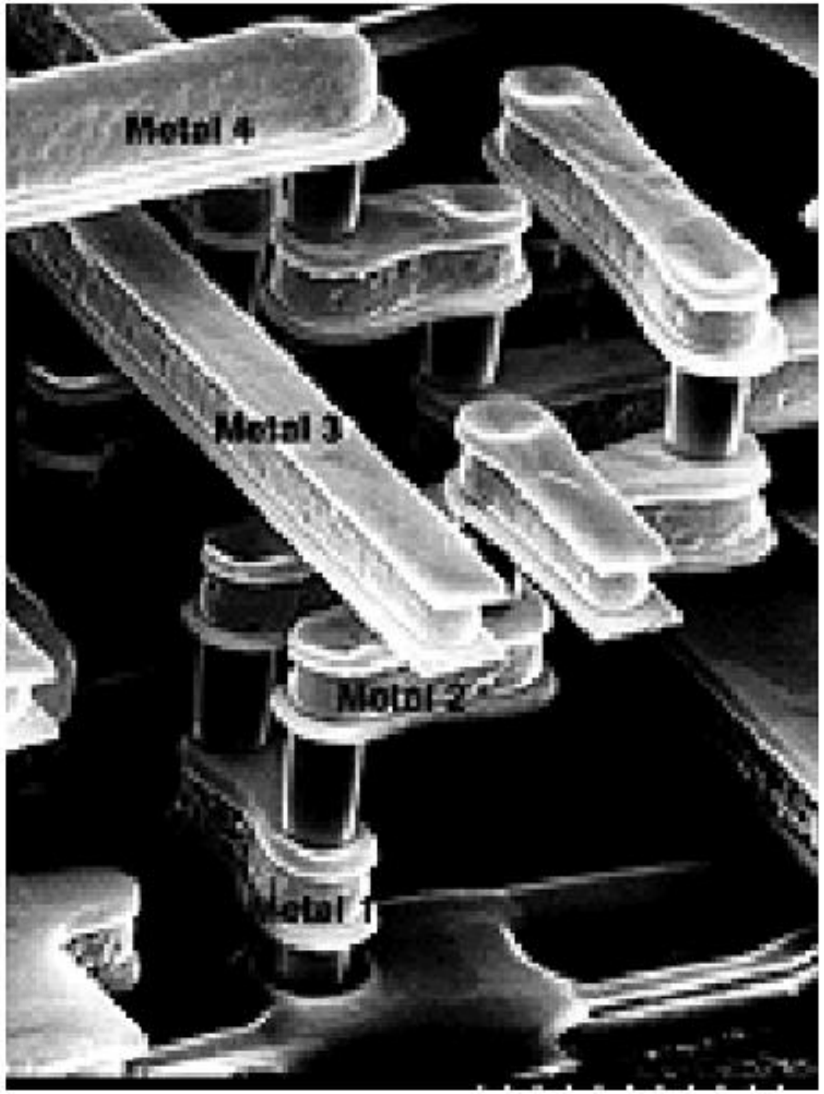
Kilby's idea was to make all the components and the chip out of the same block (monolith) of semiconductor material

Silicon IC processing

IC cross-section

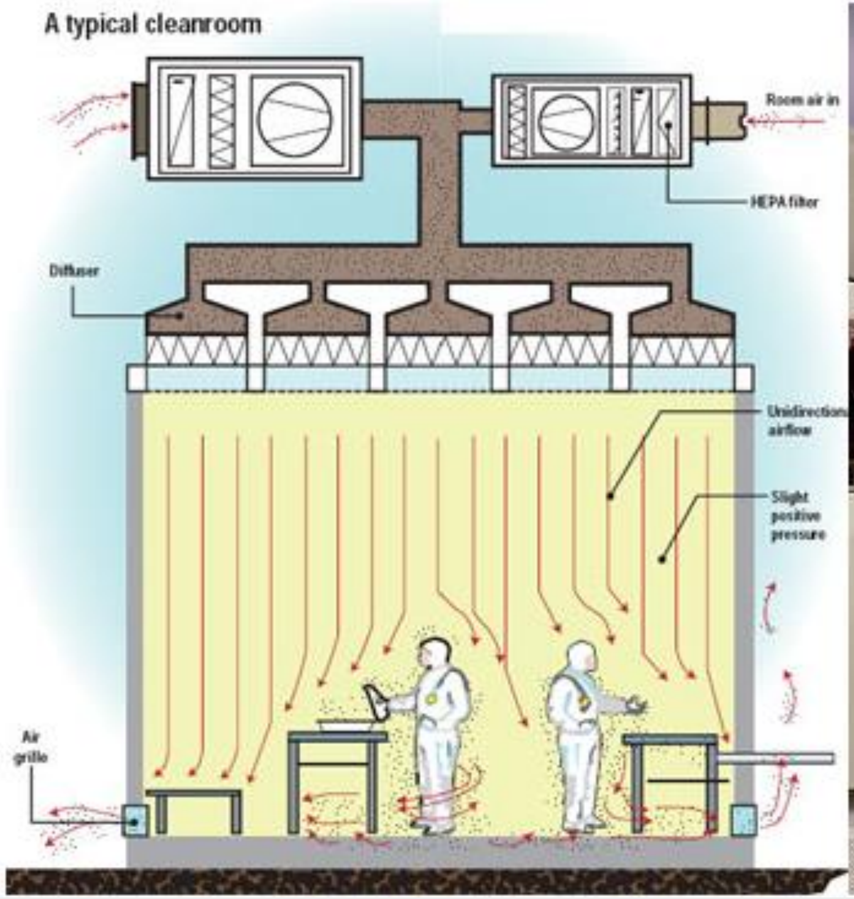






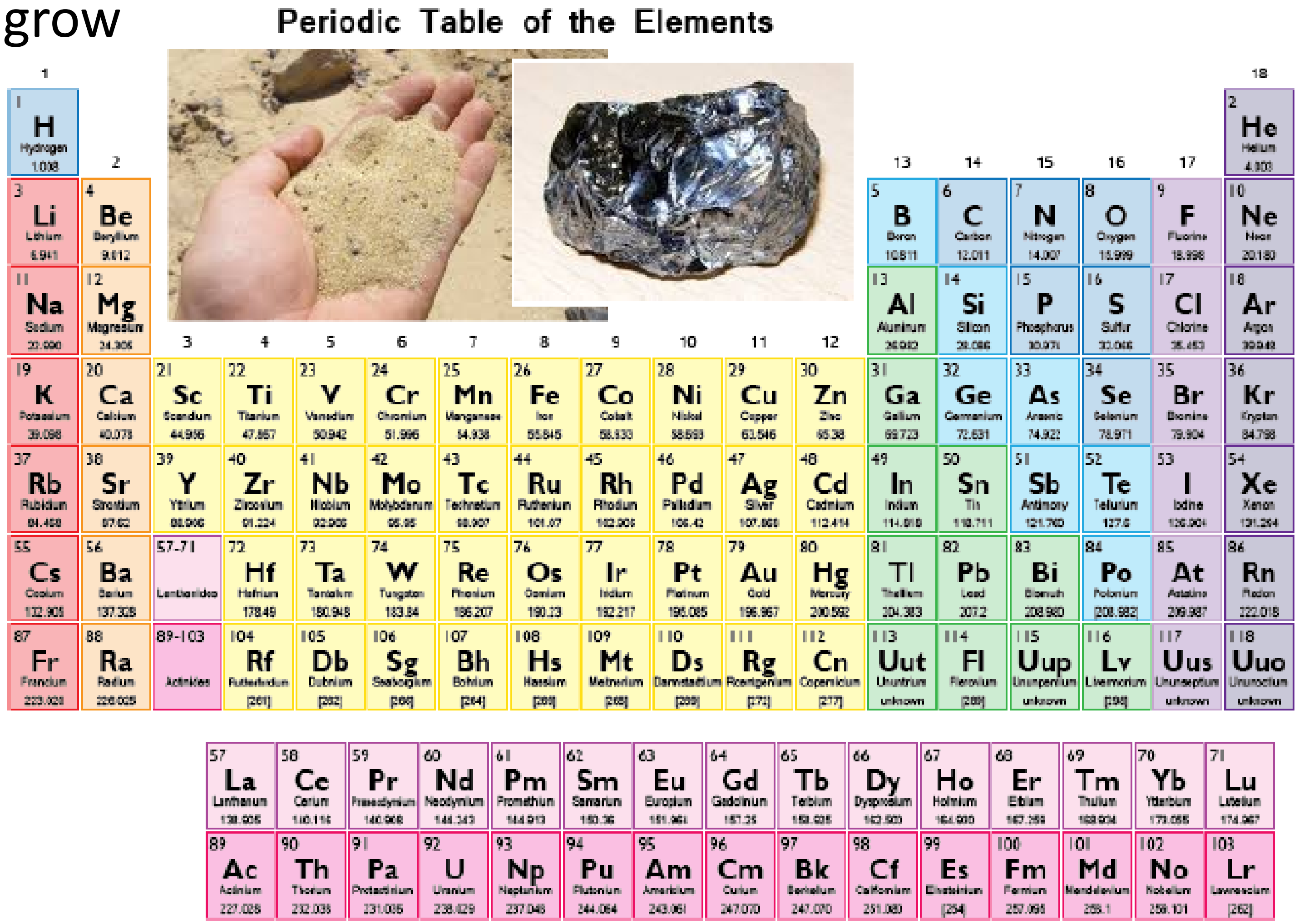
Prearrangement (Clean Room)

Urban environment = 35,000,000 particles$/cm^3$ of $\phi > 0.5\mu m$
Clean room =12 particles$/cm^3$ of $\phi < 0.3\mu m$



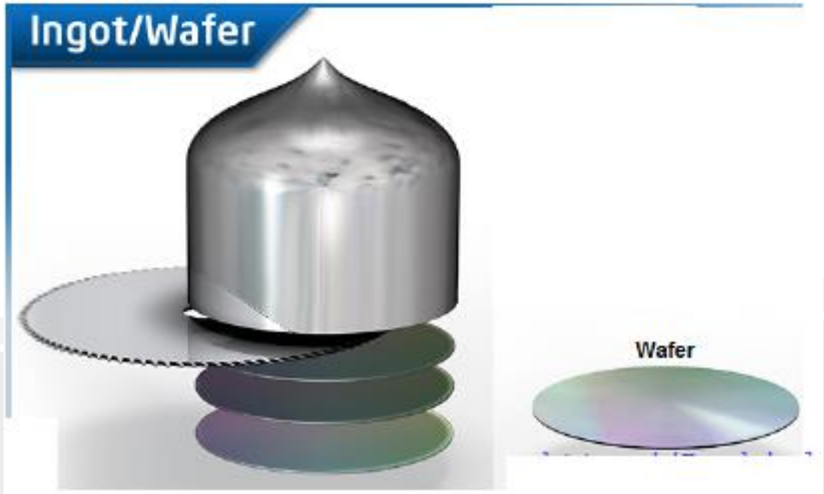
Prearrangement (Silicon Material)

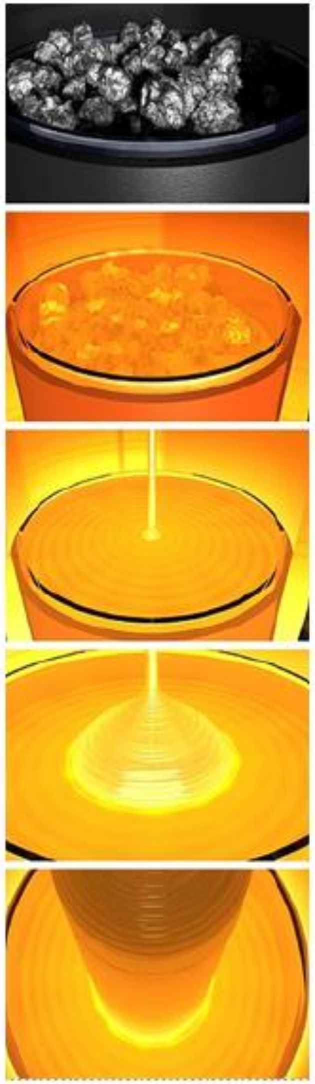
Silicon is an abundant element and occurs naturally in the form of sand. It need to be purified[1] and uniform[2] crystal grow

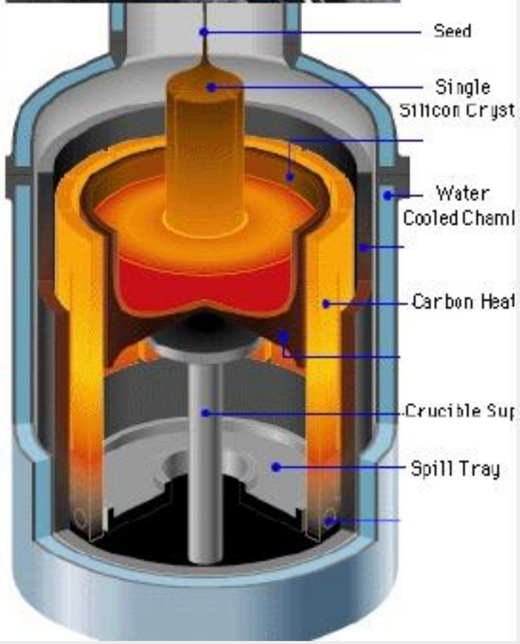


Prearrangement (*Czochralski process*)

1. Melt silicon at 1425 °C
2. Add impurities (dopants substrate)
3. Spin and pull crystal
4. Slice into wafers (400 µm to 600 µm) thick.
5. Polish one side (Using chemical and mechanical polishing (CMP) techniques)

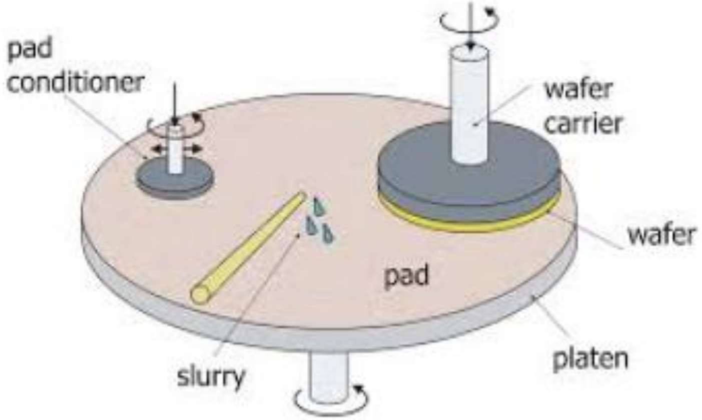


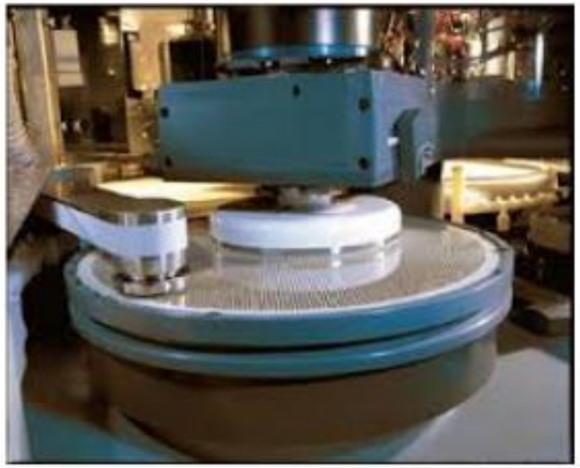




Prearrangement (Chemical Mechanical Polishing (CMP))

1. Mechanical polishing component and Chemical reaction component.
2. Goal: to planarize the surface of the wafer prior to photolithography.
3. abrasive chemical solution(slurry), is introduced between a polishing pad and the wafer.

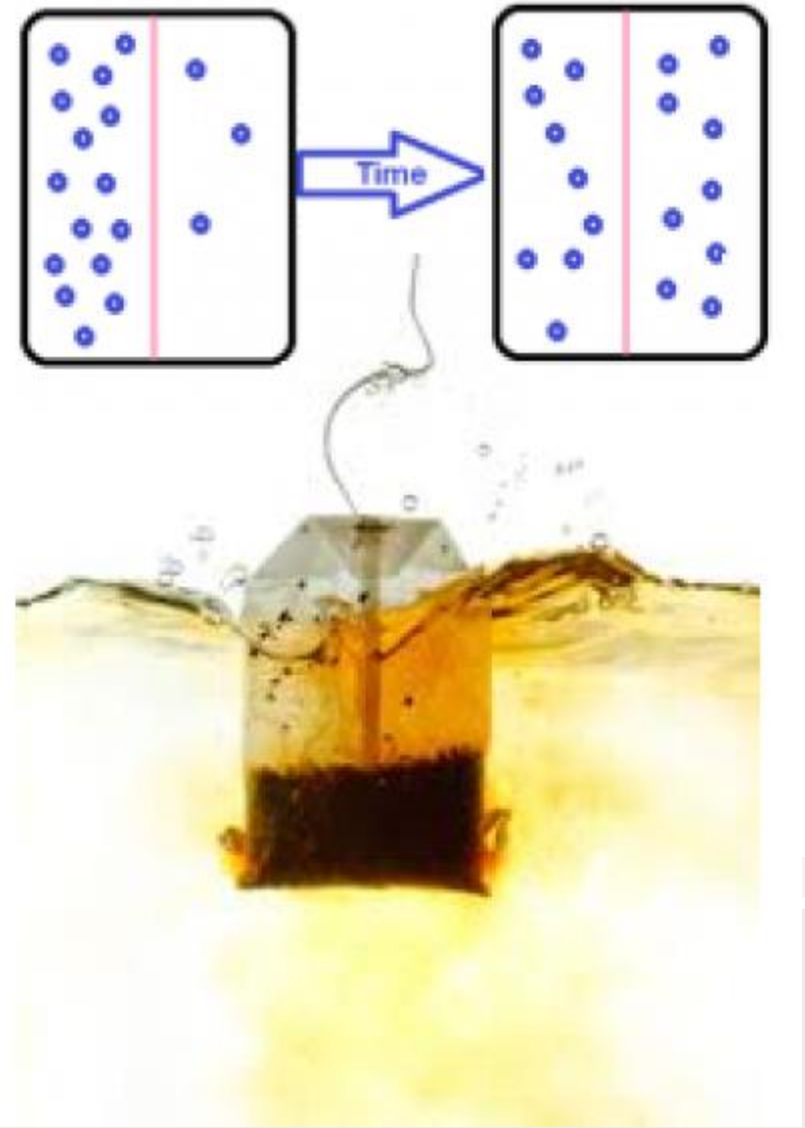




Doping Processes

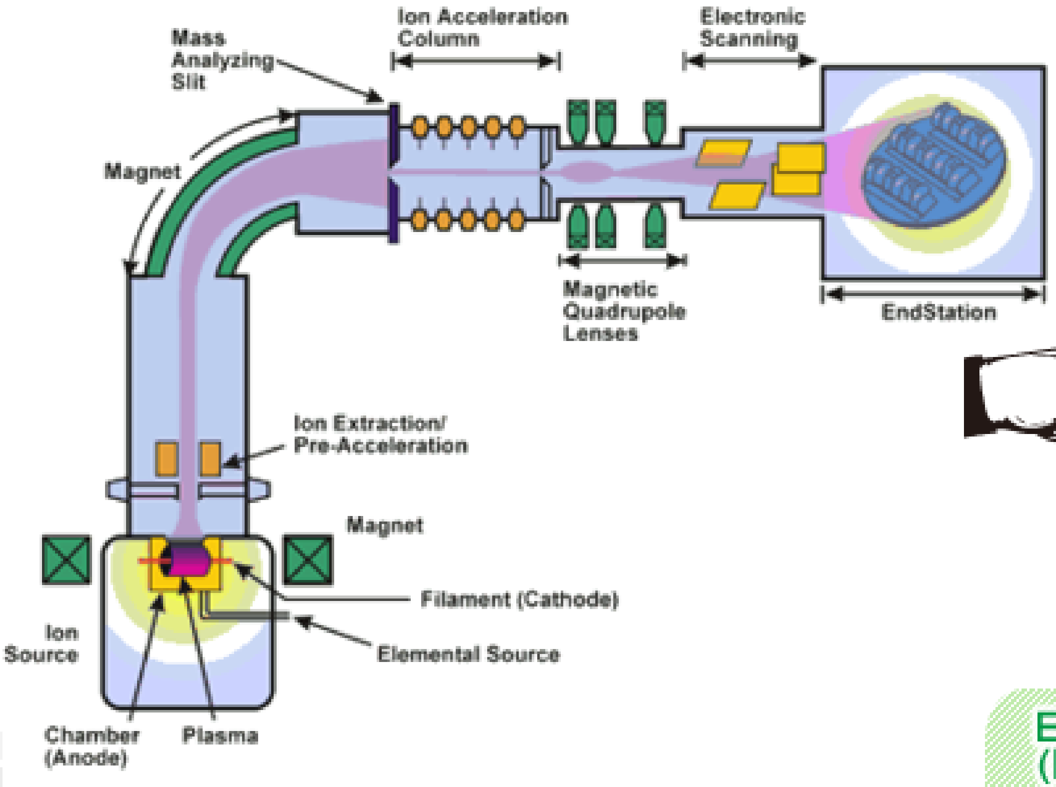
Solid State Diffusion

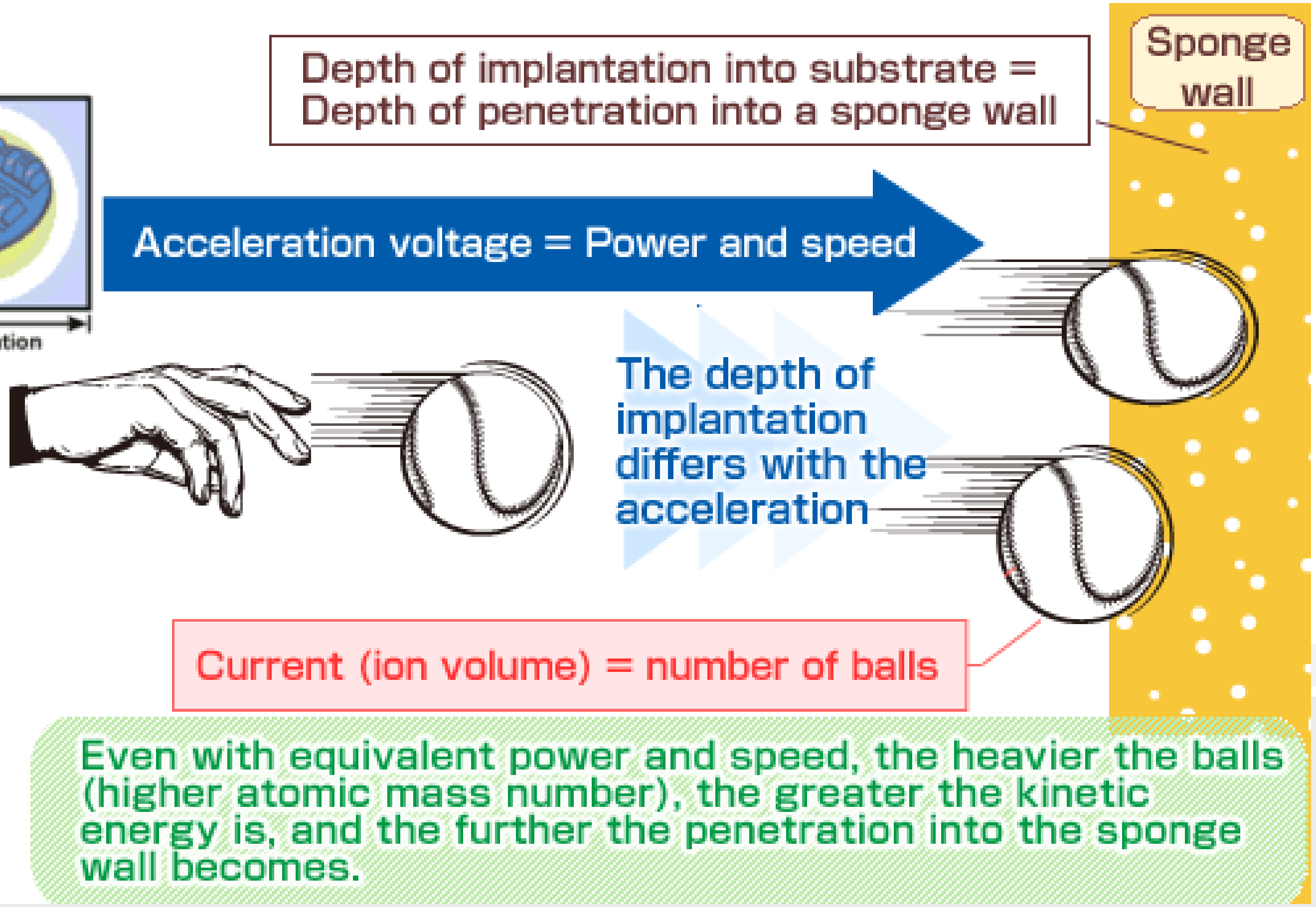
1. Diffusion is a process by which atoms move from a high-concentration region to a low concentration region.
2. this method introduces impurity atoms (dopants) into silicon to
3. change its resistivity.
4. The most common impurities used as dopants are boron (p-type), phosphorus(n-type), and arsenic(n-type).
5. Solid state diffusion inherently occurs in **high temperature** steps.



Ion Implantation

An ion implanter produces ions of the desired dopant, accelerates them by an electric field, and allows them to strike the semiconductor surface





Diffusion vs. Ion Implantation

Diffusion	Ion Implantation
Introducing impurities to semiconductors	
Based on concentration gradient	Injecting an energetic ion beam
A high-temperature process	A low-temperature process
Uncontrollable	Dopant concentration could be controlled
Isotropic dopant profile	Anisotropic dopant profile
Limited to solid solubility	leads to a high degree of lattice damage
Need thick layers	Possible through the thin layers

Deposition Processes

Oxidation Isolation

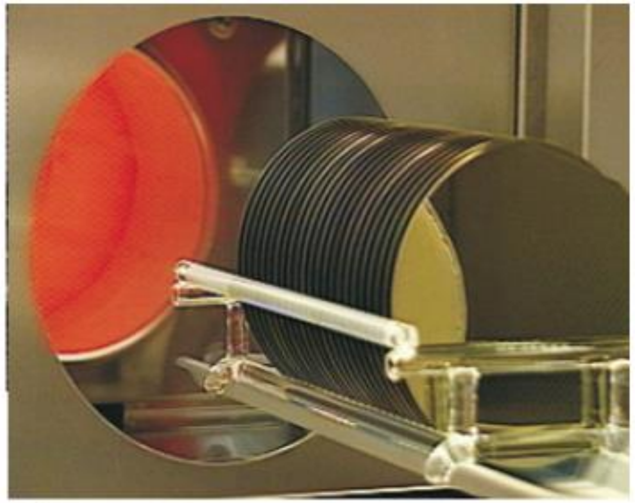
In oxidation, silicon reacts with oxygen to form silicon dioxide (SiO_2).
(ultra clean furnaces 1000-1200 °C)

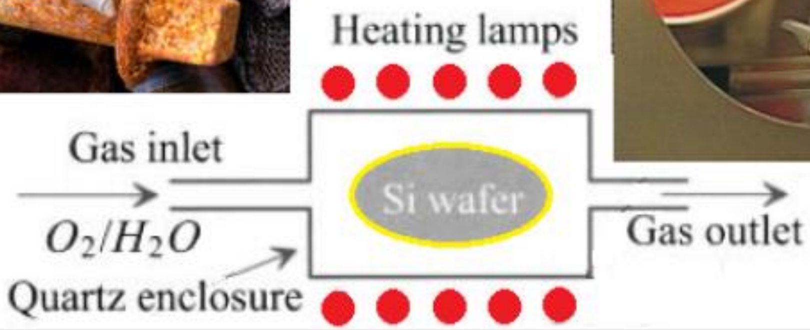
$$Si + O_2 \xrightarrow{heat} SiO_2 \qquad \text{(dry oxidation)} \qquad (1)$$

$$Si + 2H_2O \xrightarrow{heat} SiO_2 + 2H_2 \qquad \text{(wet oxidation)} \qquad (2)$$

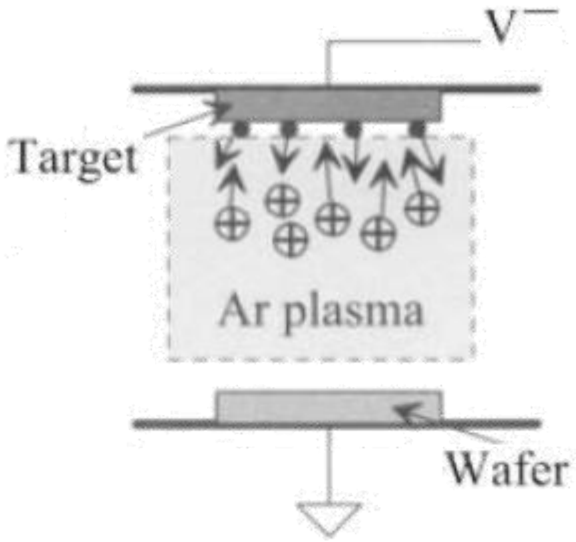
high-purity gas

steam



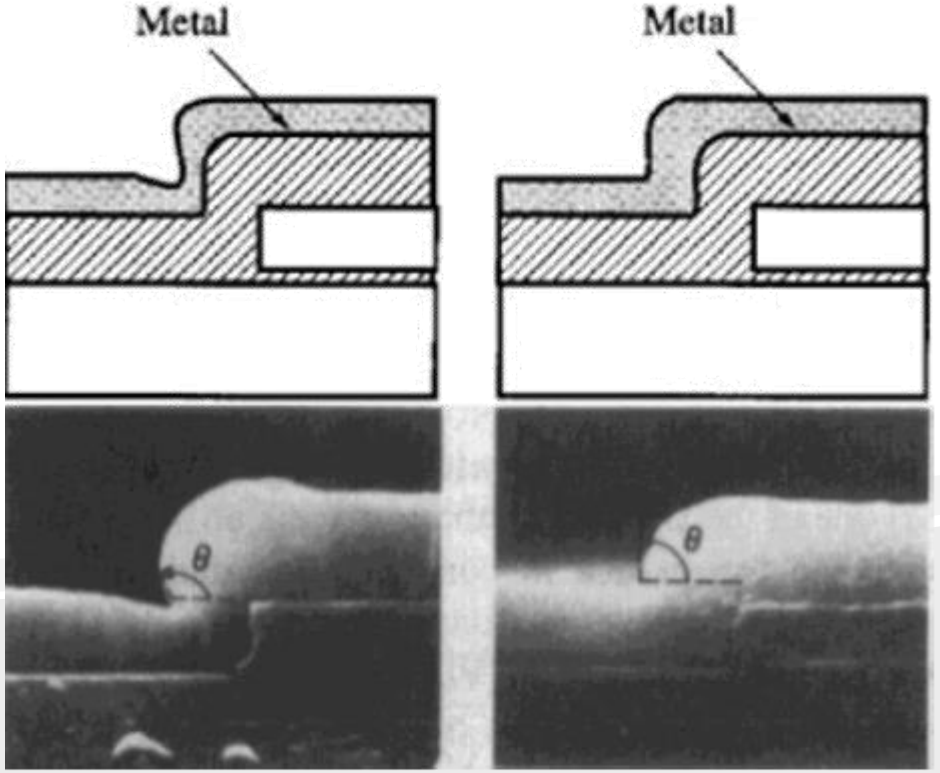


Physical Vapor Deposition (PVD)



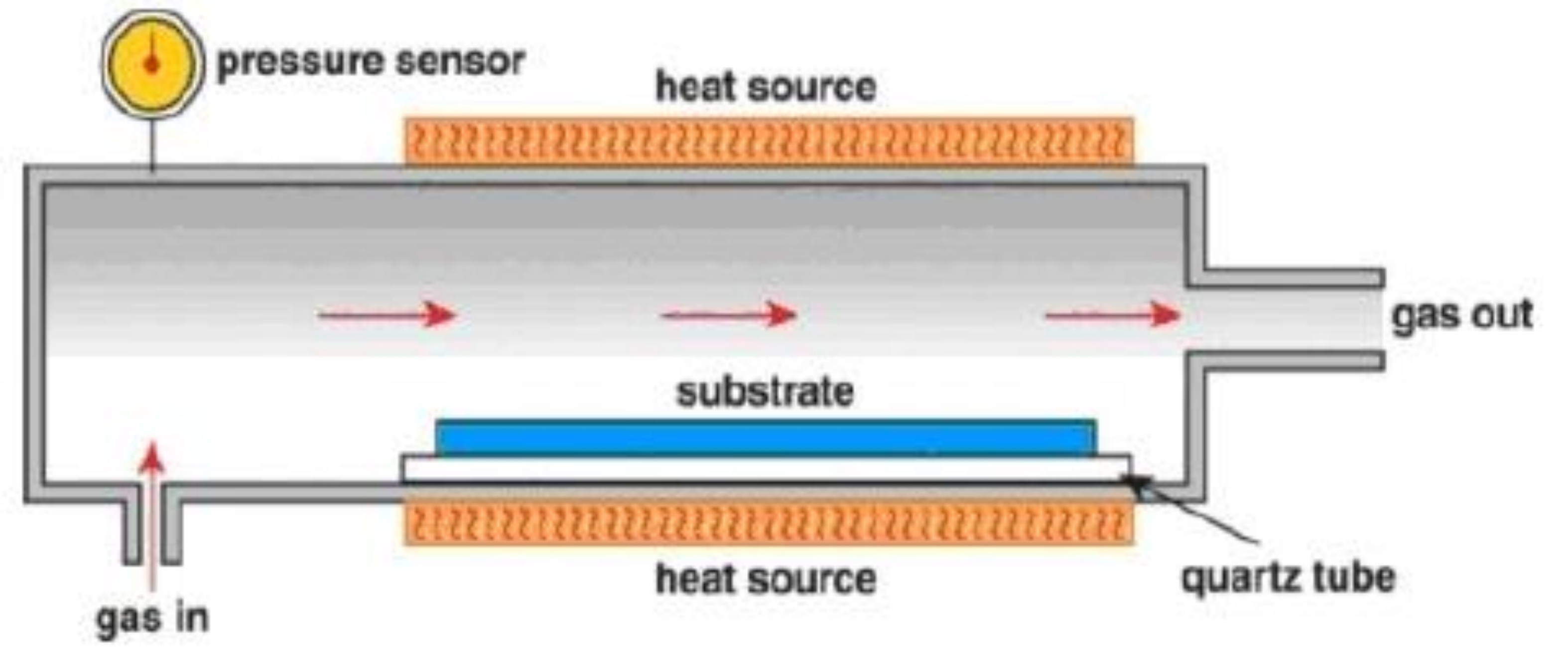
Sputter Deposition

1. Gas (e.g., argon)
2. Positively ionized
3. Accelerated through an electric field
4. Target metal sits on the cathode
5. Bombarded by the positively charged ions
6. Material to be ejected off (mechanically) to wafer
7. Poor step coverage



Chemical Vapor Deposition (CVD)

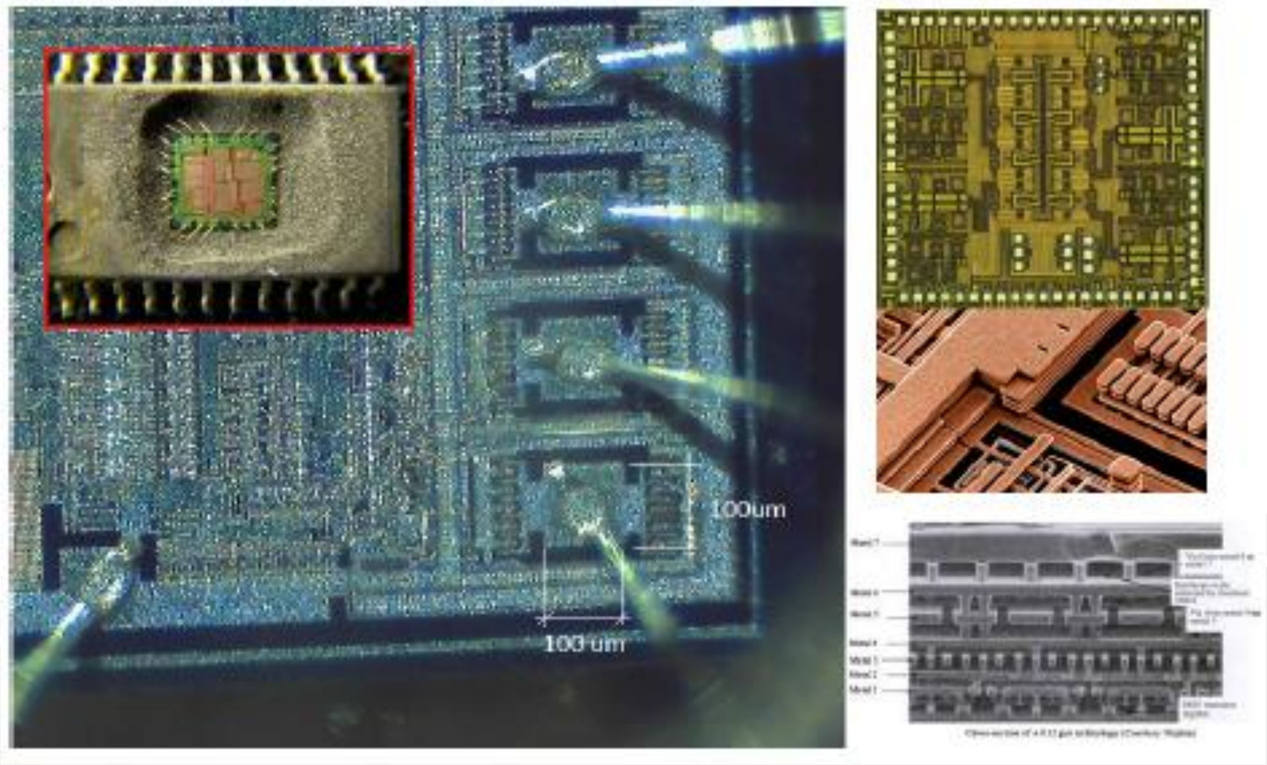
is a process by which gases or vapors are , leading to the formation of solids on a substrate. CVD can be used to deposit various materials on a silicon substrate including SiO_2, Si_3N_4, polysilicon



Metallization

Metallization is the process by which the components of IC's are interconnected by aluminum conductor polysilicon. CVD is used for metallization.

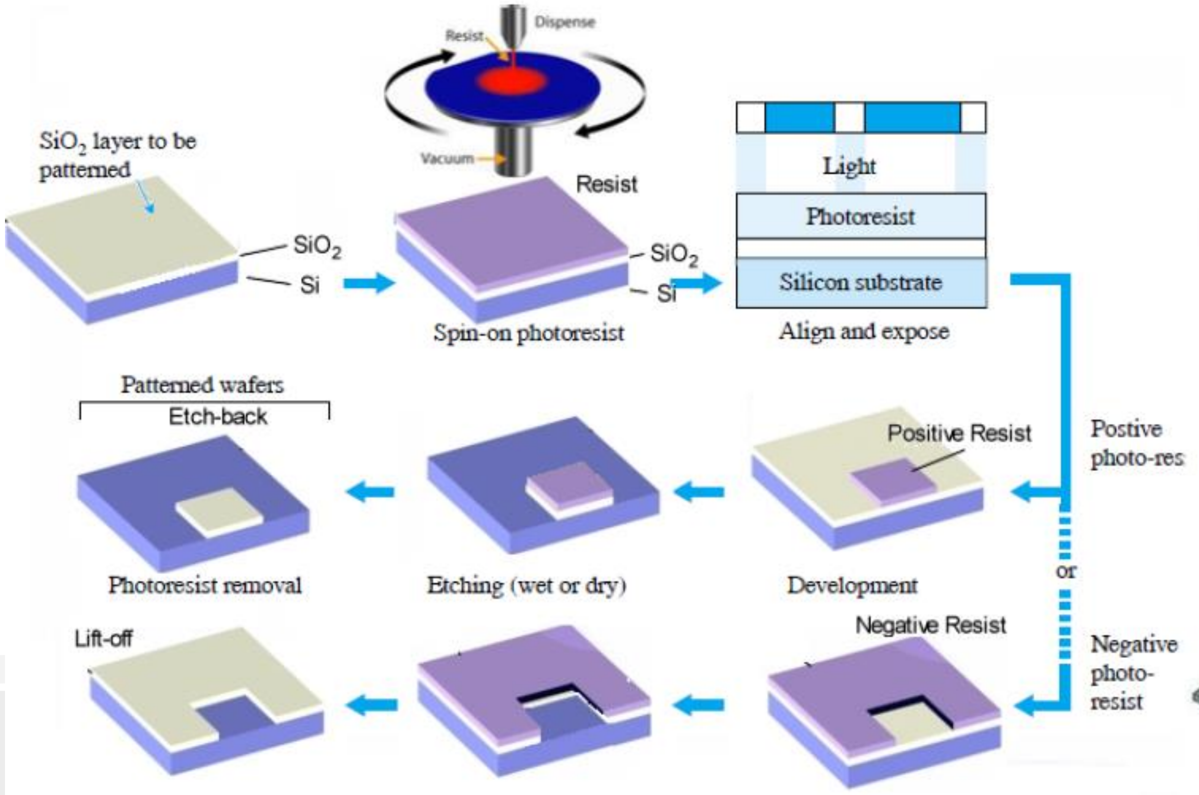
1. Interconnect the various components on the chip.
2. bonding pads.

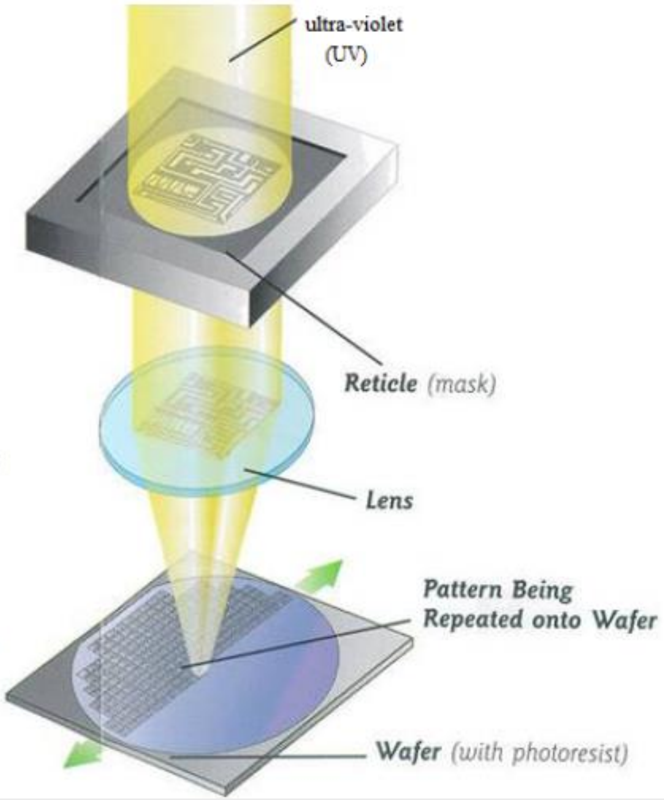


Formation processes

Photolithography

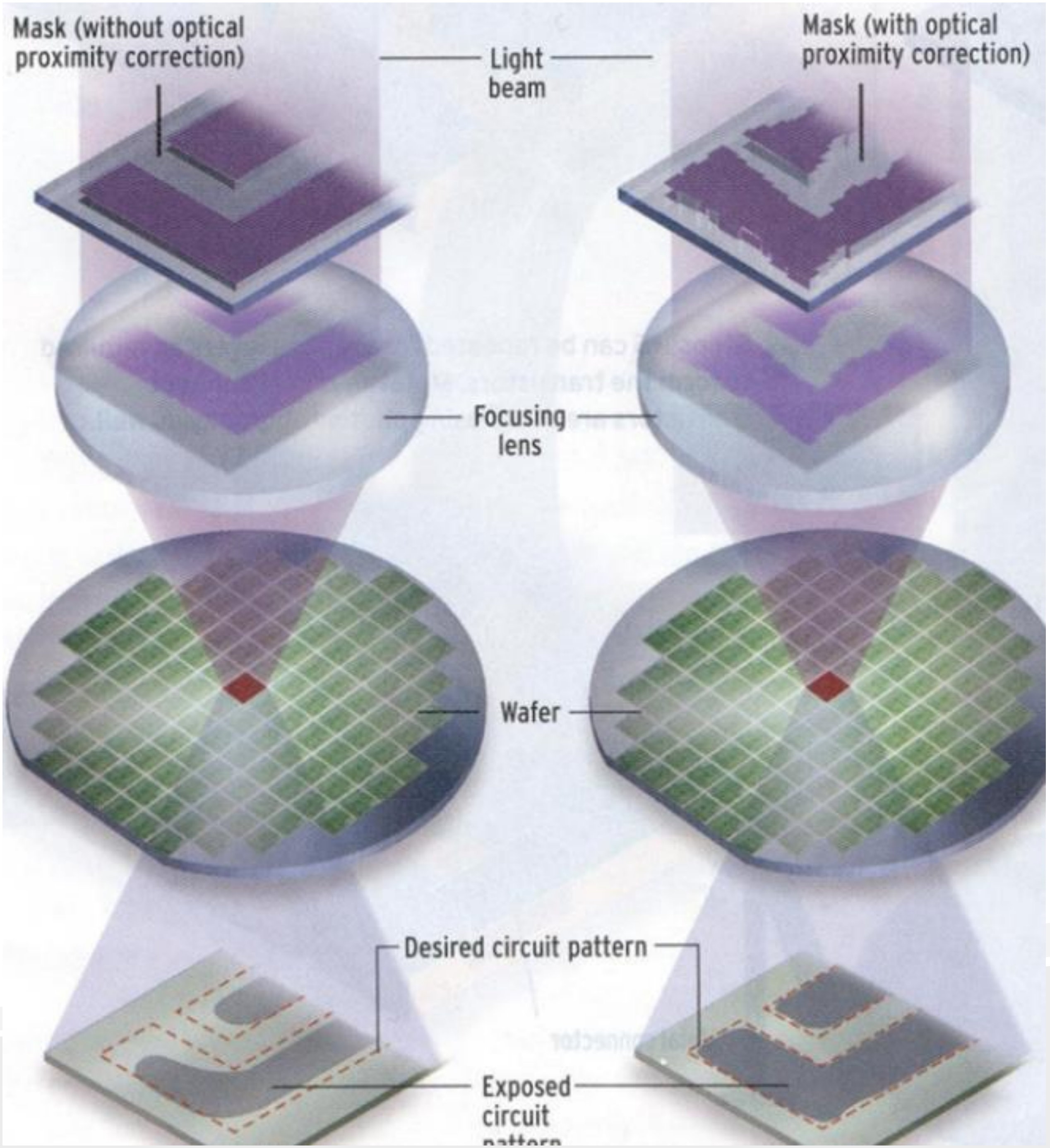
is the process of transferring geometric shapes on a mask to the surface of a silicon wafer. (ultraviolet light + a mask + a light-sensitive chemical resistant polymer). By dropping photoresist to a rotating wafer yielding a uniform thin film on the surface.





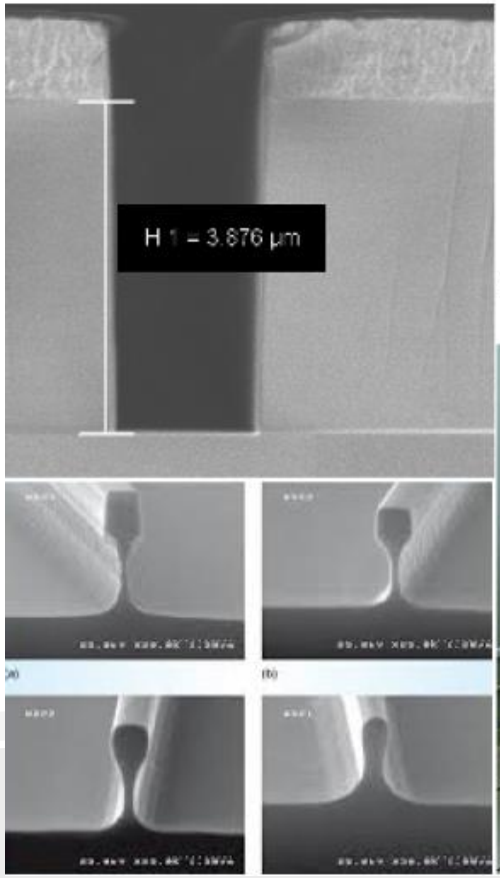
Mask (Reticle)

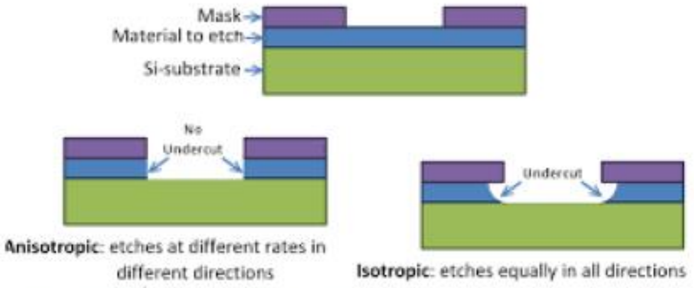
numerous mask levels (e.g., active, poly, contacts, etc.) are printed on the wafer.



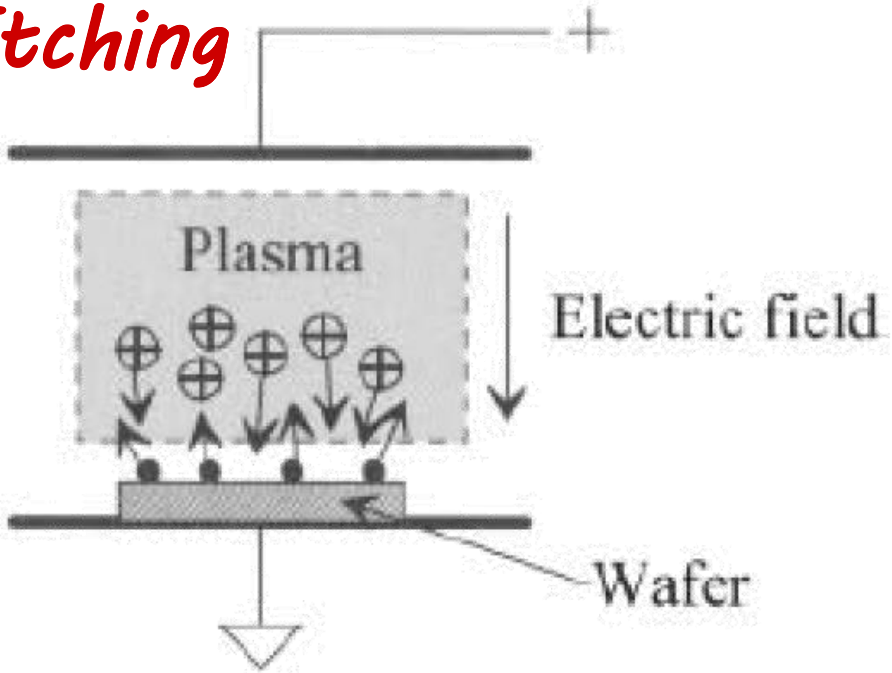
Wet Etching

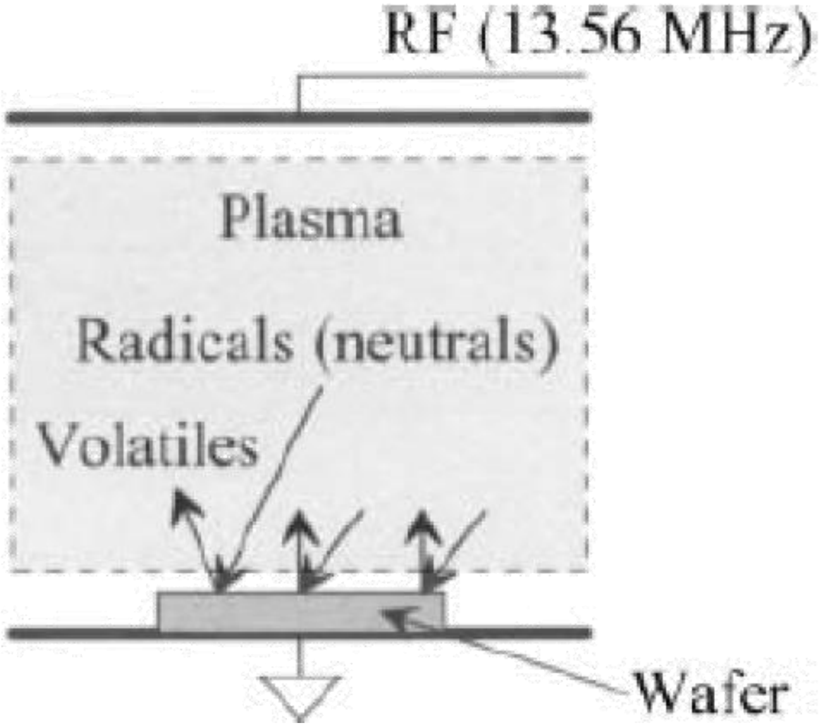
Isotropy and anisotropy: When a material is attacked by a liquid or vapor etchant, it is removed isotopically (uniformly in all directions) or anisotropic etching (uniformity in vertical direction)





Dry Etching

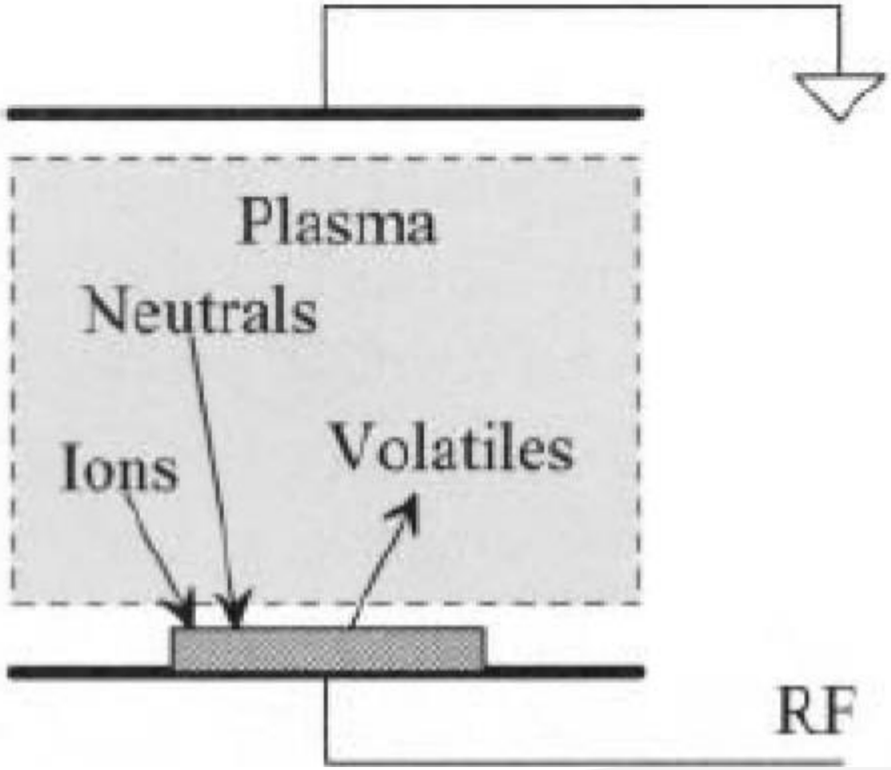




Sputter (sound) etching	Plasma etch
Gas (e.g., argon)	Gas or mixture of gases (e.g., halogens)
Positively ionized	Ionized producing reactive species (radicals)
Accelerated through an electric field	
Wafer sits on the cathode	Wafer sits on the cathode
Bombarded by the positively charged ions	Radicals chemically react with surface
Material to be ejected off (mechanically)	Material forming reaction products in the gas phase
Not selective and anisotropic.	Highly selective and isotropic

Dry Etching

Reactive ion etching (RIE)
Combination of sputter etching and plasma etching
Radicals and ionized species are generated
Wafer sits on the cathode
Highly selective and highly anisotropic



Wet/Dry Etching

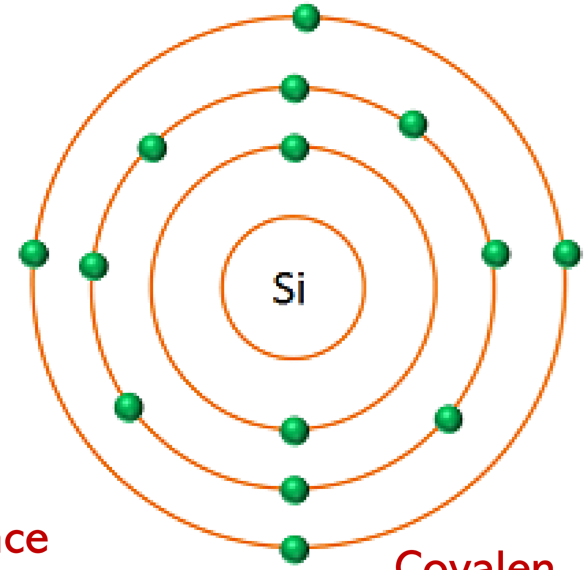
Wet etching	Dry etching
Removal of metals, semiconductors, and insulators	
Isotropic and anisotropic	Higher degree of anisotropy
Using a chemical solution	
Cleaning of wafers	
Rinsed in deionized (DI) water	

PN Junction

Texbook Reference

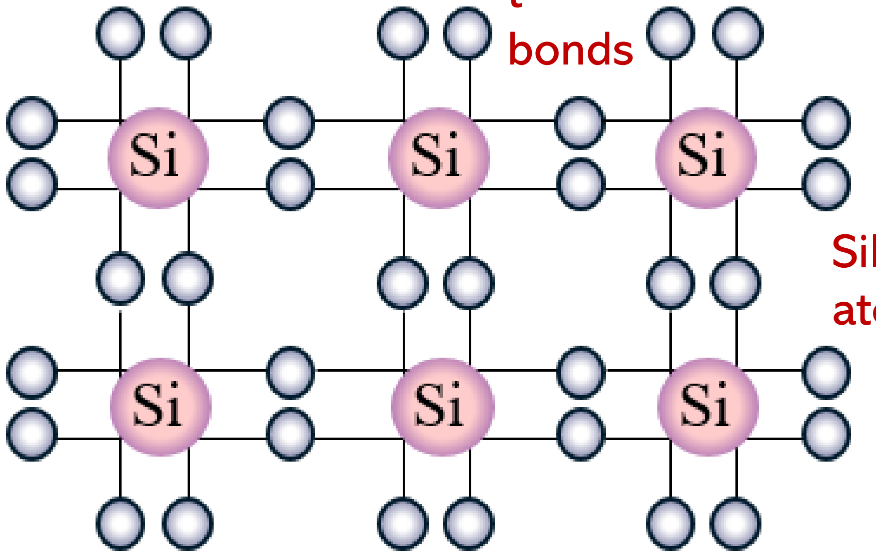
“Microelectronic Circuits” , Adel Sedra

Intrinsic Semiconductors

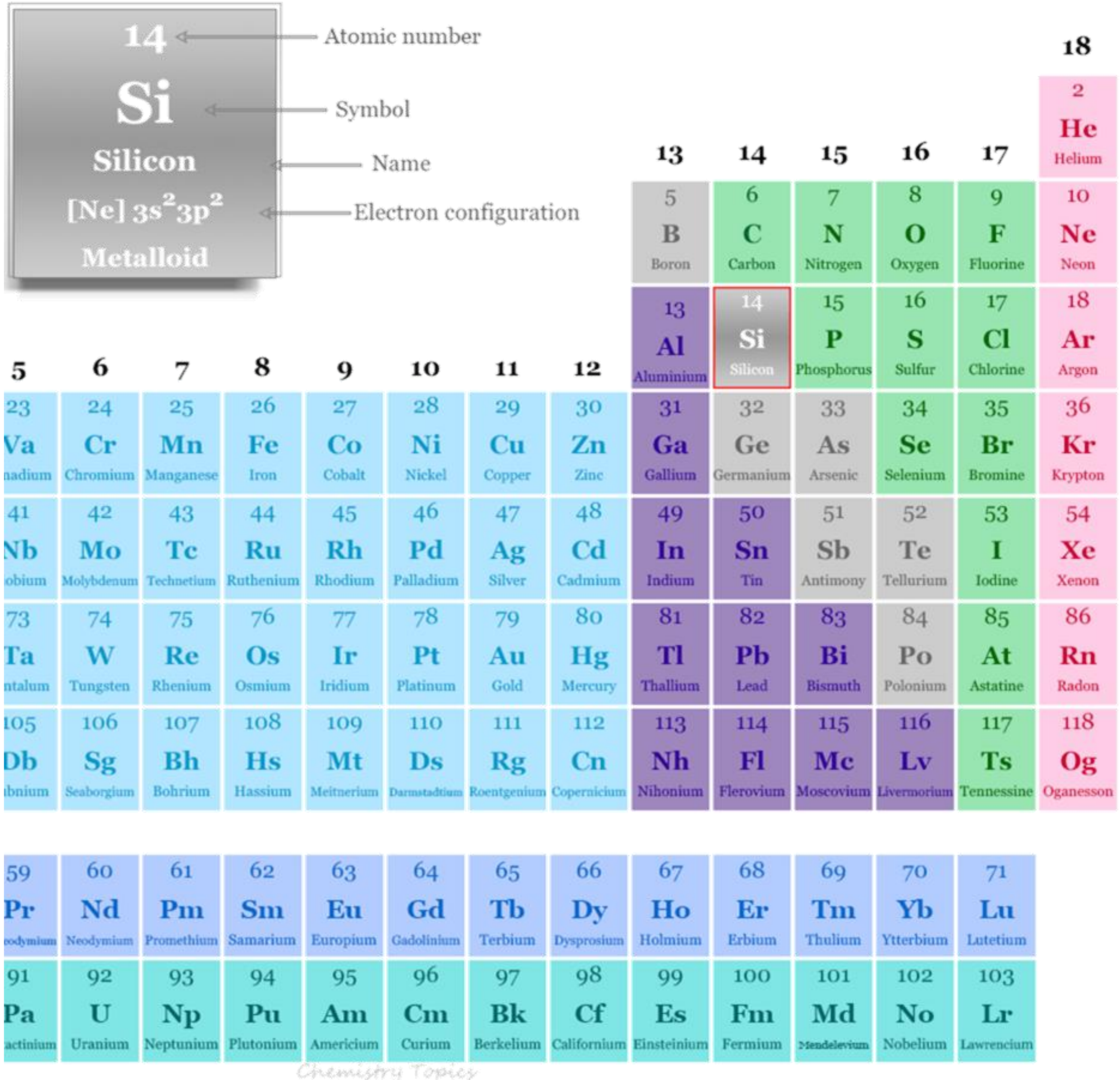


Valence electrons

Covalent bonds



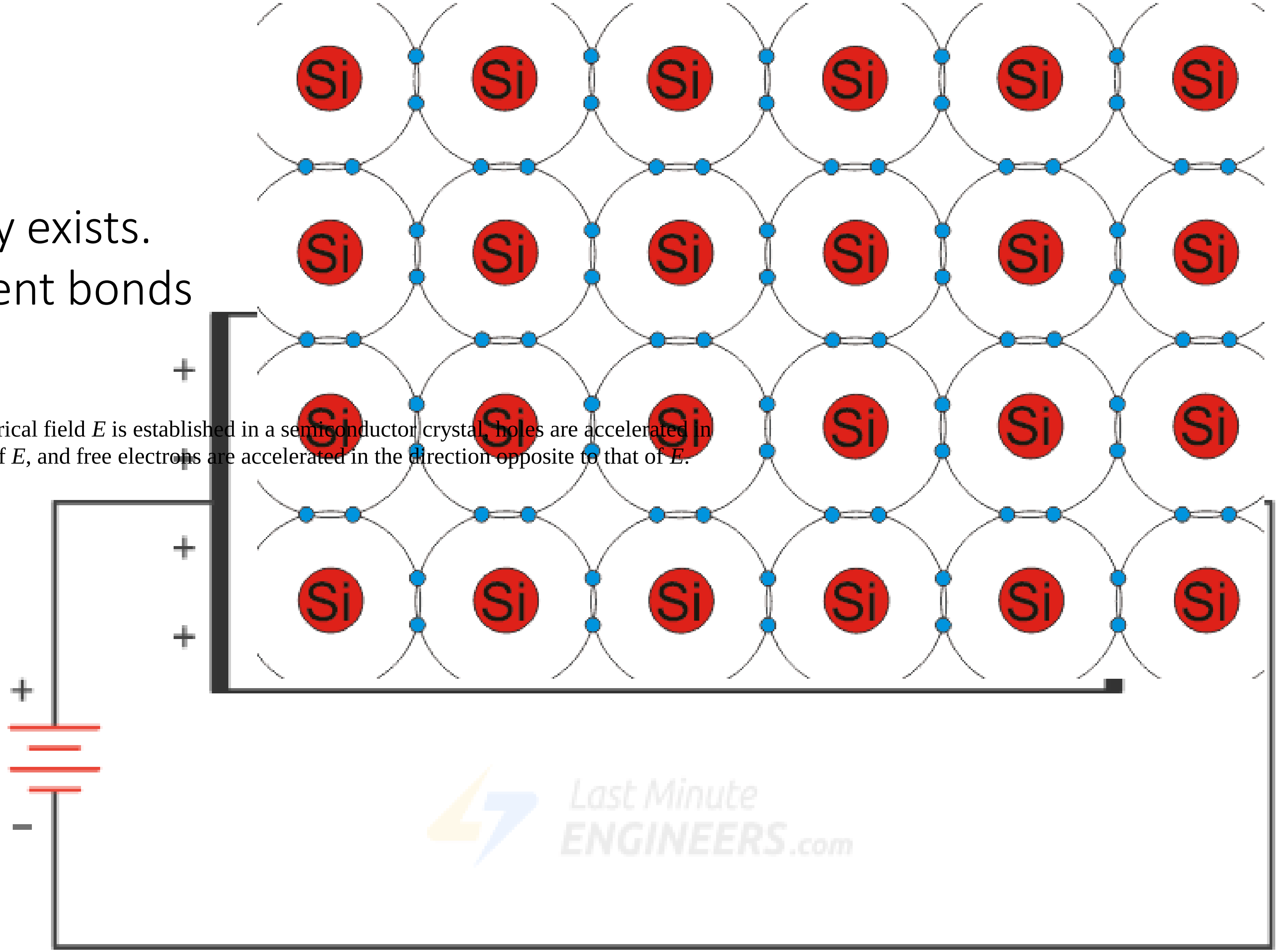
Silicon atoms



Thermal Generation

1. At room temperature
2. Sufficient thermal energy exists.
3. Break some of the covalent bonds

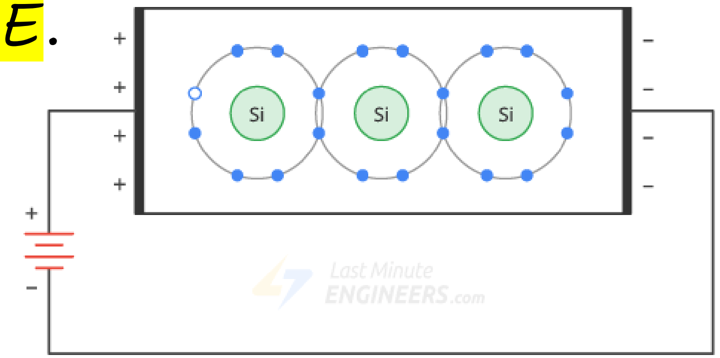
If a voltage is applied, then both the electron and the hole can contribute to a small current flow.



When an electrical field E is established in a semiconductor crystal, holes are accelerated in the direction of E, and free electrons are accelerated in the direction opposite to that of E.

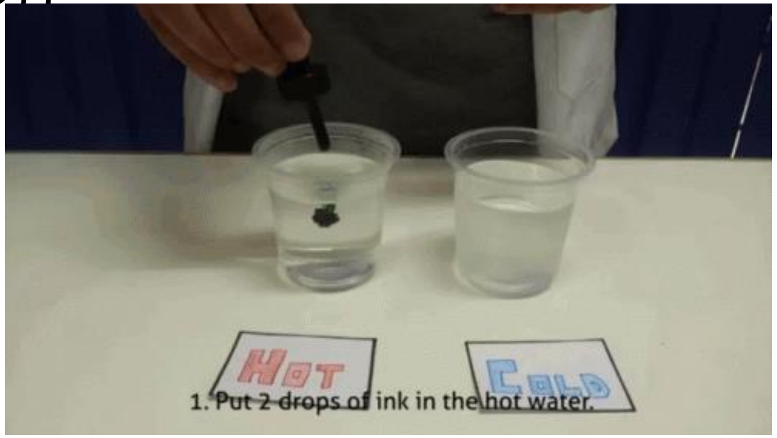
Drift Current

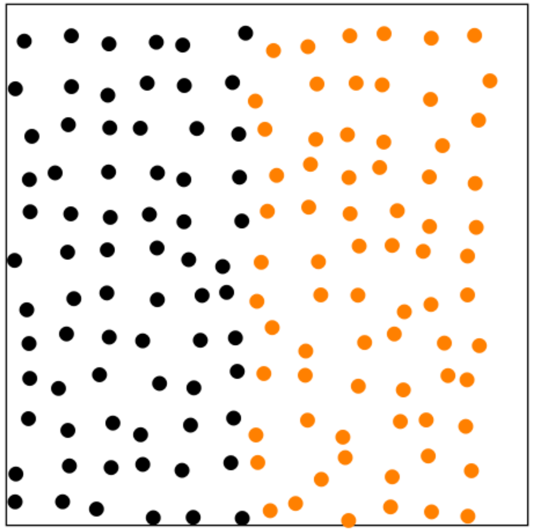
When an electrical field E is established in a semiconductor crystal, holes are accelerated in the direction of E, and free electrons are accelerated in the direction opposite to that of E.



Diffusion Current

At non-uniform charge distribution , the charges flow from high concentration to low concentration

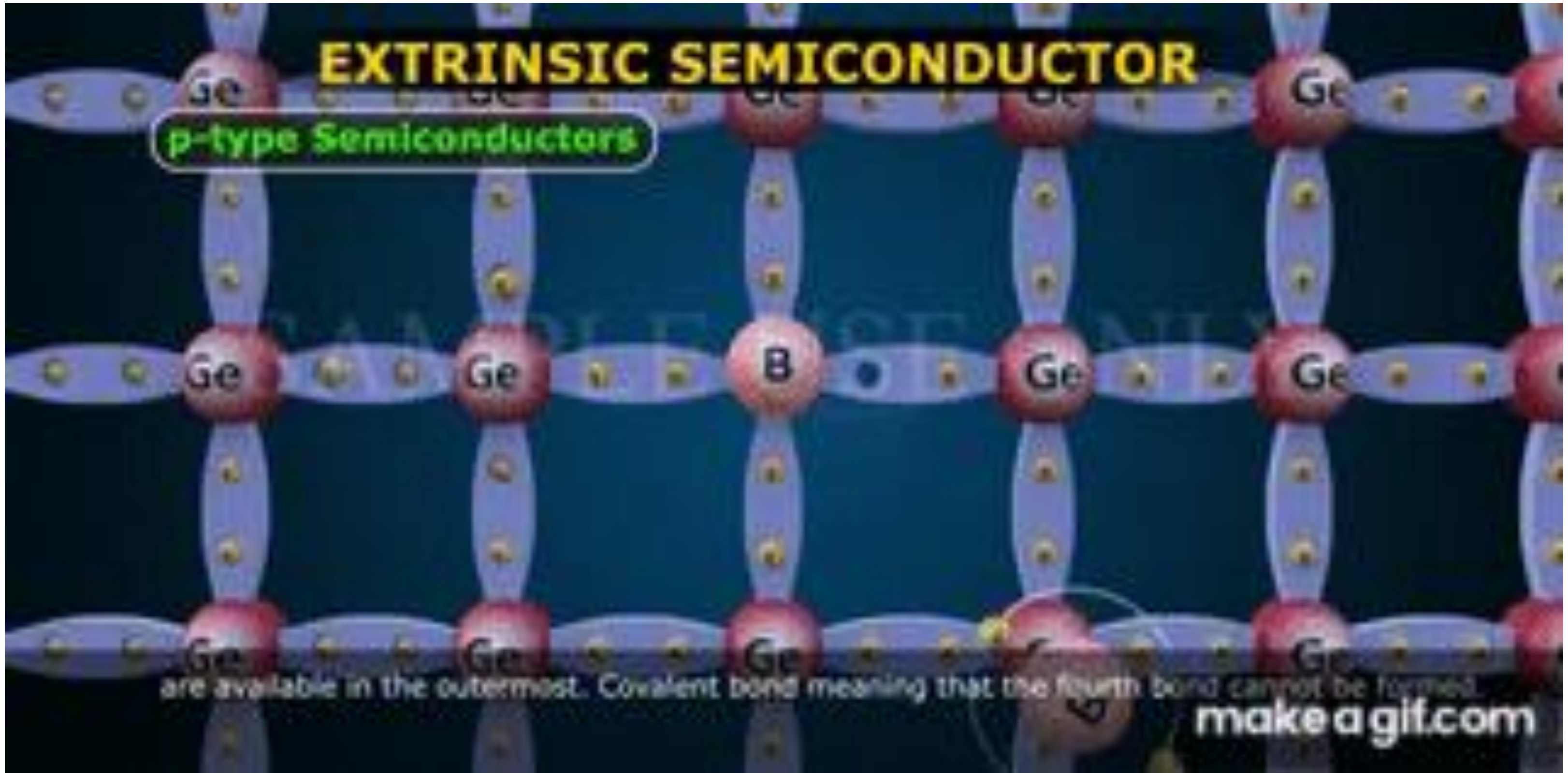




Recombination

1. Some electrons may fill some of the holes.
2. Disappearance of free electrons and holes

Doped Semiconductors

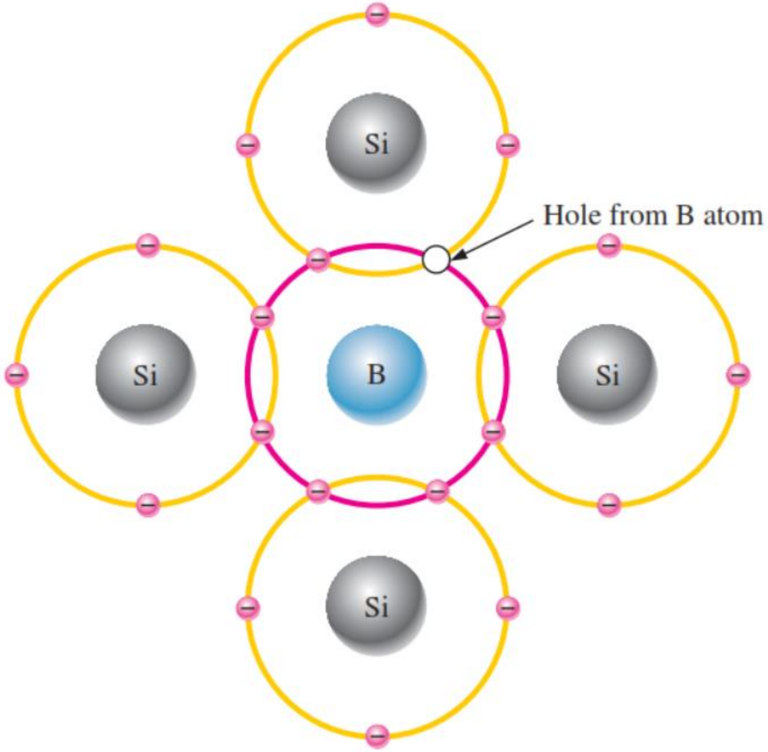


13	14	15
5 B Boron	6 C Carbon	7 N Nitrogen
13 Al Aluminium	14 Si Silicon	15 P Phosphorus
31 Ga Gallium	32 Ge Germanium	33 As Arsenic
49 In Indium	50 Sn Tin	51 Sb Antimony
81 Tl Thallium	82 Pb Lead	83 Bi Bismuth
113 Nh Nihonium	114 Fl Flerovium	115 Mc Moscovium

introducing impurity atoms into the silicon crystal in sufficient numbers to substantially increase the concentration of either free electrons or holes but with little change in the crystal properties of silicon.

Doped Semiconductors

Sb impurity is called an **acceptor**.



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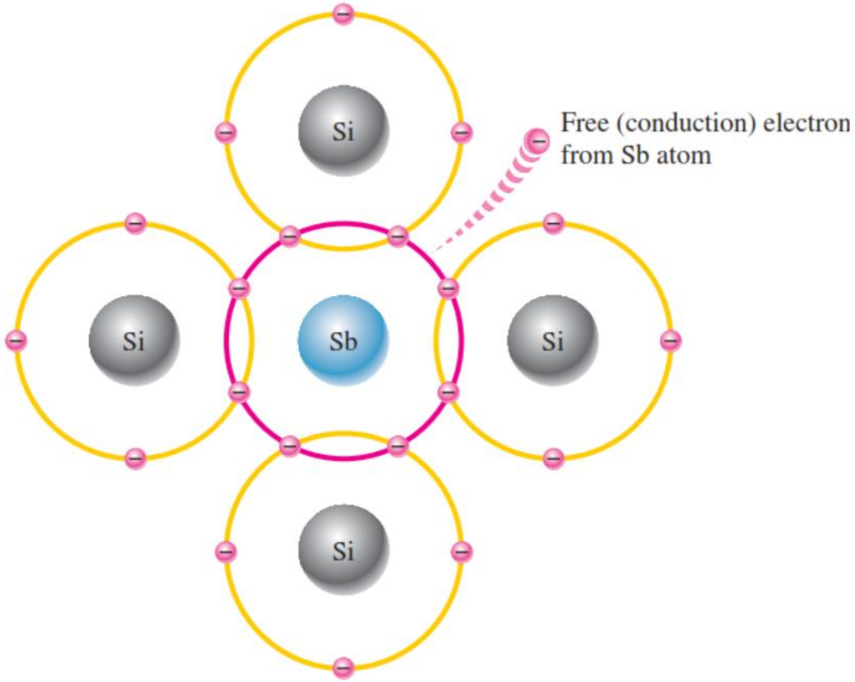
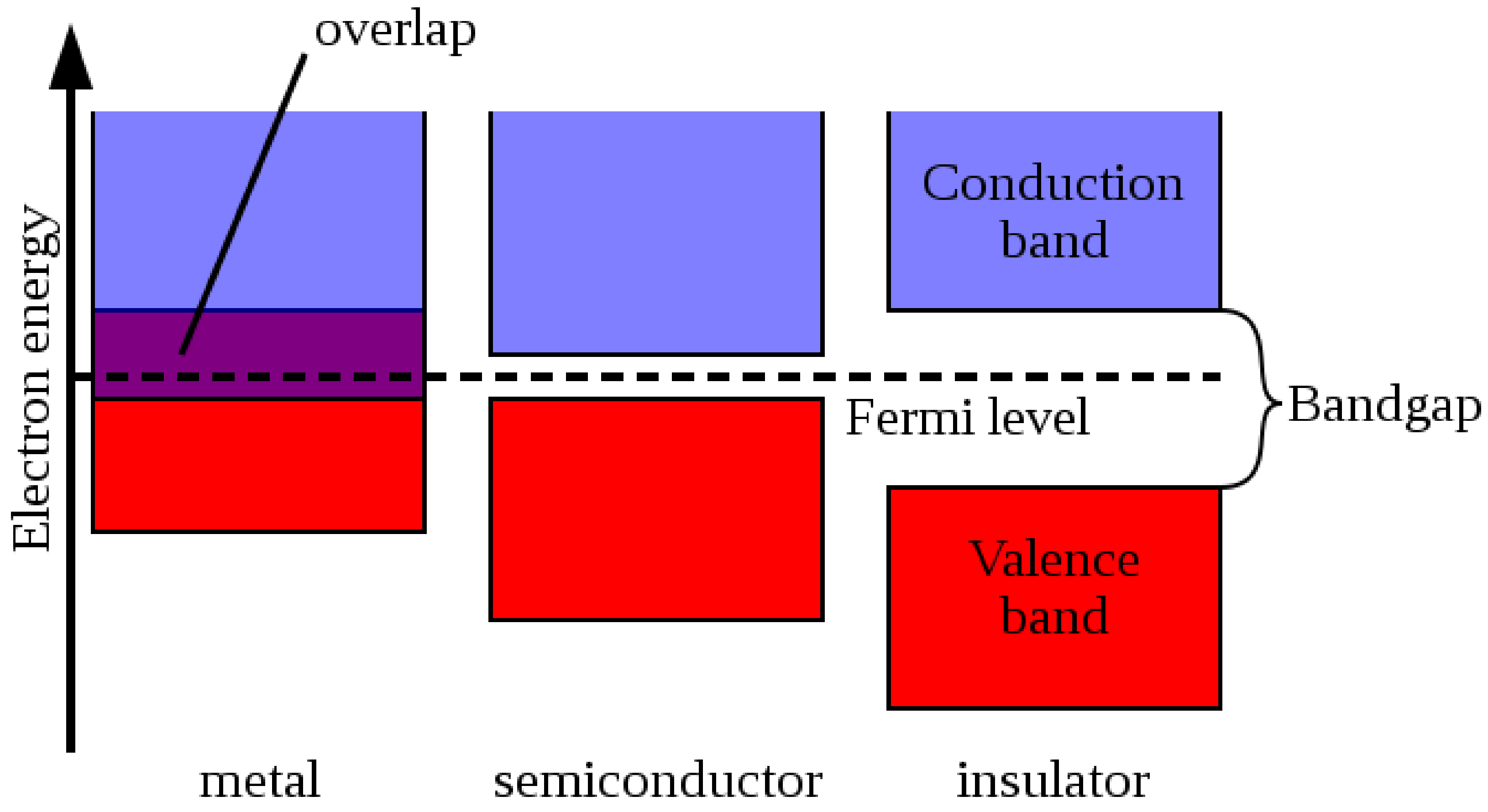
Sb impurity is called a **donor**.

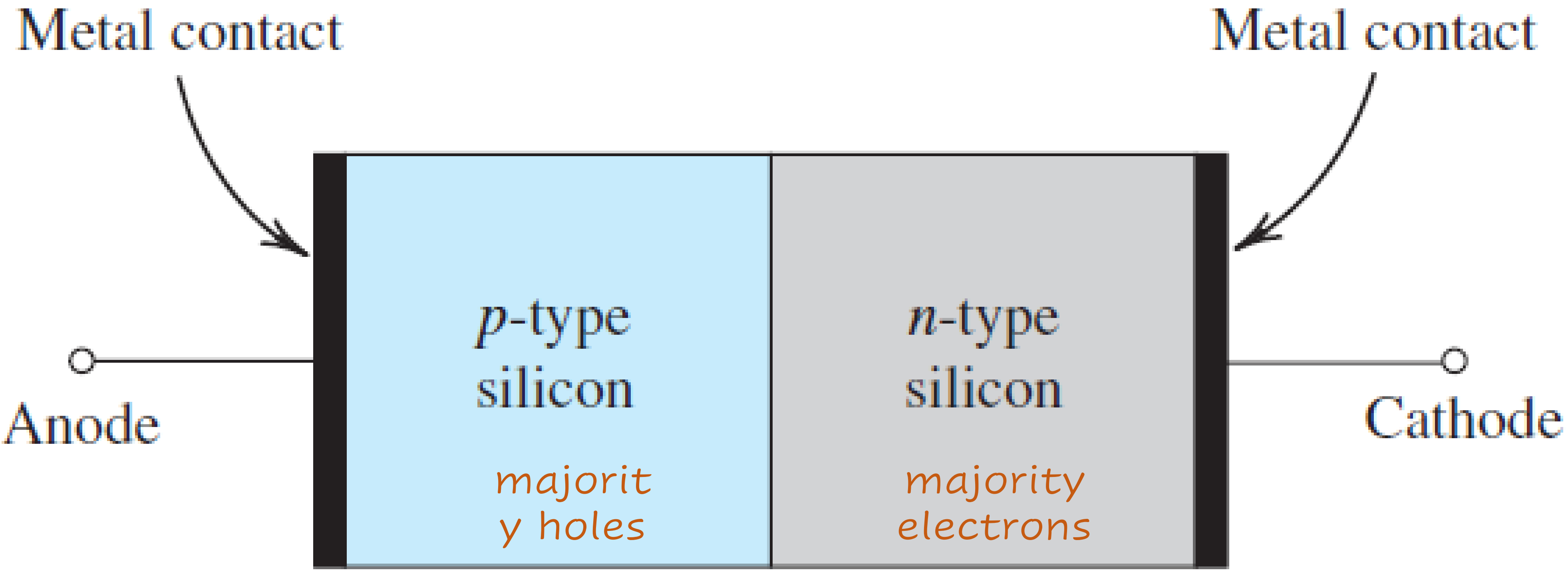


Band Diagrams

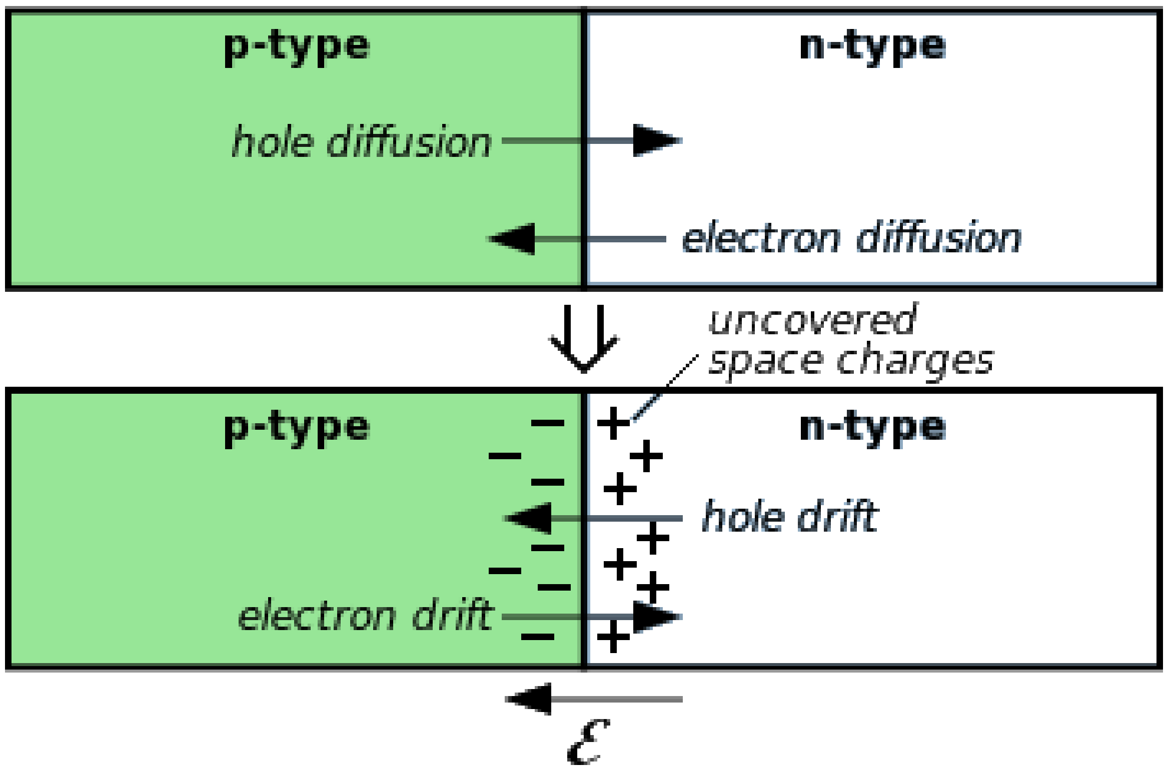


PN Junction

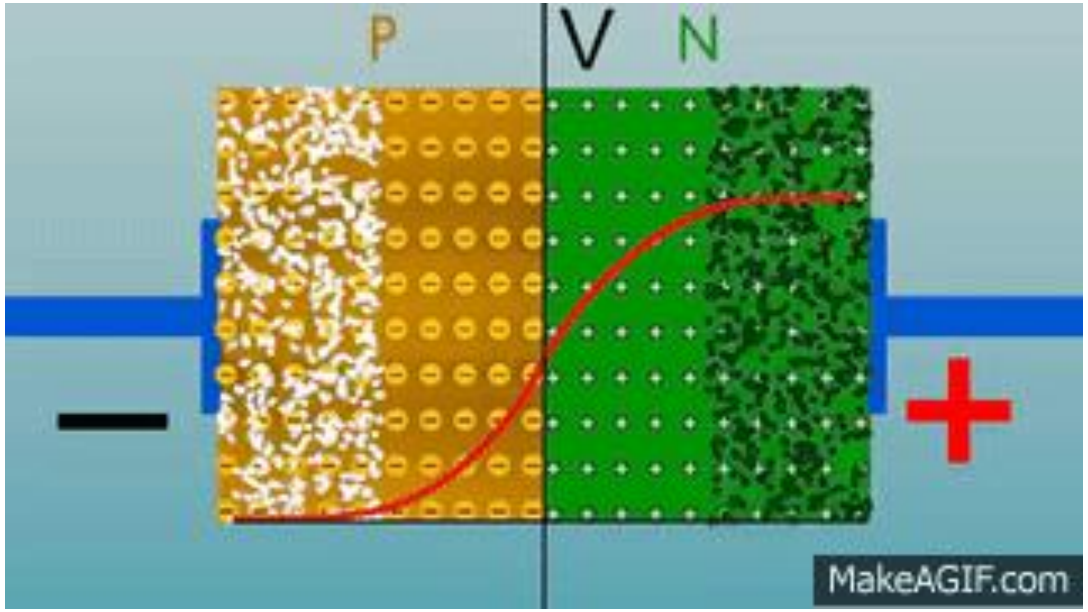
Physical Structure

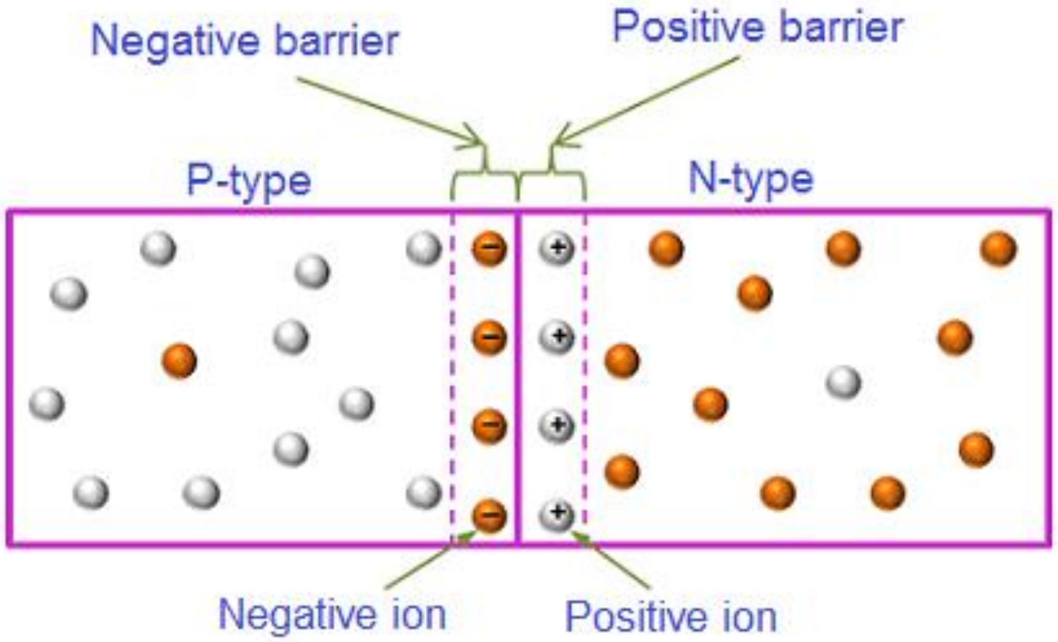


1. Diffusion current

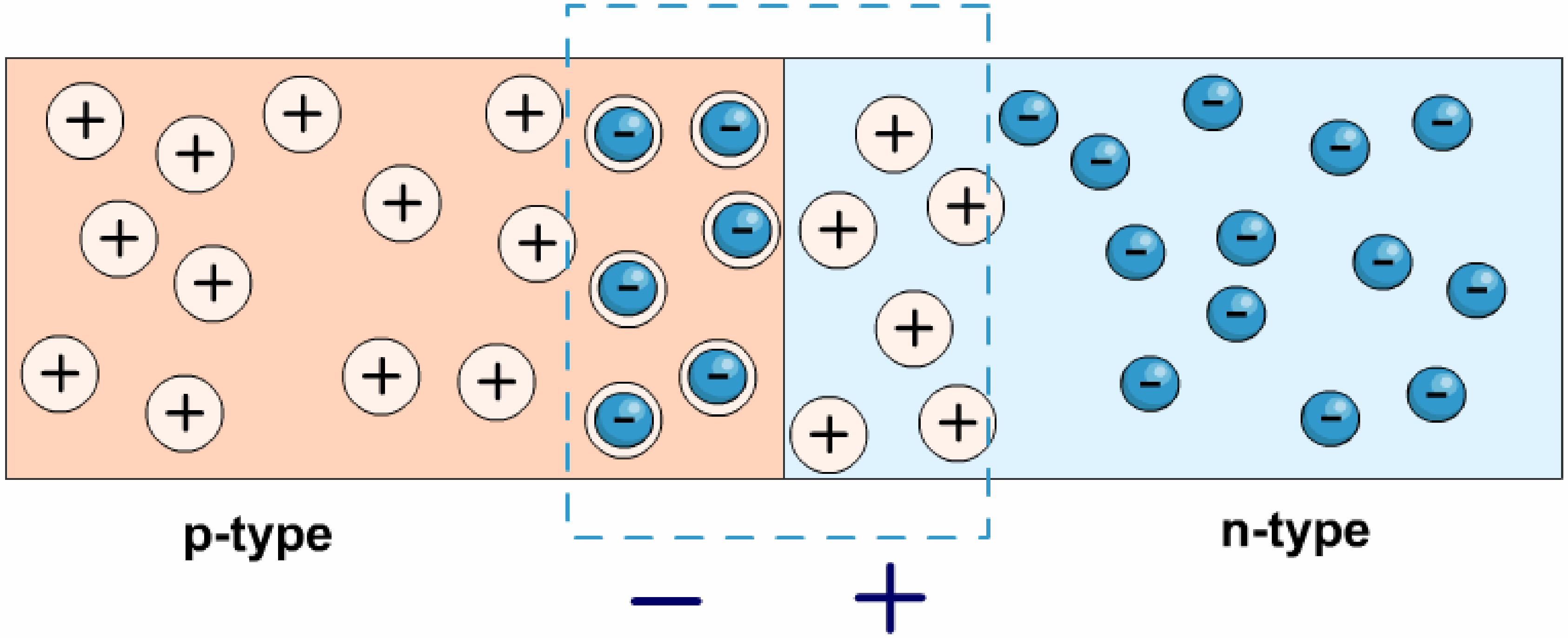


2. Depletion Region





Summary



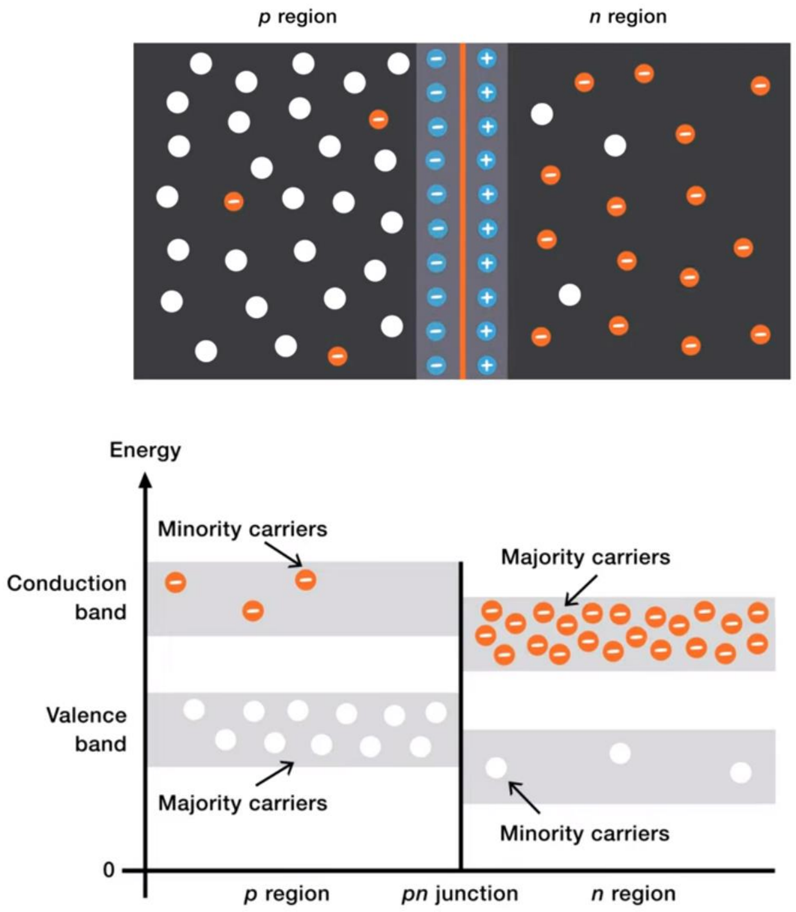
-Semiconductors n-type and p-type are brought together

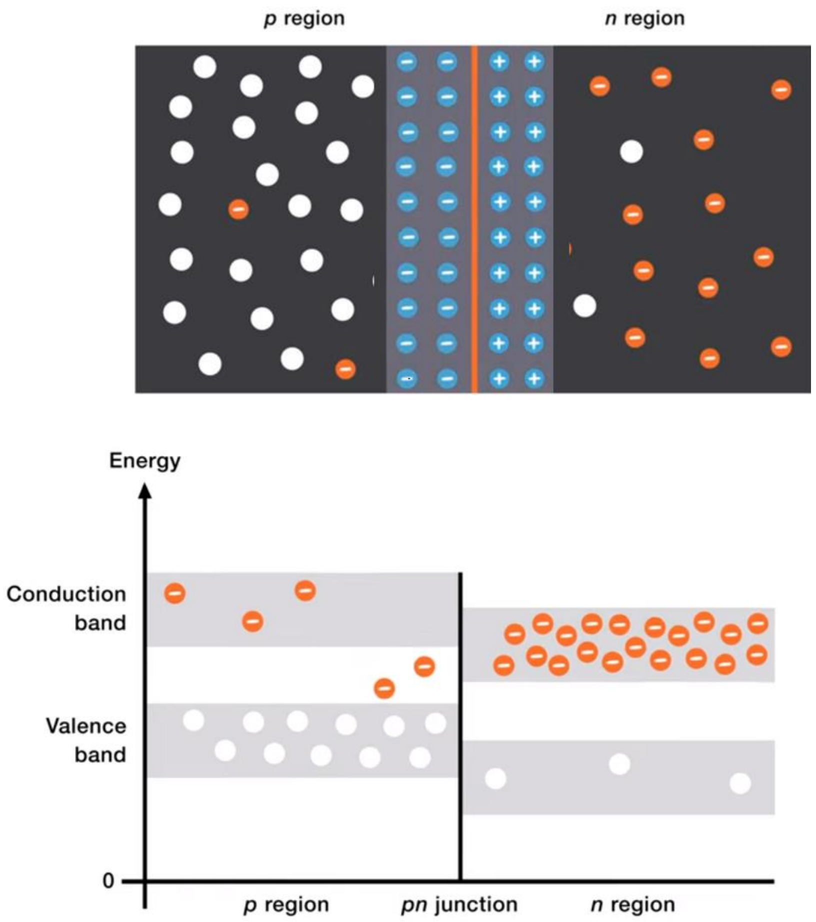
-Electrons and holes migrate across the junction

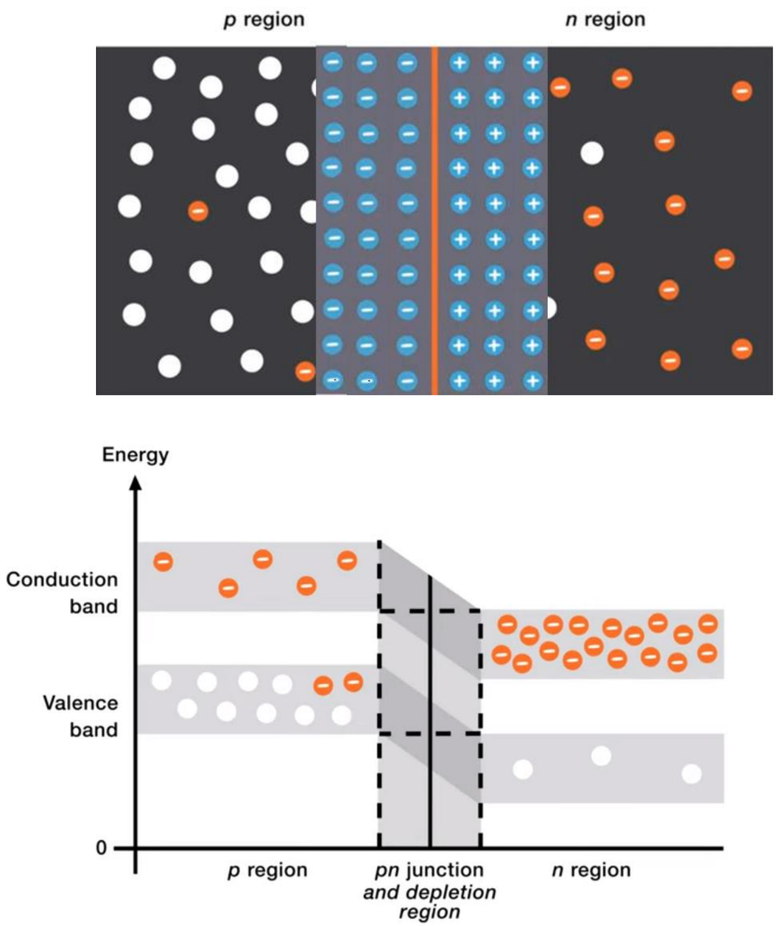
-The depletion layer is formed

-A p.d. is set up across the depletion layer

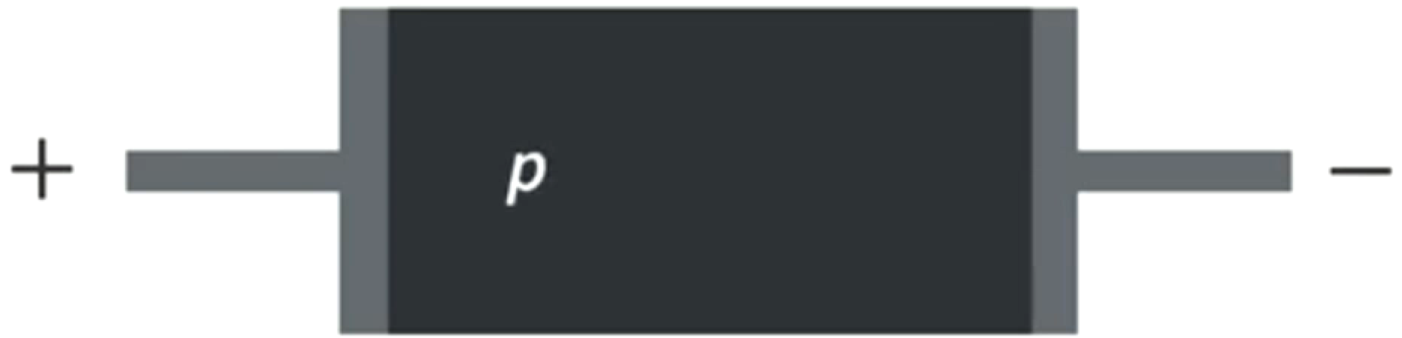
Unbiased PN Junction



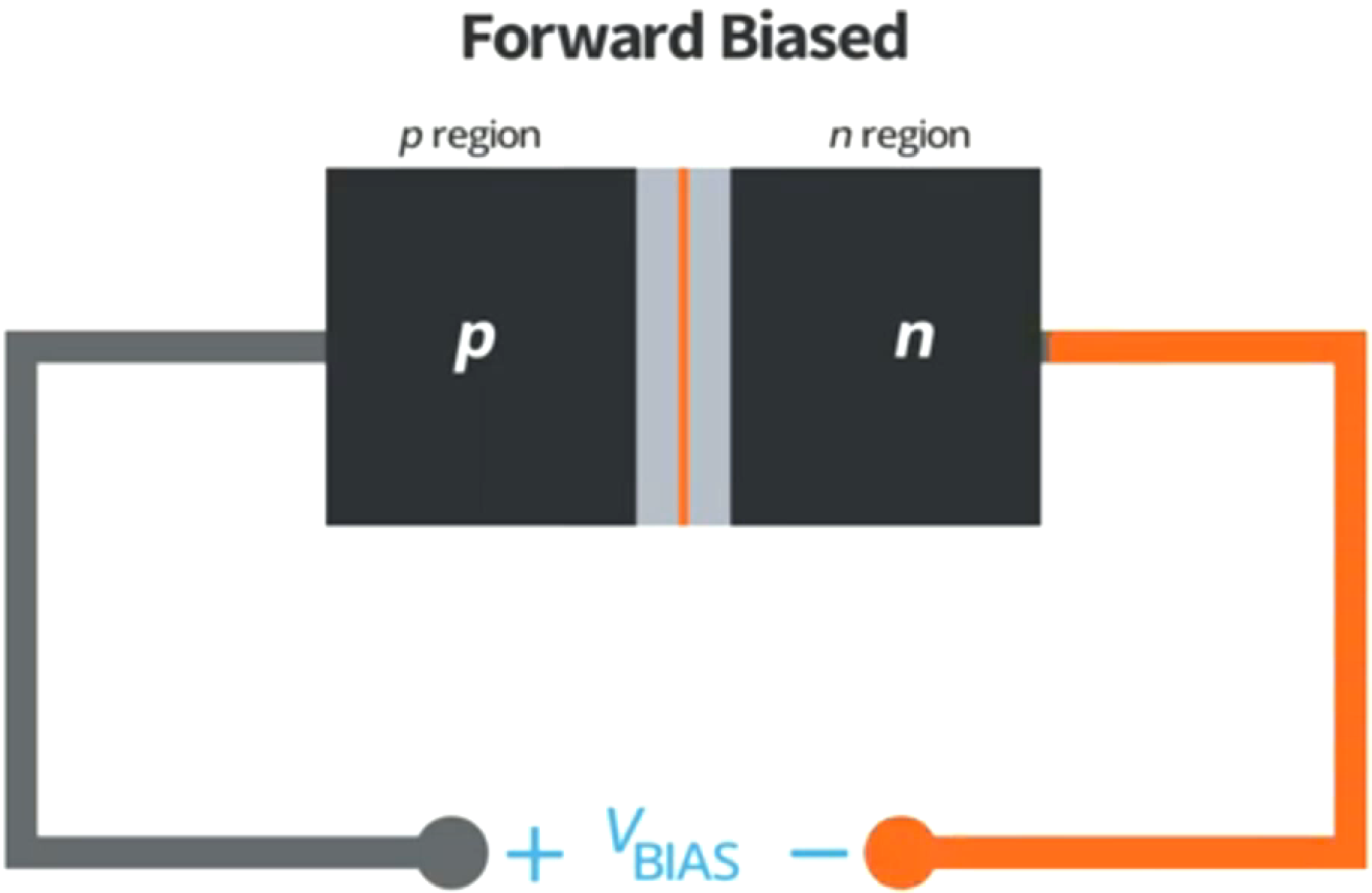




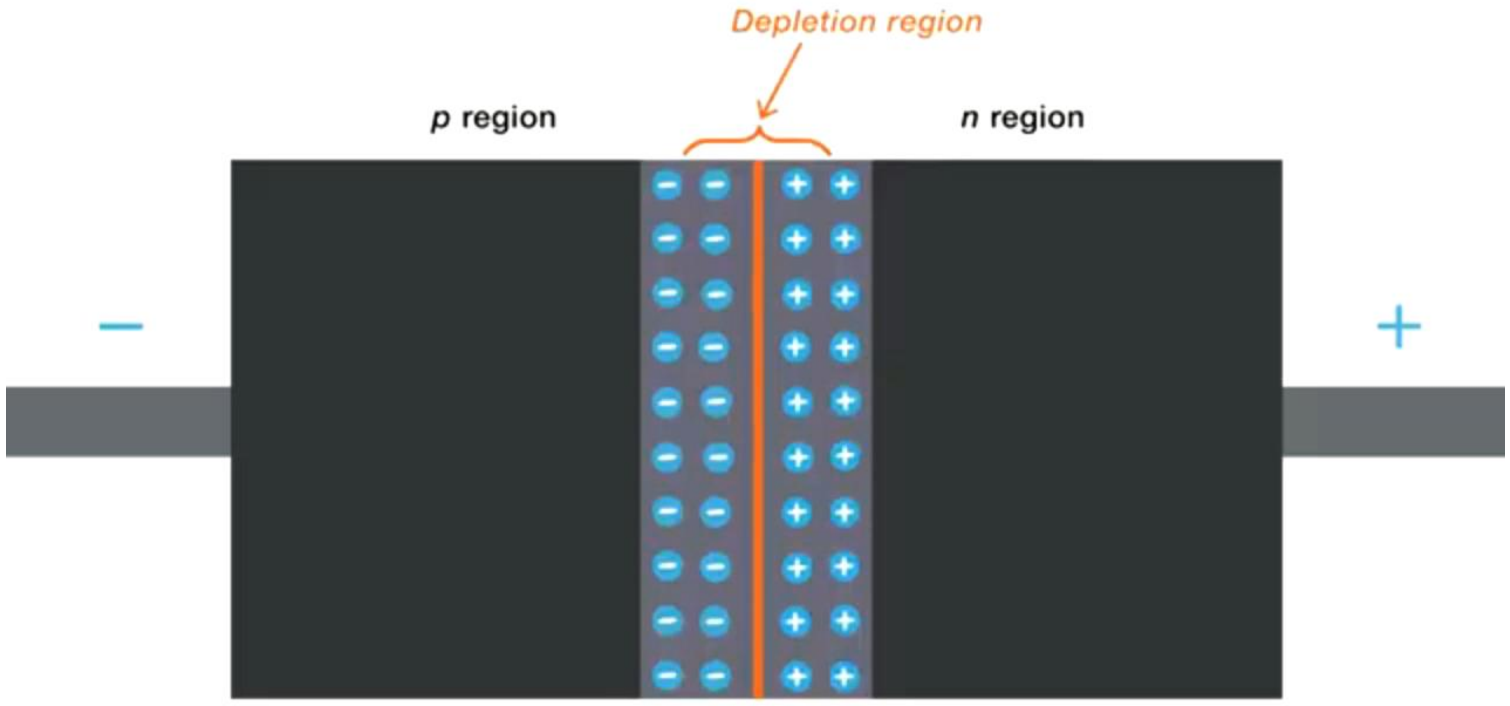
Biased PN Junction (forward bias)

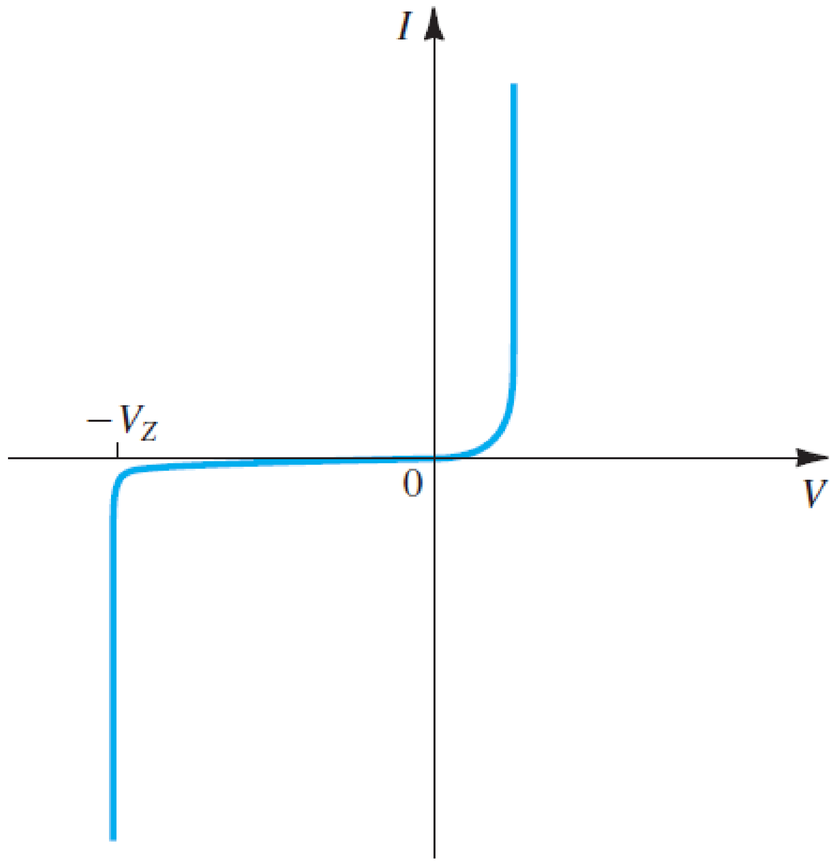


Biased PN Junction (Reverse bias)



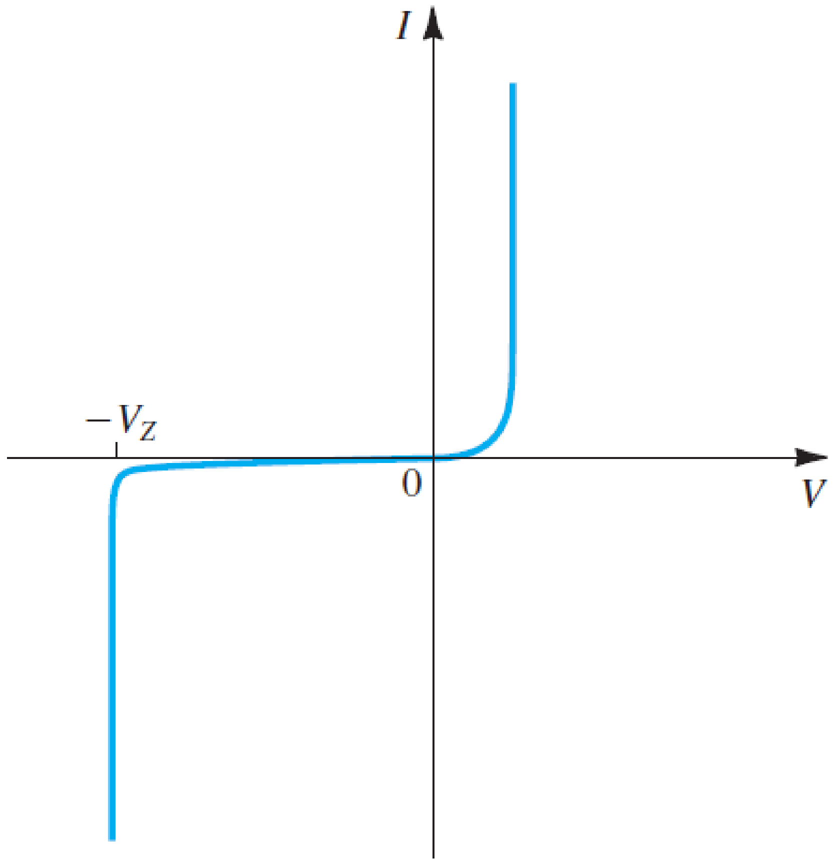
Biased PN Junction (Reverse bias)





Reverse Breakdown

The phenomenon that occurs at $V = VZ$ is known as **junction breakdown**. It is not a destructive phenomenon. That is, the *pn* junction can be repeatedly operated in the breakdown region without a permanent effect on its characteristics.



End