



VLSI FABRICATION TECHNOLOGY

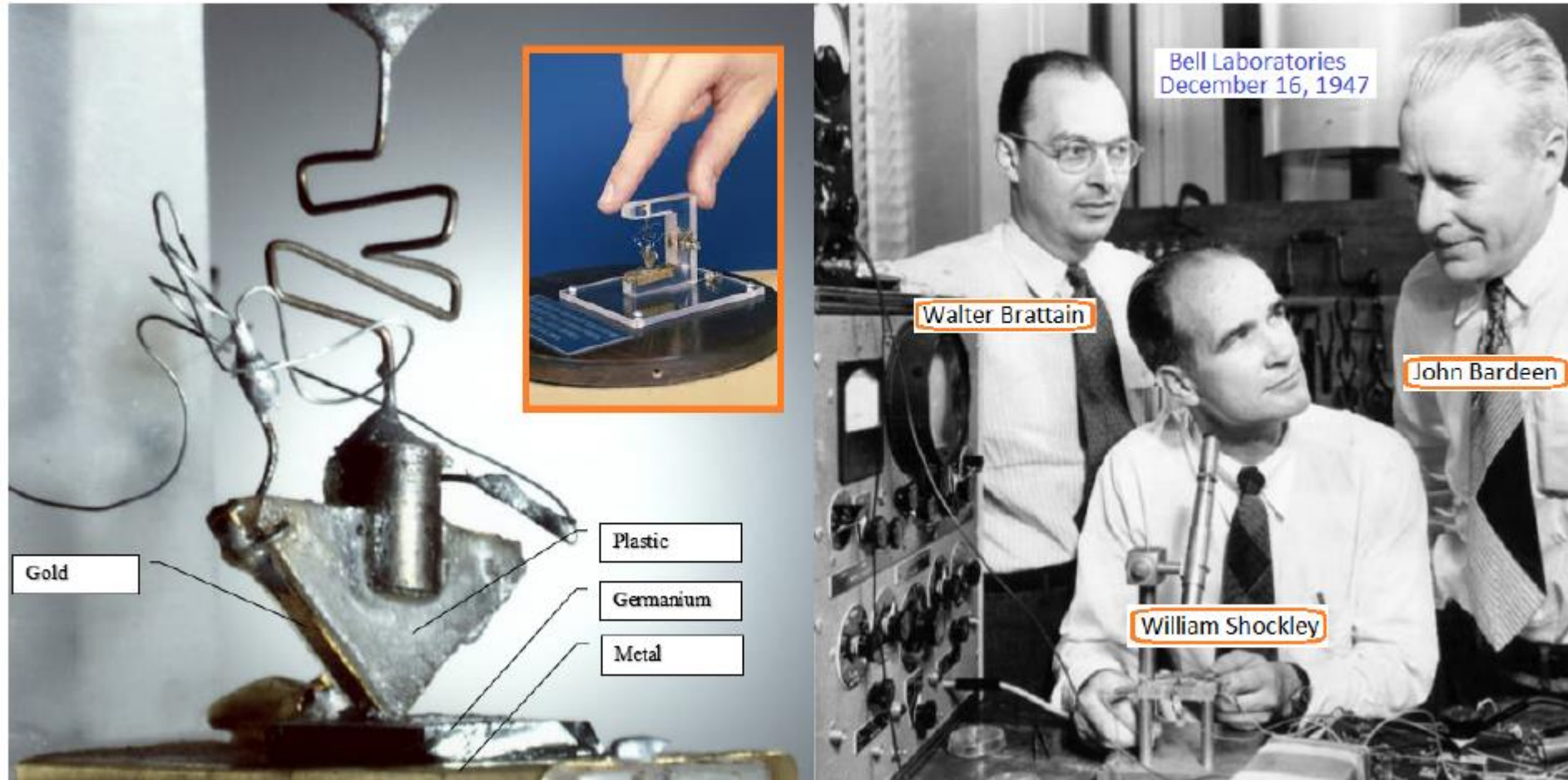
Dr. Mustafa Shiple



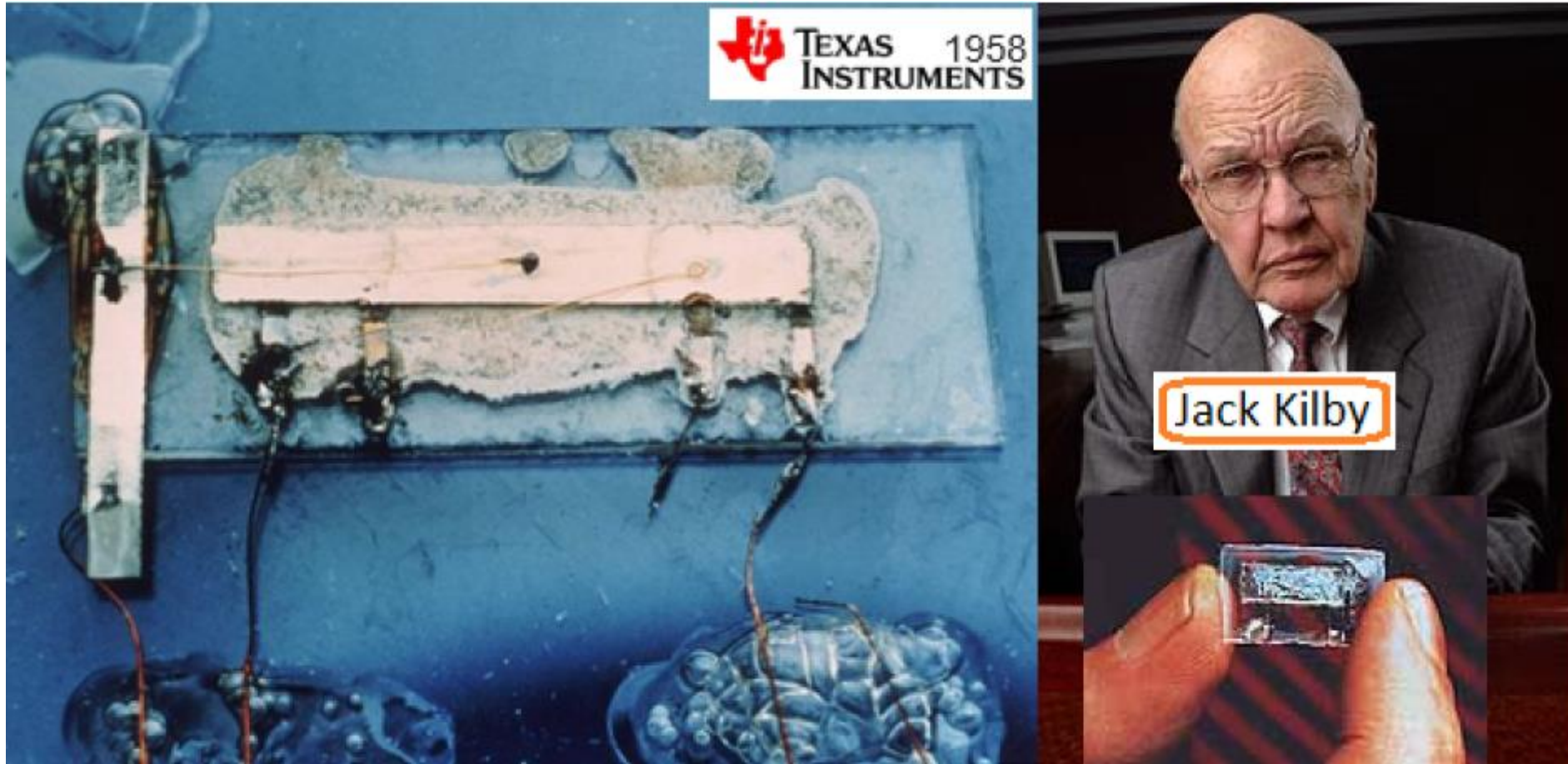
Agenda

- **Introduction**
- **Silicon IC processing**
 - Prearrangement
 - Doping Processes
 - Deposition Processes
 - Formation processes

First Point Contact Transistor



First integrated circuit

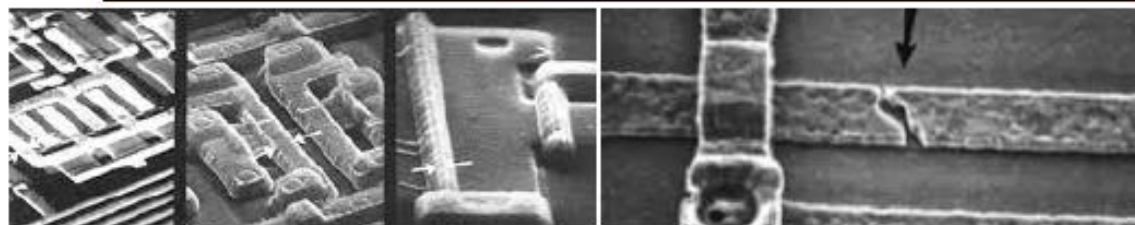
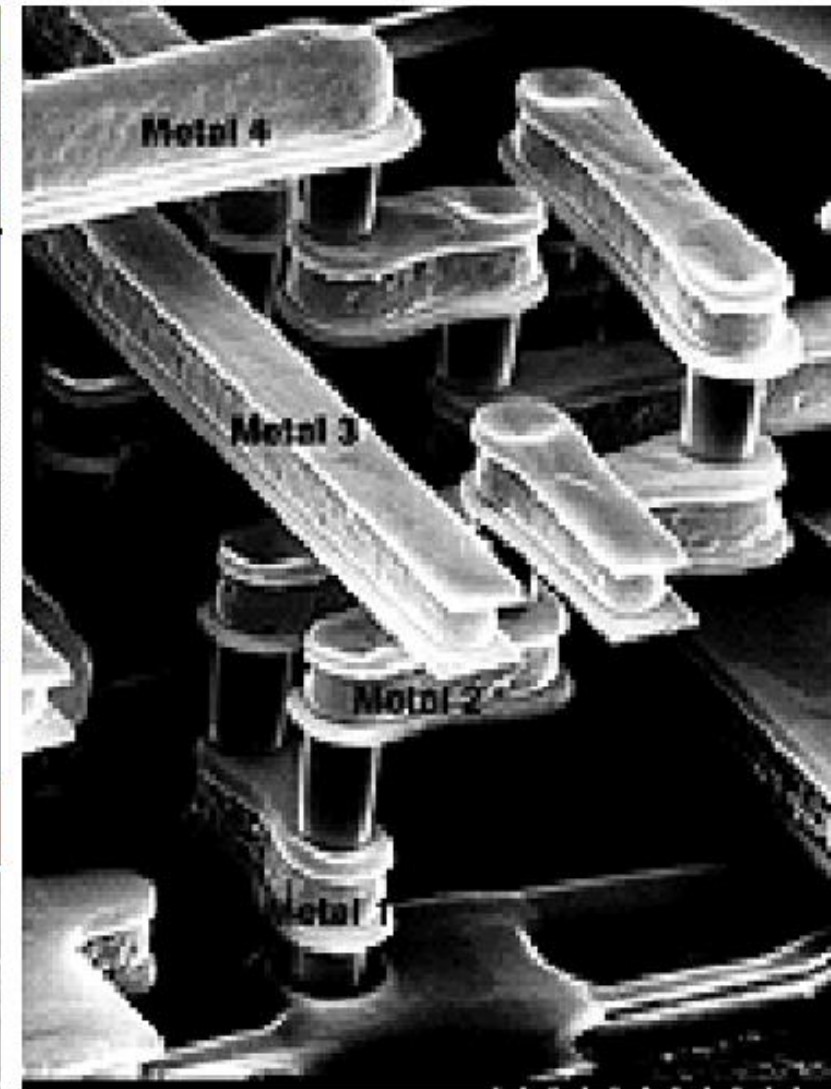
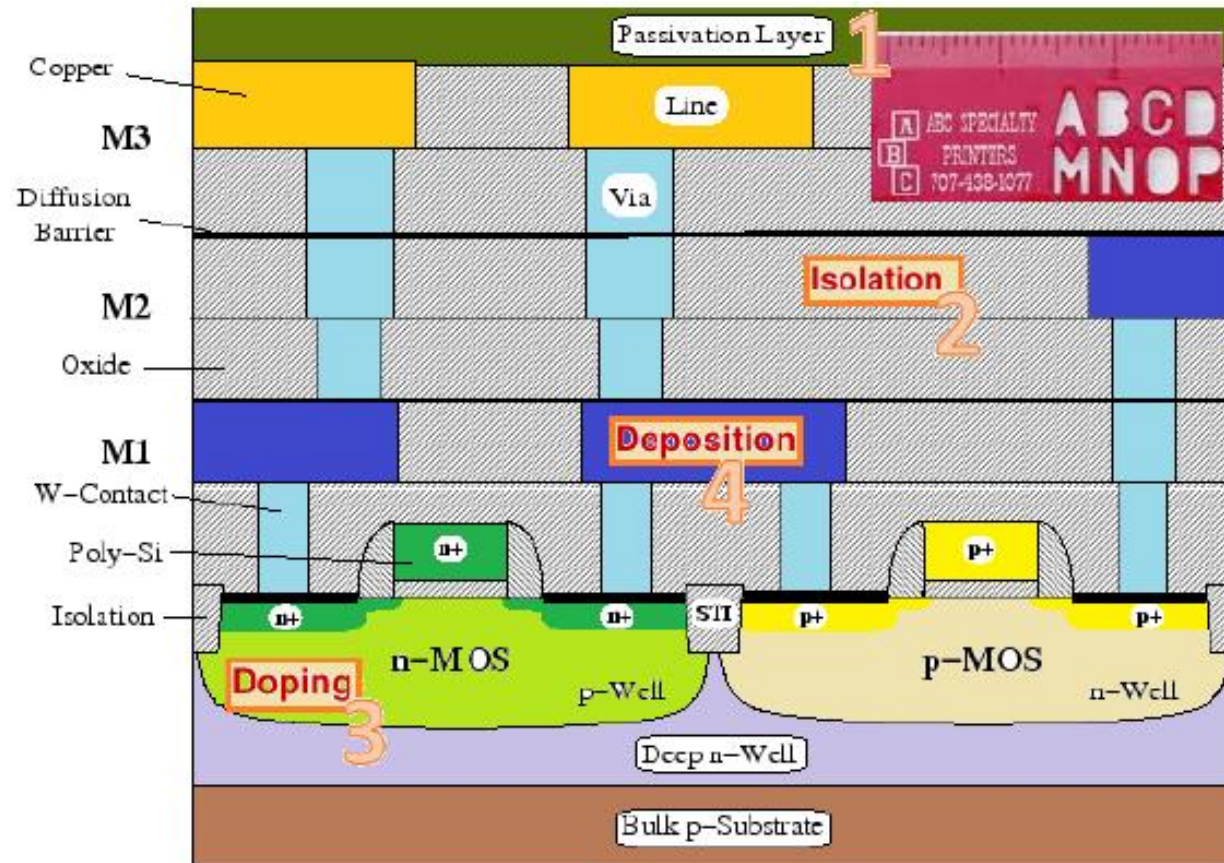


Kilby's idea was to make all the components and the chip out of the same block (monolith) of semiconductor material



Silicon IC processing

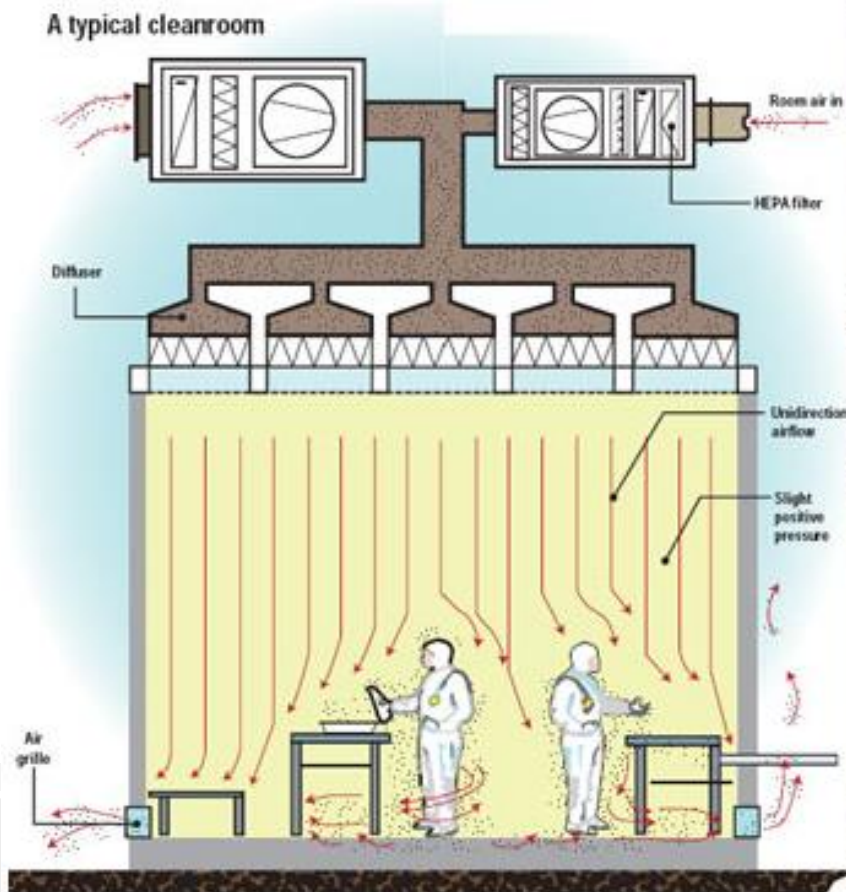
IC cross-section



Prearrangement (Clean Room)

Urban environment = 35,000,000 particles/ cm^3 of $\phi > 0.5\mu m$


Clean room = 12 particles/ cm^3 of $\phi < 0.3\mu m$



Prearrangement (*Silicon Material*)

Silicon is an abundant element and occurs naturally in the form of sand. It need to be **purified**¹ and **uniform**² crystal grow

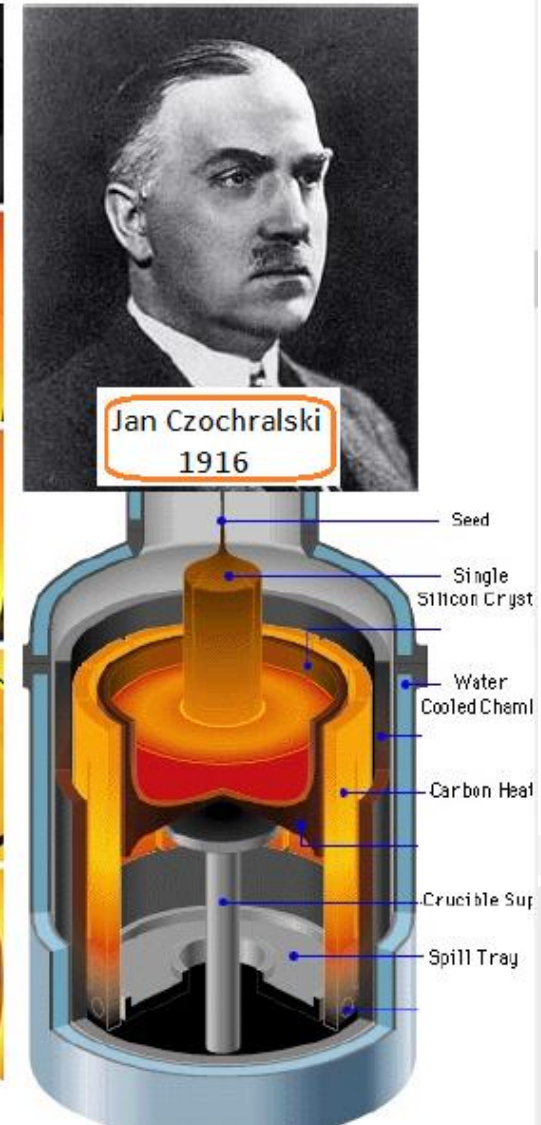
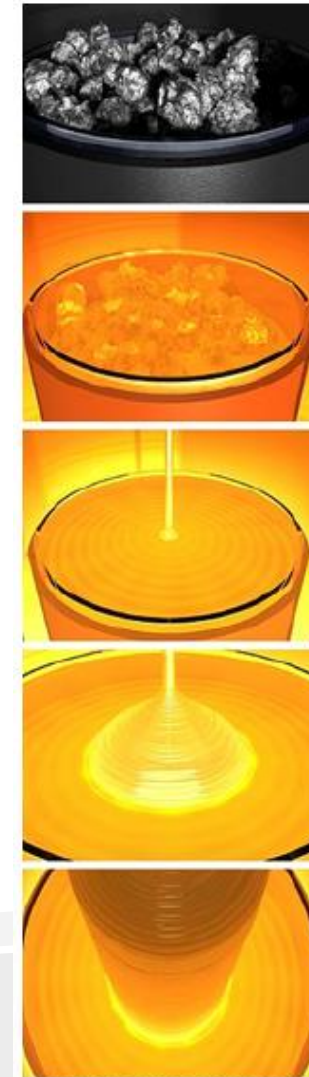
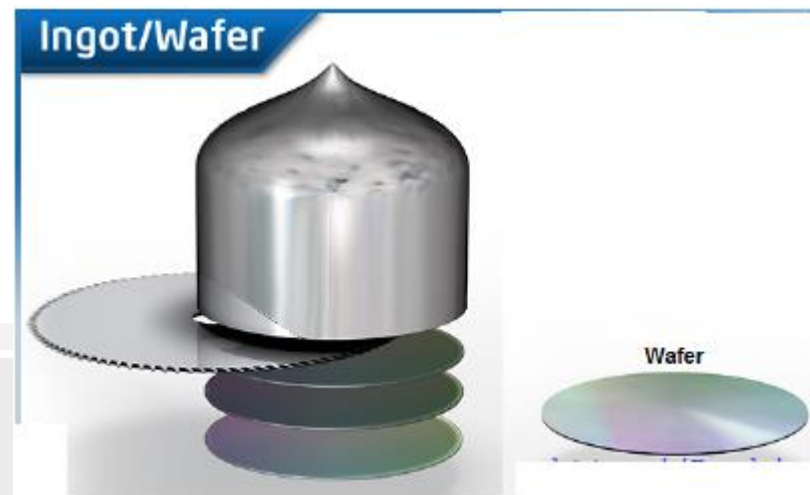
Periodic Table of the Elements



1 H Hydrogen 1.008																	2 He Helium 4.003
3 Li Lithium 6.941	4 Be Beryllium 9.012											5 B Boron 10.811	6 C Carbon 12.011	7 N Nitrogen 14.007	8 O Oxygen 15.999	9 F Fluorine 18.998	10 Ne Neon 20.180
11 Na Sodium 22.990	12 Mg Magnesium 24.305											13 Al Aluminum 26.982	14 Si Silicon 28.086	15 P Phosphorus 30.974	16 S Sulfur 32.065	17 Cl Chlorine 35.453	18 Ar Argon 39.948
19 K Potassium 39.098	20 Ca Calcium 40.078	21 Sc Scandium 44.956	22 Ti Titanium 47.867	23 V Vanadium 50.942	24 Cr Chromium 51.996	25 Mn Manganese 54.938	26 Fe Iron 55.845	27 Co Cobalt 58.933	28 Ni Nickel 58.693	29 Cu Copper 63.546	30 Zn Zinc 65.38	31 Ga Gallium 69.723	32 Ge Germanium 72.631	33 As Arsenic 74.922	34 Se Selenium 78.971	35 Br Bromine 79.904	36 Kr Krypton 84.798
37 Rb Rubidium 84.468	38 Sr Strontium 87.62	39 Y Yttrium 88.906	40 Zr Zirconium 91.224	41 Nb Niobium 92.906	42 Mo Molybdenum 95.95	43 Tc Technetium 98.907	44 Ru Ruthenium 101.07	45 Rh Rhodium 102.905	46 Pd Palladium 106.42	47 Ag Silver 107.868	48 Cd Cadmium 112.414	49 In Indium 114.818	50 Sn Tin 118.711	51 Sb Antimony 121.760	52 Te Tellurium 127.6	53 I Iodine 126.905	54 Xe Xenon 131.294
55 Cs Cesium 132.905	56 Ba Barium 137.328	57-71 Lanthanides	72 Hf Hafnium 178.49	73 Ta Tantalum 180.948	74 W Tungsten 183.84	75 Re Rhenium 186.207	76 Os Osmium 190.23	77 Ir Iridium 192.227	78 Pt Platinum 195.085	79 Au Gold 196.967	80 Hg Mercury 200.592	81 Tl Thallium 204.383	82 Pb Lead 207.2	83 Bi Bismuth 208.980	84 Po Polonium [209]	85 At Astatine [209]	86 Rn Radon [222]
87 Fr Francium [223]	88 Ra Radium [226]	89-103 Actinides	104 Rf Rutherfordium [261]	105 Db Dubnium [262]	106 Sg Seaborgium [266]	107 Bh Bohrium [264]	108 Hs Hassium [265]	109 Mt Meitnerium [268]	110 Ds Darmstadtium [271]	111 Rg Roentgenium [272]	112 Cn Copernicium [277]	113 Uut Ununtrium unknown	114 Fl Flerovium [289]	115 Uup Ununpentium unknown	116 Lv Livermorium [293]	117 Uus Ununseptium unknown	118 Uuo Ununoctium unknown
57 La Lanthanum 138.905	58 Ce Cerium 140.116	59 Pr Praseodymium 140.908	60 Nd Neodymium 144.242	61 Pm Promethium 144.913	62 Sm Samarium 150.36	63 Eu Europium 151.964	64 Gd Gadolinium 157.25	65 Tb Terbium 158.925	66 Dy Dysprosium 162.503	67 Ho Holmium 164.930	68 Er Erbium 167.258	69 Tm Thulium 168.934	70 Yb Ytterbium 173.055	71 Lu Lutetium 174.967			
89 Ac Actinium 227.028	90 Th Thorium 232.038	91 Pa Protactinium 231.036	92 U Uranium 238.029	93 Np Neptunium 237.048	94 Pu Plutonium 244.064	95 Am Americium 243.061	96 Cm Curium 247.070	97 Bk Berkelium 247.070	98 Cf Californium 251.083	99 Es Einsteinium [254]	100 Fm Fermium [257]	101 Md Mendelevium [258]	102 No Nobelium [259]	103 Lr Lawrencium [262]			

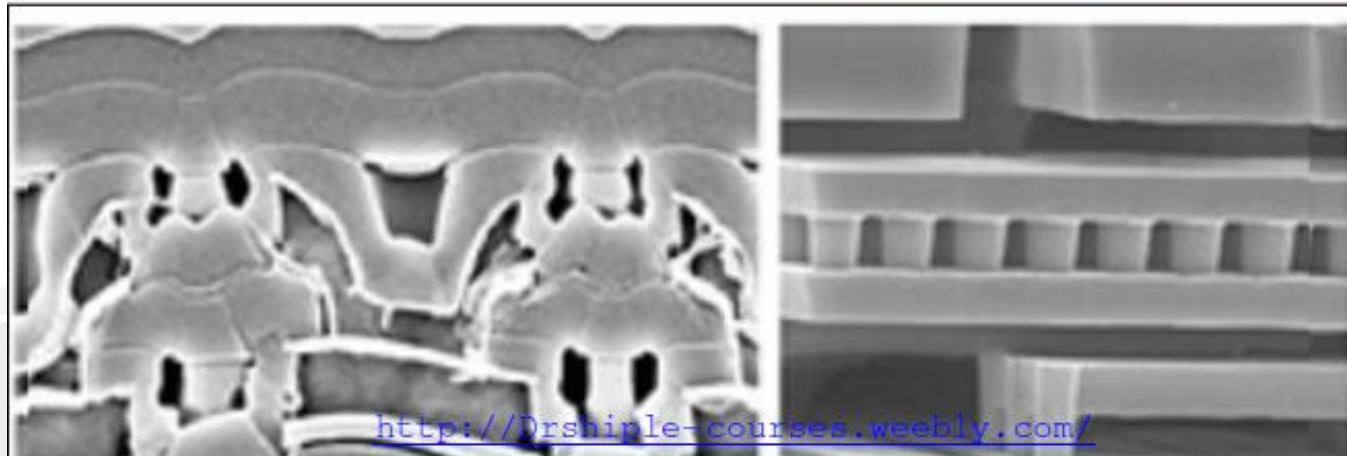
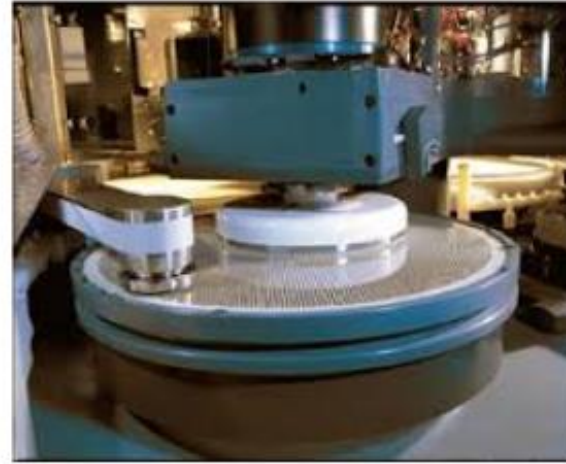
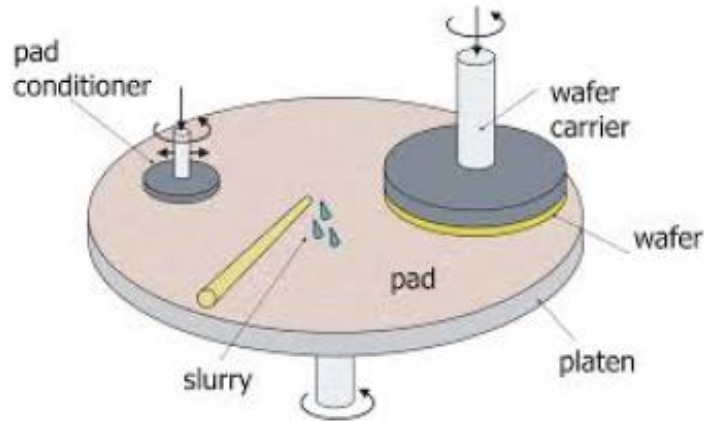
Prearrangement (*Czochralski process*)

1. Melt silicon at 1425°C
2. Add impurities (dopants substrate)
3. Spin and pull crystal
4. Slice into wafers ($400\ \mu\text{m}$ to $600\ \mu\text{m}$) thick.
5. Polish one side (Using chemical and mechanical polishing (CMP) techniques)



Prearrangement (Chemical Mechanical Polishing (CMP))

1. Mechanical polishing component and Chemical reaction component.
2. Goal: to planarize the surface of the wafer prior to photolithography.
3. abrasive chemical solution (slurry), is introduced between a polishing pad and the wafer.

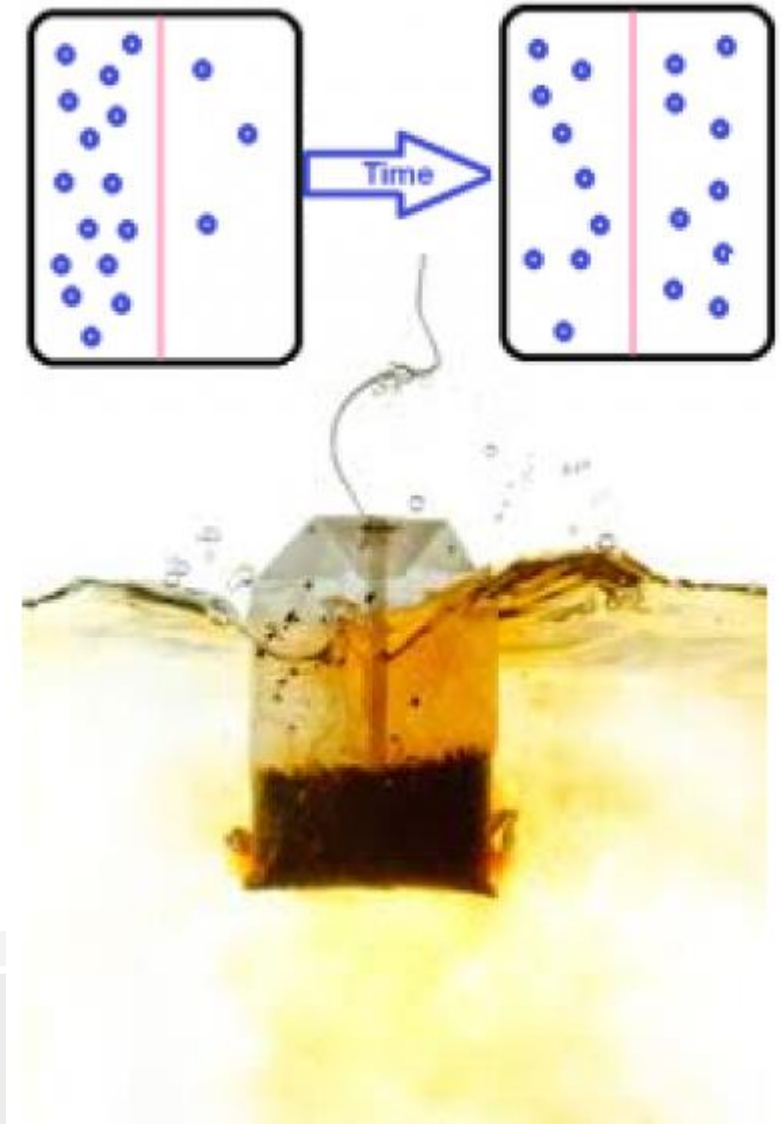




Doping Processes

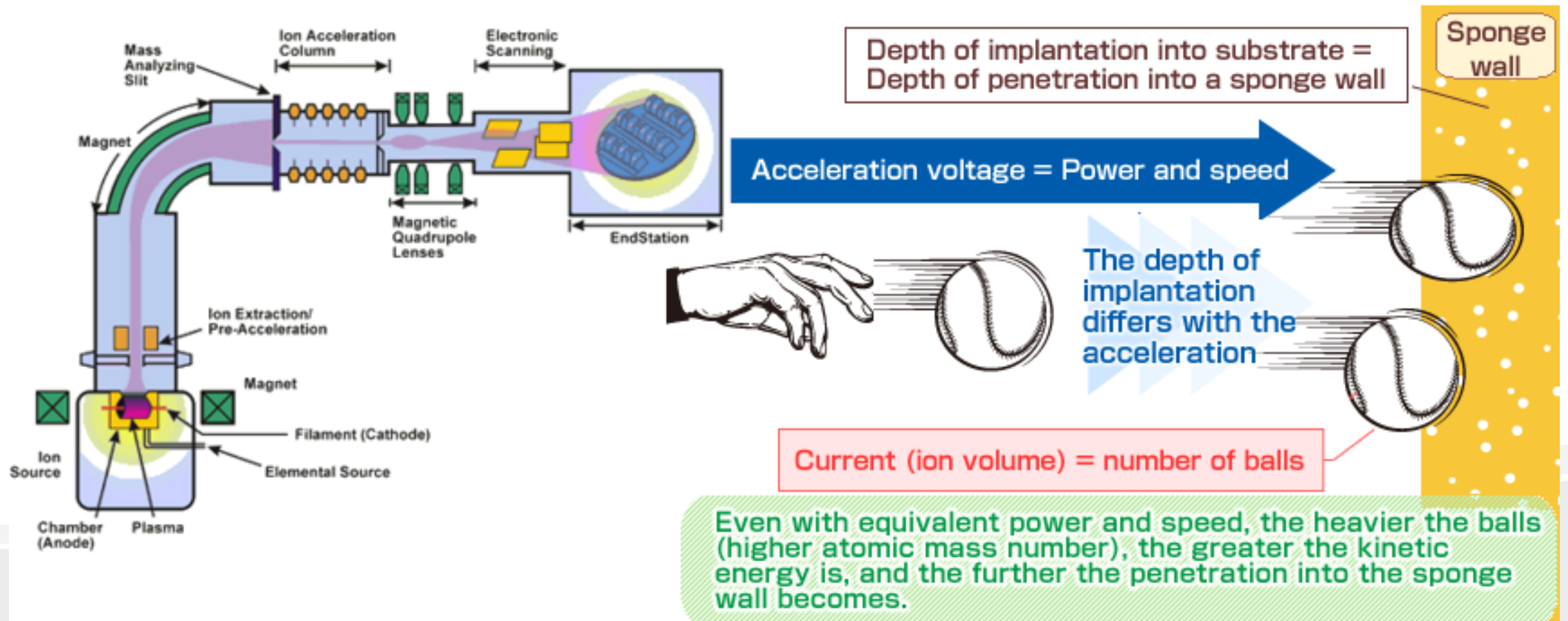
Solid State Diffusion

1. Diffusion is a process by which atoms move from a high-concentration region to a low concentration region.
2. this method introduces impurity atoms (dopants) into silicon to
3. change its resistivity.
4. The most common impurities used as dopants are boron (p-type), phosphorus(n-type), and arsenic(n-type).
5. Solid state diffusion inherently occurs in **high temperature** steps.



Ion Implantation

An ion implanter produces ions of the desired dopant, accelerates them by an electric field, and allows them to strike the semiconductor surface



Diffusion vs. Ion Implantation

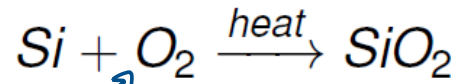
<i>Diffusion</i>	<i>Ion Implantation</i>
Introducing impurities to semiconductors	
Based on concentration gradient	Injecting an energetic ion beam
A high-temperature process	A low-temperature process
Uncontrollable	Dopant concentration could be controlled
Isotropic dopant profile	Anisotropic dopant profile
Limited to solid solubility	leads to a high degree of lattice damage
Need thick layers	Possible through the thin layers



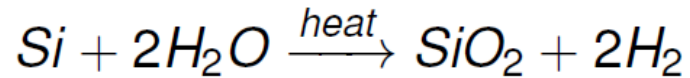
Deposition Processes

Oxidation Isolation

In oxidation, silicon reacts with oxygen to form silicon dioxide (SiO_2).
(ultra clean furnaces 1000-1200 °C)



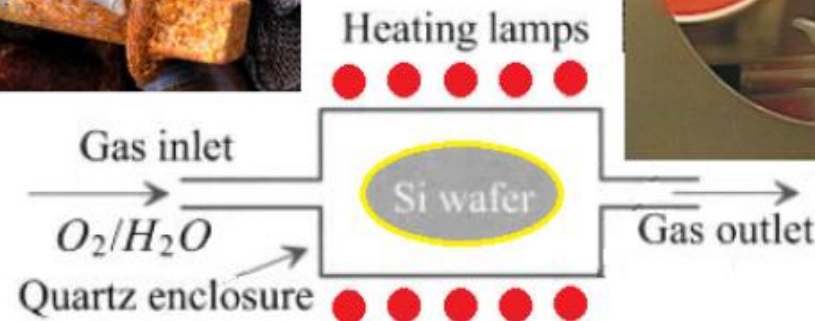
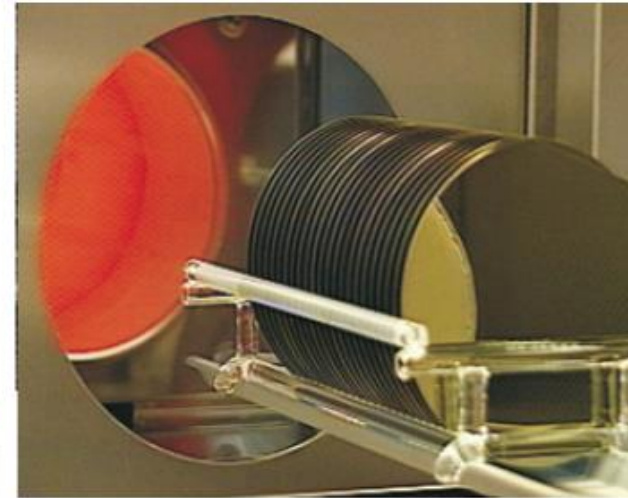
(dry oxidation) (1)



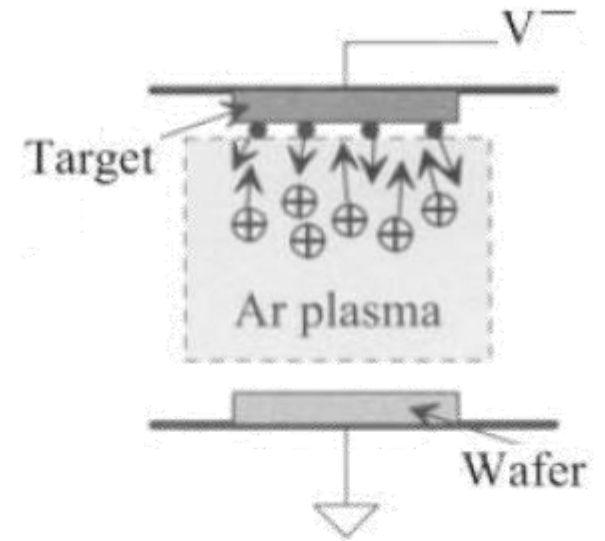
(wet oxidation) (2)

high-purity gas

steam

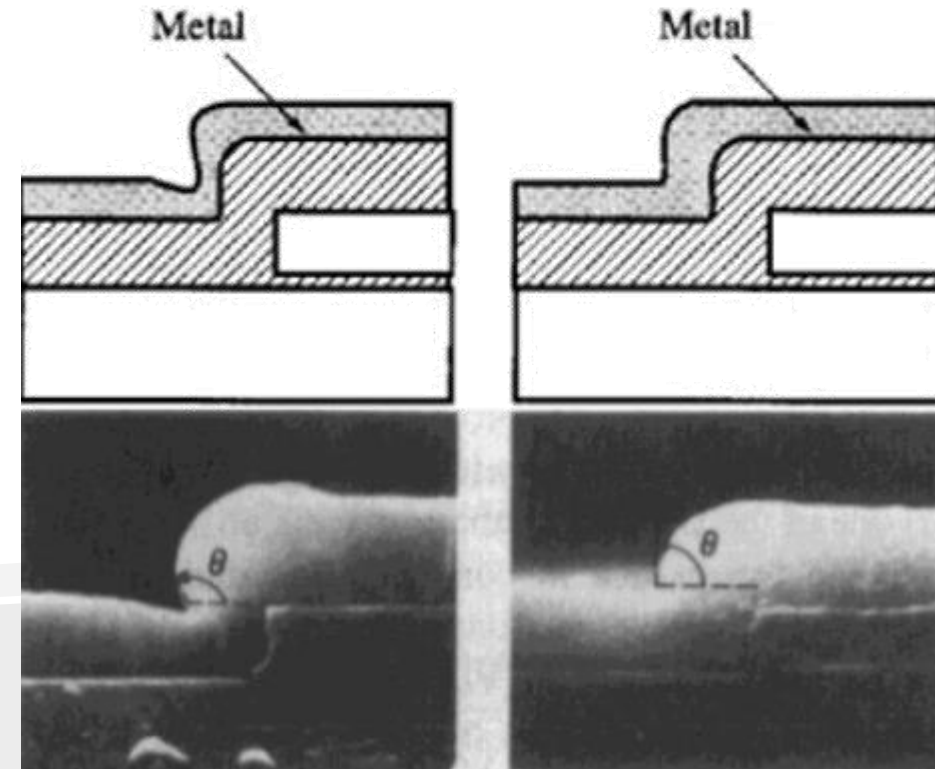


Physical Vapor Deposition (PVD)



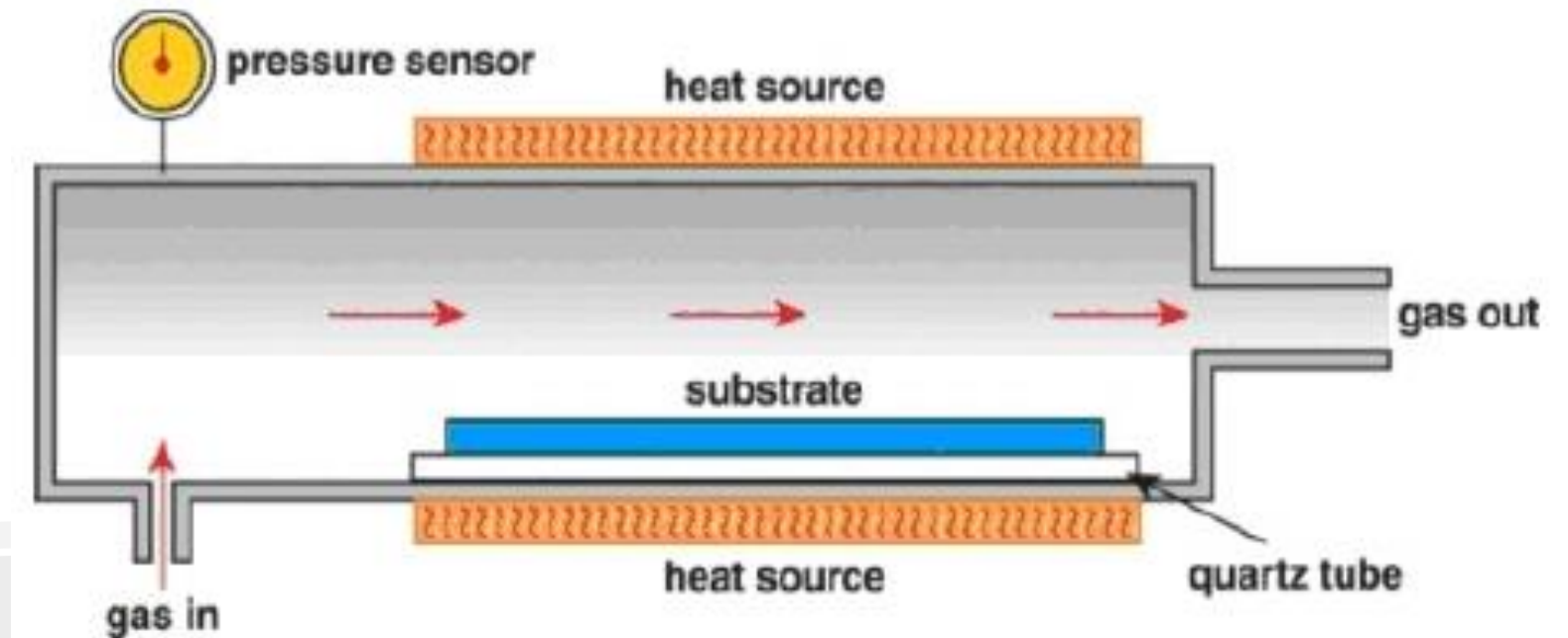
Sputter Deposition

1. Gas (e.g., argon)
2. Positively ionized
3. Accelerated through an electric field
4. Target metal sits on the cathode
5. Bombarded by the positively charged ions
6. Material to be ejected off (mechanically) to wafer
7. Poor step coverage



Chemical Vapor Deposition (CVD)

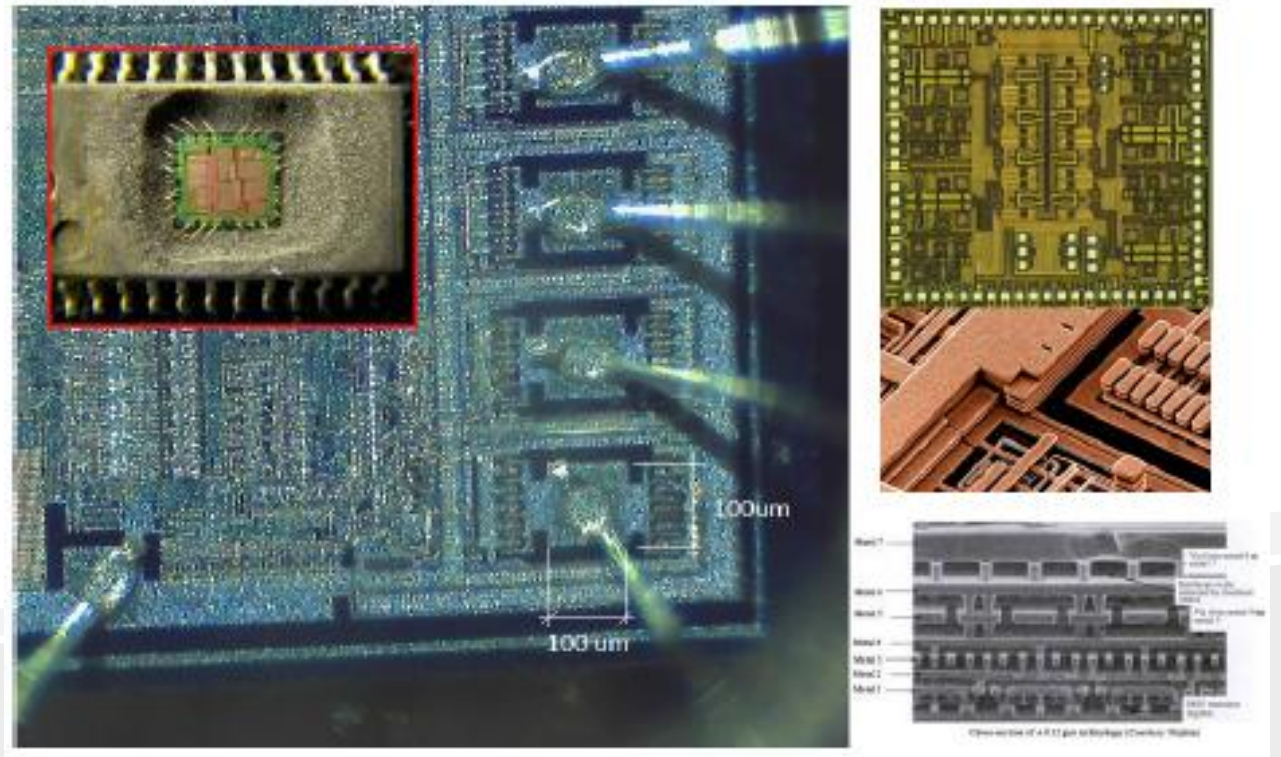
is a process by which gases or vapors are , leading to the formation of solids on a substrate. CVD can be used to deposit various materials on a silicon substrate including SiO_2 , Si_3N_4 , polysilicon



Metallization

Metallization is the process by which the components of IC's are interconnected by aluminum conductor polysilicon. CVD is used for metallization.

1. Interconnect the various components on the chip.
2. bonding pads.

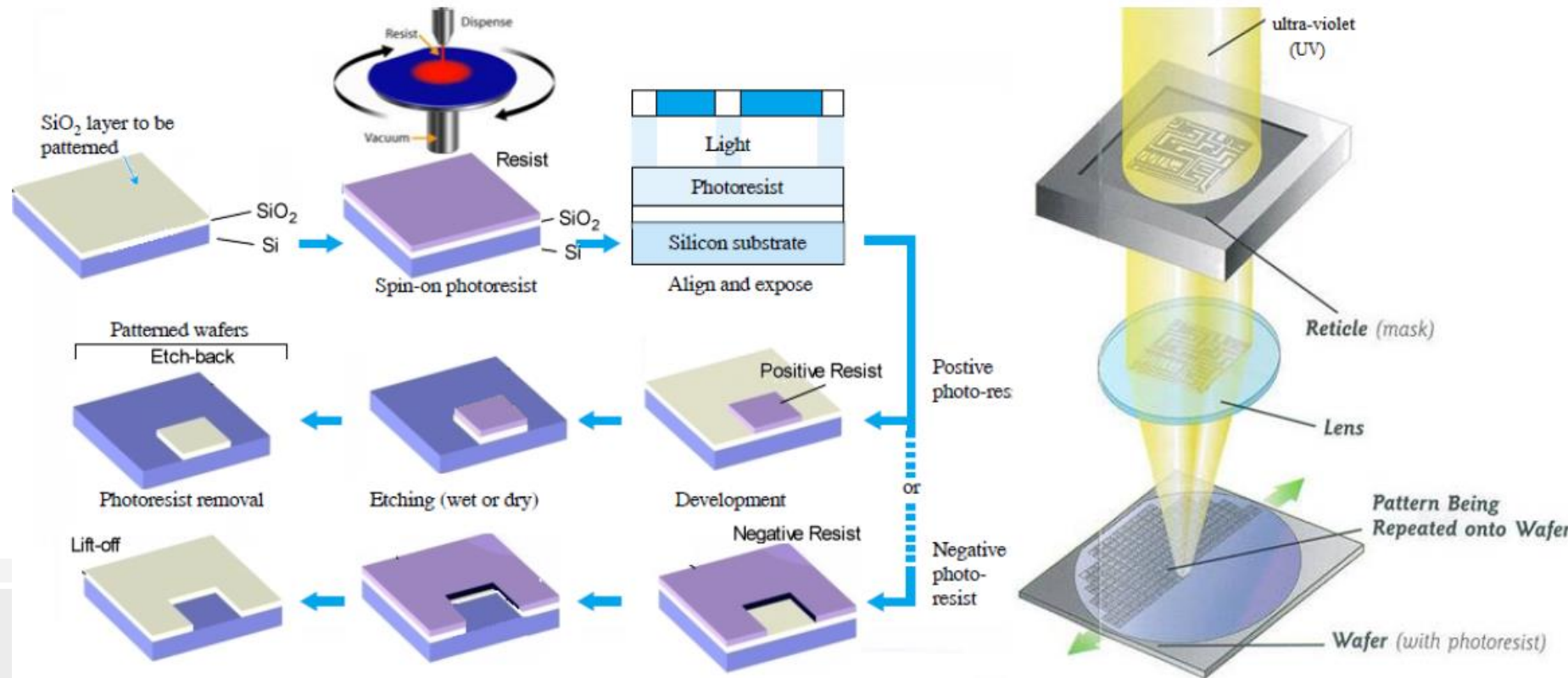




Formation processes

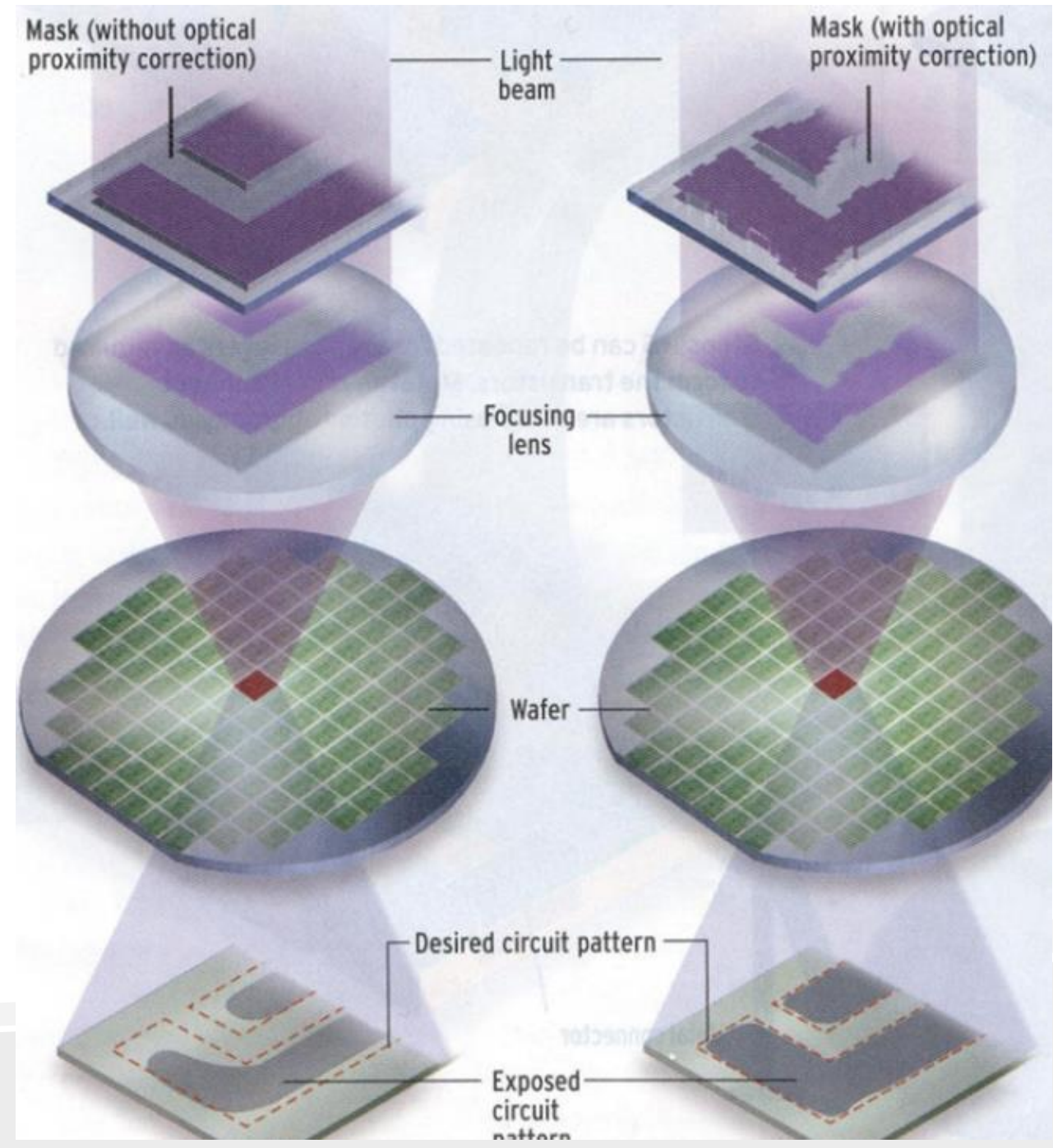
Photolithography

is the process of transferring geometric shapes on a mask to the surface of a silicon wafer. (ultraviolet light + a mask + a light-sensitive chemical resistant polymer). By dropping photoresist to a rotating wafer yielding a uniform thin film on the surface.



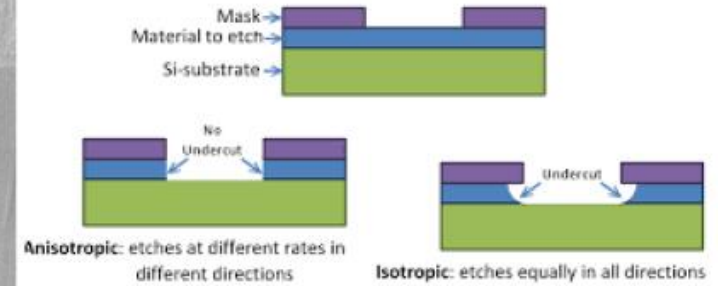
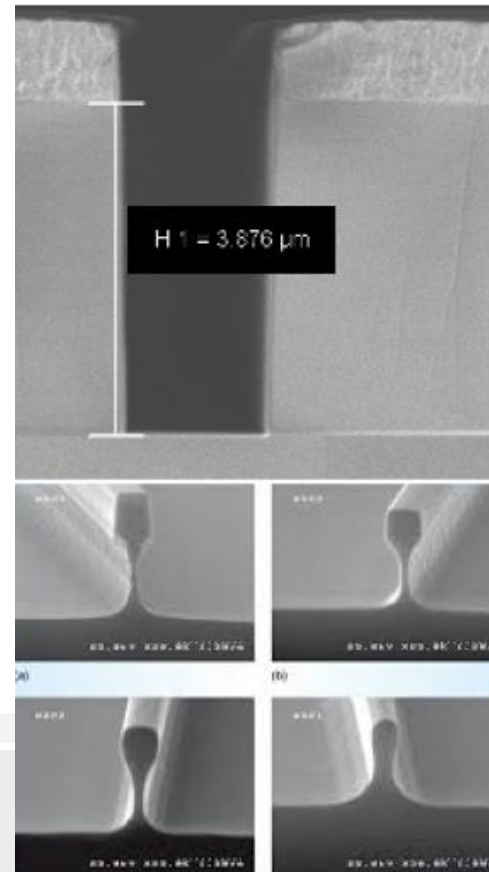
Mask (Reticle)

numerous mask levels (e.g., active, poly, contacts, etc.) are printed on the wafer.

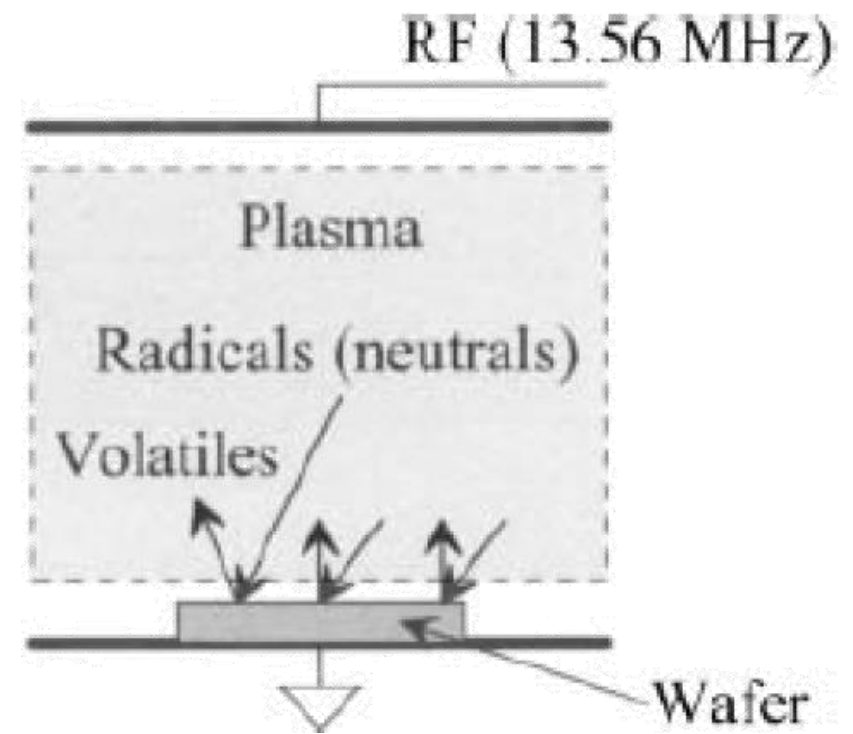
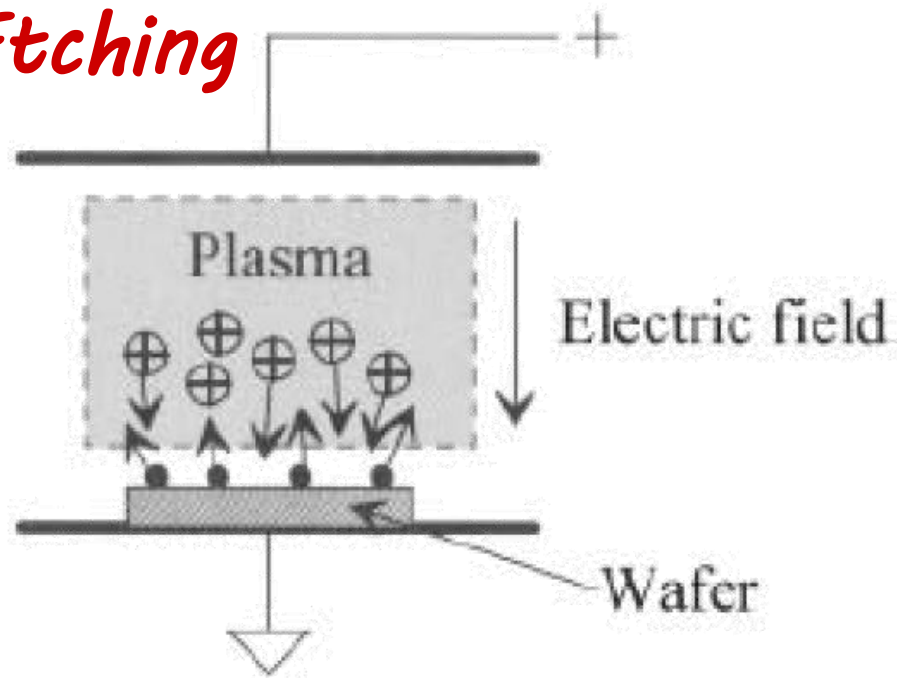


Wet Etching

Isotropy and anisotropy: When a material is attacked by a liquid or vapor etchant, it is removed isotropically (uniformly in all directions) or anisotropic etching (uniformity in vertical direction)



Dry Etching



Sputter (sound) etching	Plasma etch
Gas (e.g., argon)	Gas or mixture of gases (e.g., halogens)
Positively ionized	Ionized producing reactive species (radicals)
Accelerated through an electric field	
Wafer sits on the cathode	Wafer sits on the cathode
Bombarded by the positively charged ions	Radicals chemically react with surface
Material to be ejected off (mechanically)	Material forming reaction products in the gas phase
Not selective and anisotropic.	Highly selective and isotropic

Dry Etching

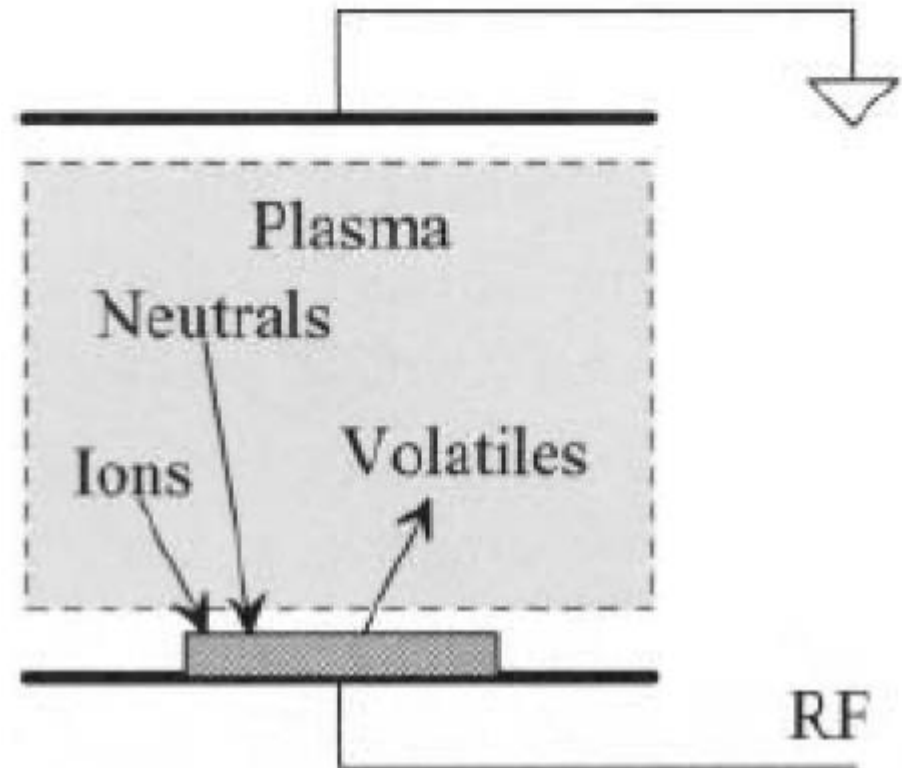
Reactive ion etching (RIE)

Combination of sputter etching and plasma etching

Radicals and ionized species are generated

Wafer sits on the cathode

Highly selective and highly anisotropic





Wet/Dry Etching

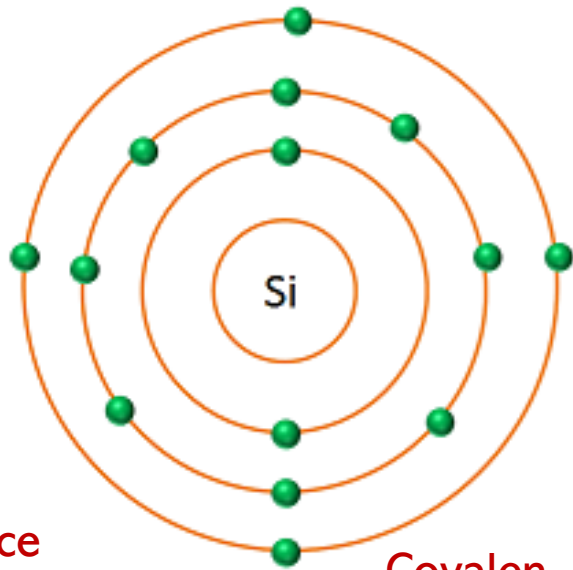
Wet etching	Dry etching
Removal of metals, semiconductors, and insulators	
Isotropic and anisotropic	Higher degree of anisotropy
Using a chemical solution	
Cleaning of wafers	
Rinsed in deionized (DI) water	



PN Junction

“Microelectronic Circuits” , Adel Sedra

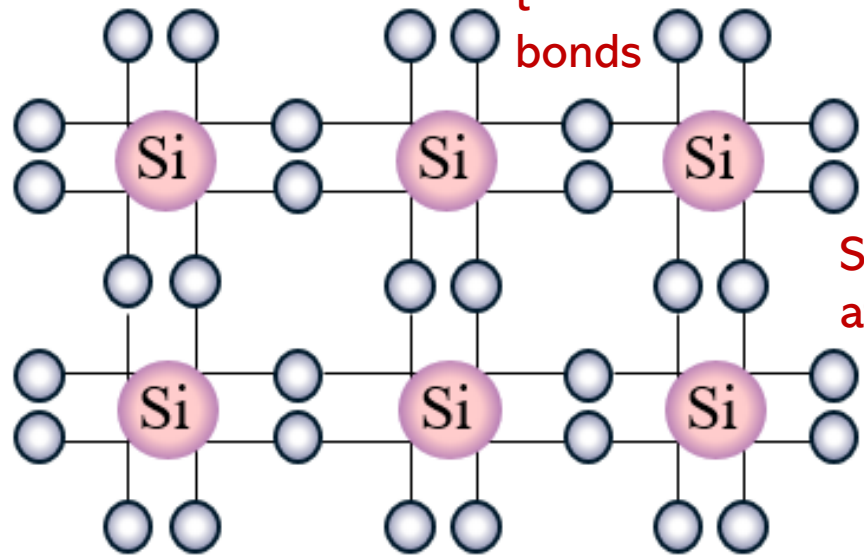
Intrinsic Semiconductors



Valence electrons

Covalent bonds

Silicon atoms



14 ← Atomic number

Si ← Symbol

Silicon ← Name

[Ne] 3s²3p² ← Electron configuration

Metalloid

													13	14	15	16	17	18
													5	6	7	8	9	10
													B Boron	C Carbon	N Nitrogen	O Oxygen	F Fluorine	Ne Neon
													13	14	15	16	17	18
													Al Aluminium	Si Silicon	P Phosphorus	S Sulfur	Cl Chlorine	Ar Argon
5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20			
23 Va Vanadium	24 Cr Chromium	25 Mn Manganese	26 Fe Iron	27 Co Cobalt	28 Ni Nickel	29 Cu Copper	30 Zn Zinc	31 Ga Gallium	32 Ge Germanium	33 As Arsenic	34 Se Selenium	35 Br Bromine	36 Kr Krypton	37	38			
41 Nb Niobium	42 Mo Molybdenum	43 Tc Technetium	44 Ru Ruthenium	45 Rh Rhodium	46 Pd Palladium	47 Ag Silver	48 Cd Cadmium	49 In Indium	50 Sn Tin	51 Sb Antimony	52 Te Tellurium	53 I Iodine	54 Xe Xenon	55	56			
73 Ta Tantalum	74 W Tungsten	75 Re Rhenium	76 Os Osmium	77 Ir Iridium	78 Pt Platinum	79 Au Gold	80 Hg Mercury	81 Tl Thallium	82 Pb Lead	83 Bi Bismuth	84 Po Polonium	85 At Astatine	86 Rn Radon	87	88			
105 Db Dubnium	106 Sg Seaborgium	107 Bh Bohrium	108 Hs Hassium	109 Mt Meitnerium	110 Ds Darmstadtium	111 Rg Roentgenium	112 Cn Copernicium	113 Nh Nihonium	114 Fl Flerovium	115 Mc Moscovium	116 Lv Livermorium	117 Ts Tennessine	118 Og Oganesson	119	120			

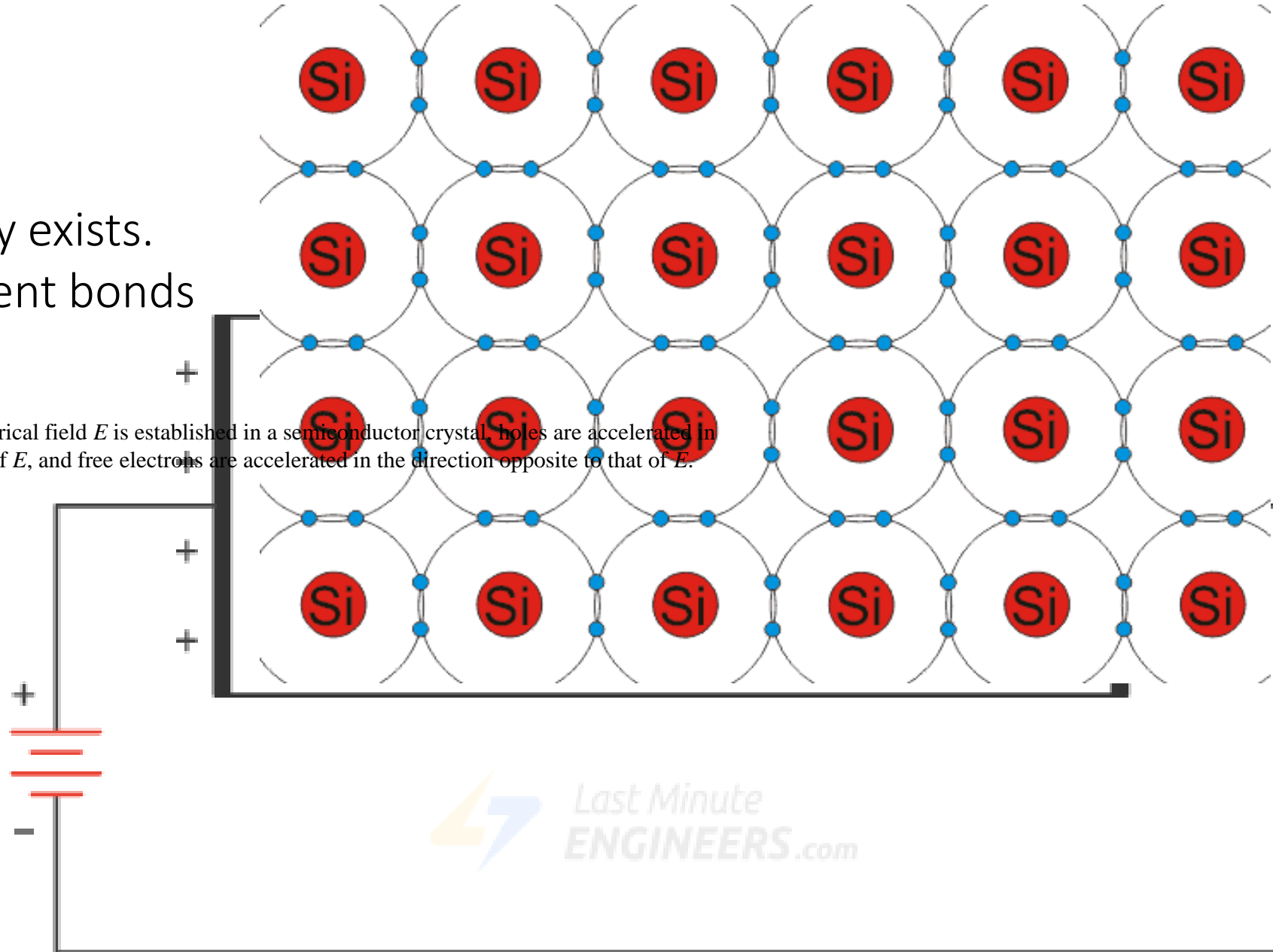
59 Pr Praseodymium	60 Nd Neodymium	61 Pm Promethium	62 Sm Samarium	63 Eu Europium	64 Gd Gadolinium	65 Tb Terbium	66 Dy Dysprosium	67 Ho Holmium	68 Er Erbium	69 Tm Thulium	70 Yb Ytterbium	71 Lu Lutetium
91 Pa Protactinium	92 U Uranium	93 Np Neptunium	94 Pu Plutonium	95 Am Americium	96 Cm Curium	97 Bk Berkelium	98 Cf Californium	99 Es Einsteinium	100 Fm Fermium	101 Md Mendelevium	102 No Nobelium	103 Lr Lawrencium

Thermal Generation

1. At room temperature
2. Sufficient thermal energy exists.
3. Break some of the covalent bonds

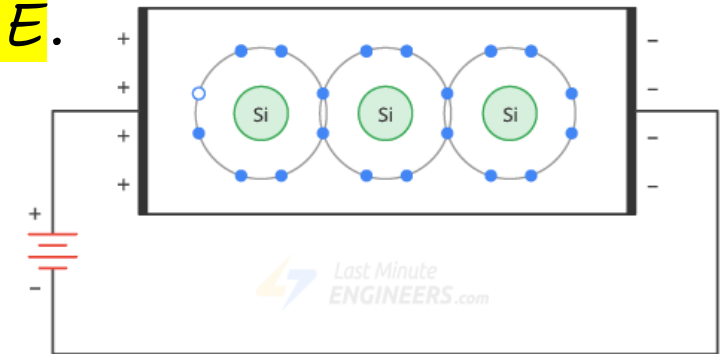
When an electrical field E is established in a semiconductor crystal, holes are accelerated in the direction of E , and free electrons are accelerated in the direction opposite to that of E .

If a voltage is applied, then both the electron and the hole can contribute to a small current flow.



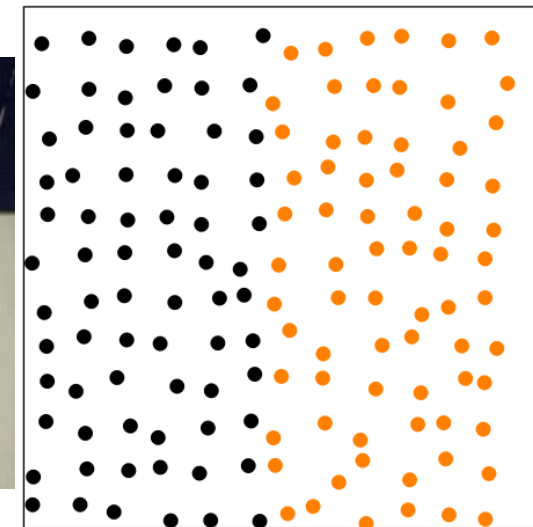
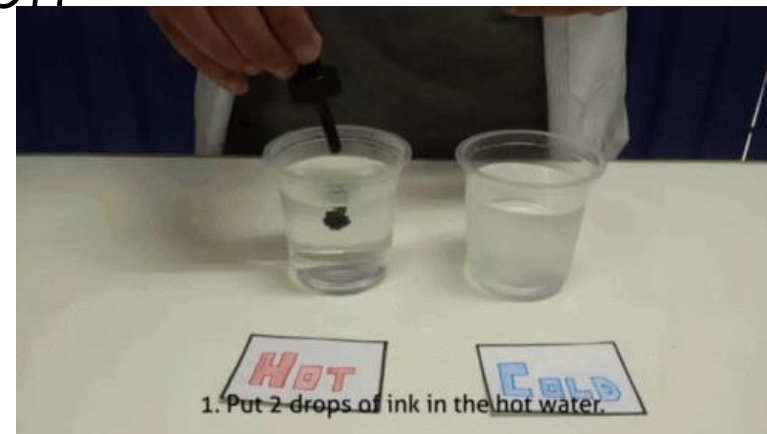
Drift Current

When an electrical field E is established in a semiconductor crystal, holes are accelerated in the direction of E , and free electrons are accelerated in the direction opposite to that of E .



Diffusion Current

At non-uniform charge distribution, the charges flow from high concentration to low concentration



Recombination

1. Some electrons may fill some of the holes.
2. Disappearance of free electrons and holes

Doped Semiconductors

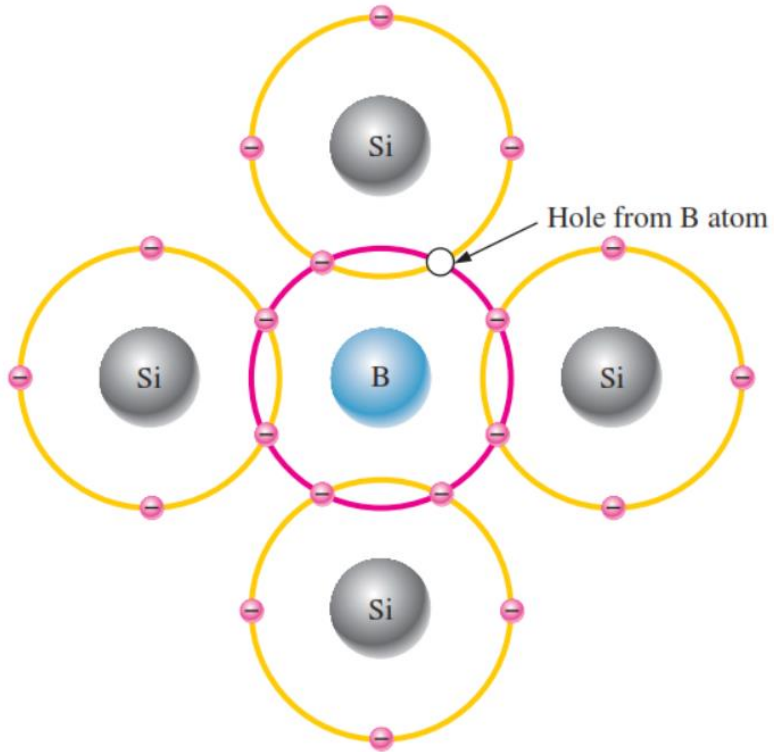


13	14	15
5 B Boron	6 C Carbon	7 N Nitrogen
13 Al Aluminium	14 Si Silicon	15 P Phosphorus
31 Ga Gallium	32 Ge Germanium	33 As Arsenic
49 In Indium	50 Sn Tin	51 Sb Antimony
81 Tl Thallium	82 Pb Lead	83 Bi Bismuth
113 Nh Nihonium	114 Fl Flerovium	115 Mc Moscovium

introducing impurity atoms into the silicon crystal in sufficient numbers to substantially increase the concentration of either free electrons or holes but with little change in the crystal properties of silicon.

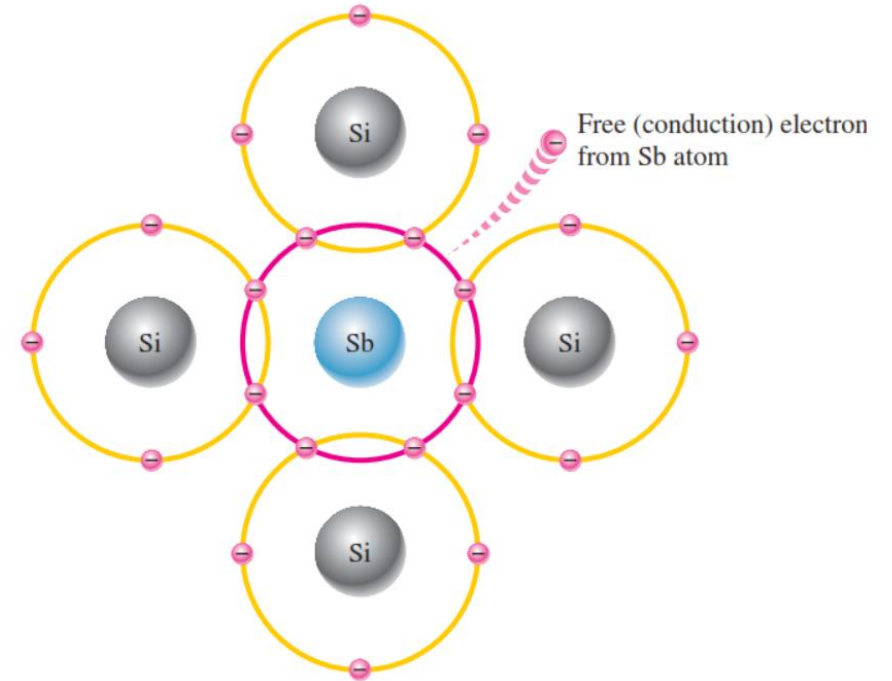
Doped Semiconductors

Sb impurity is called an **acceptor**.

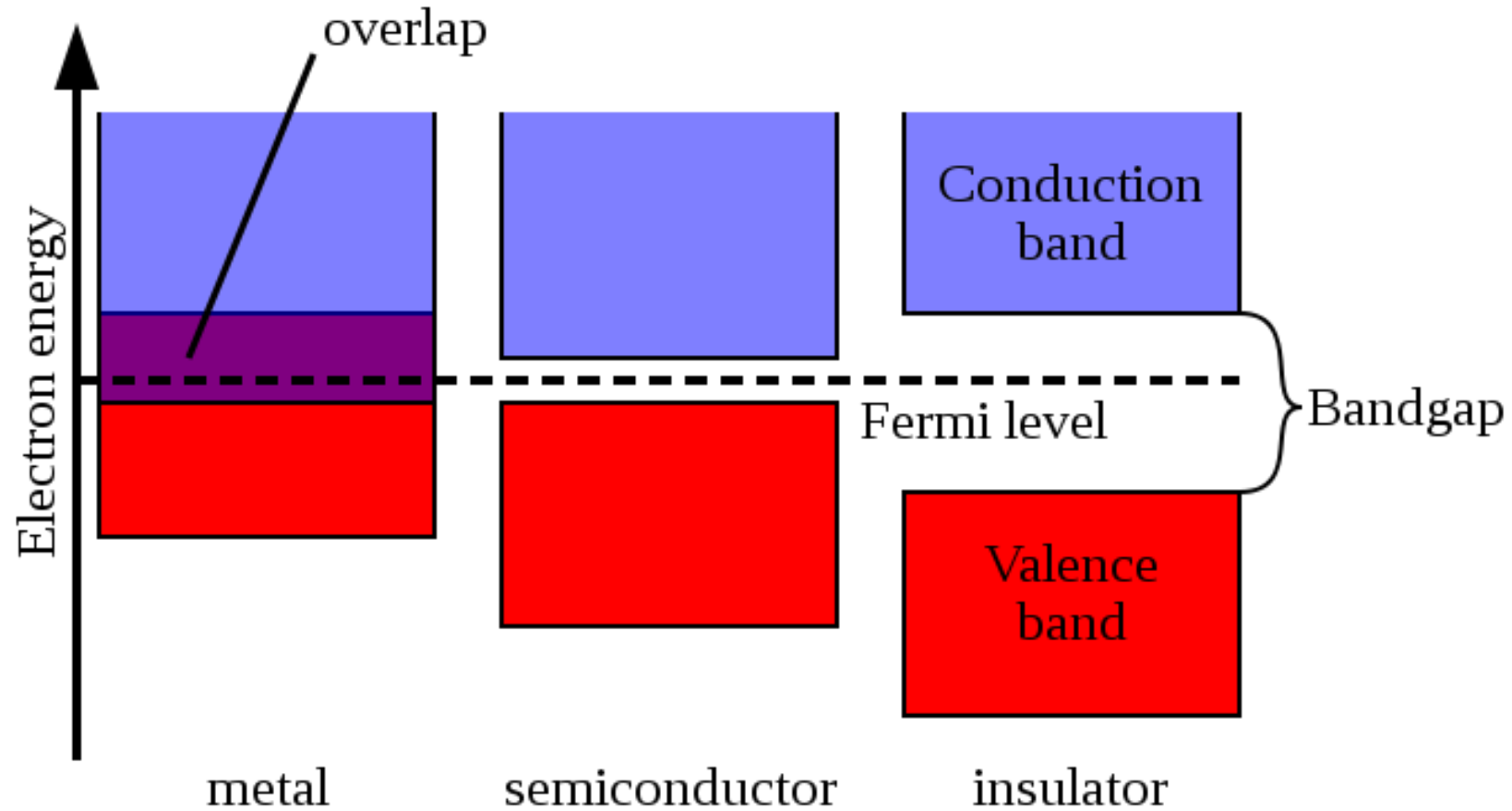


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49 In Indium	50 Sn Tin	51 Sb Antimony
81 Tl Thallium	82 Pb Lead	83 Bi Bismuth
113 Nh Nihonium	114 Fl Flerovium	115 Mc Moscovium

Sb impurity is called a **donor**.

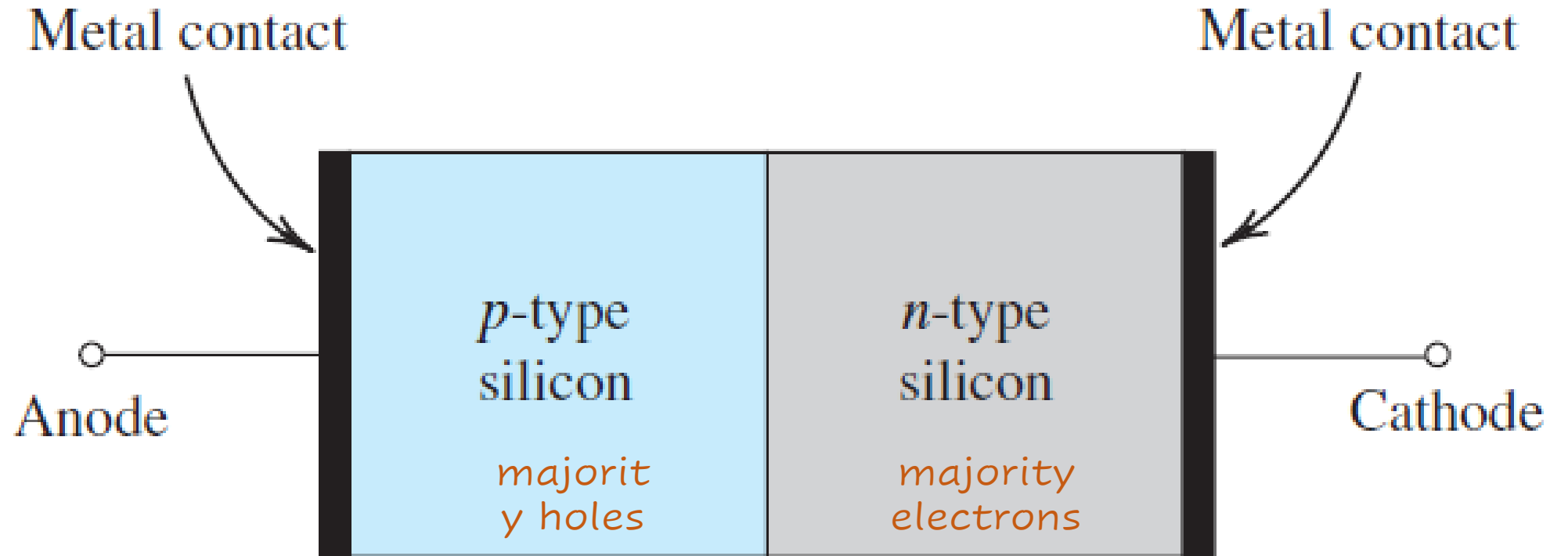


Band Diagrams

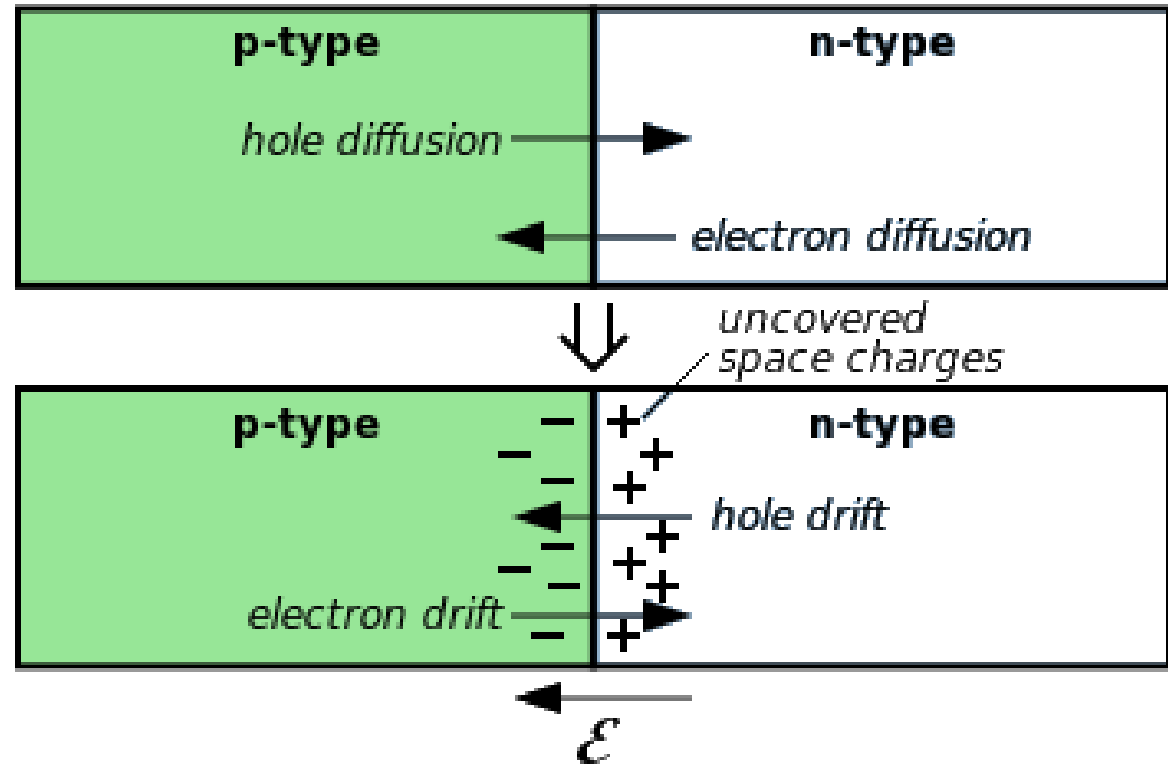


PN Junction

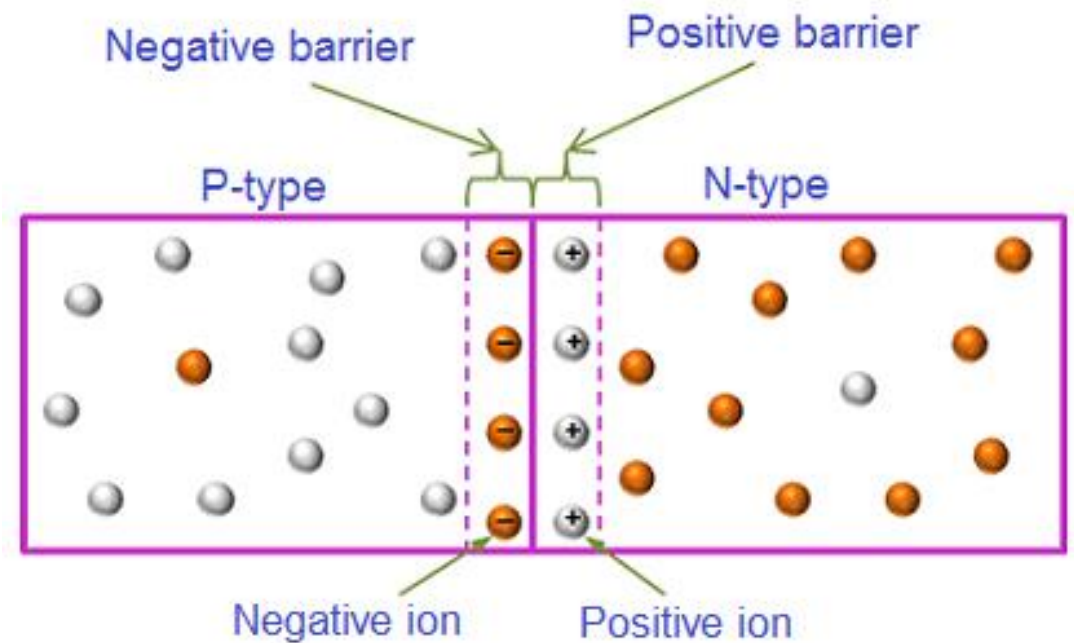
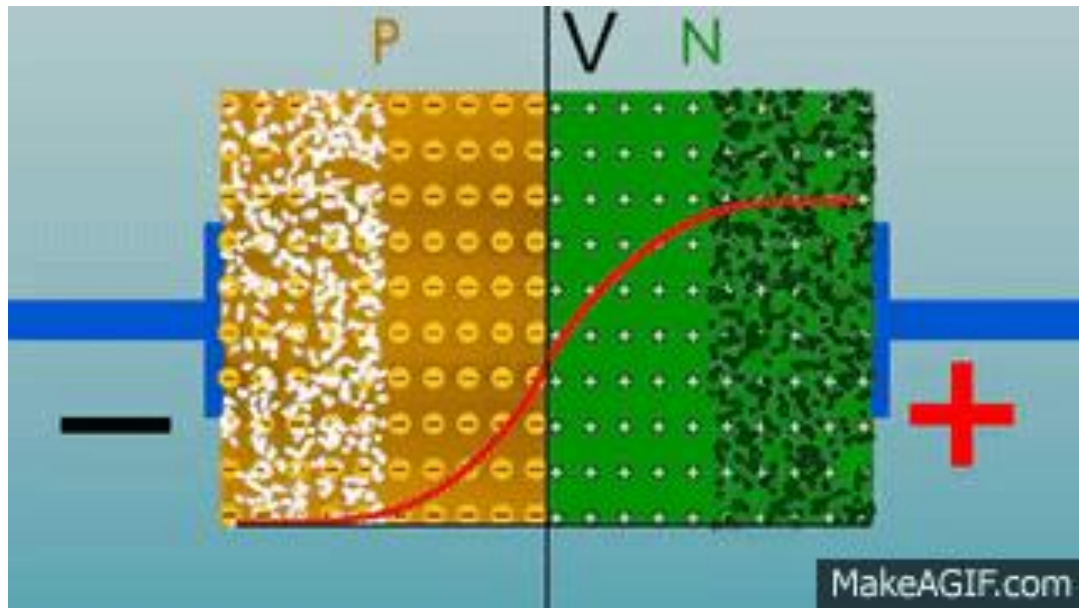
Physical Structure



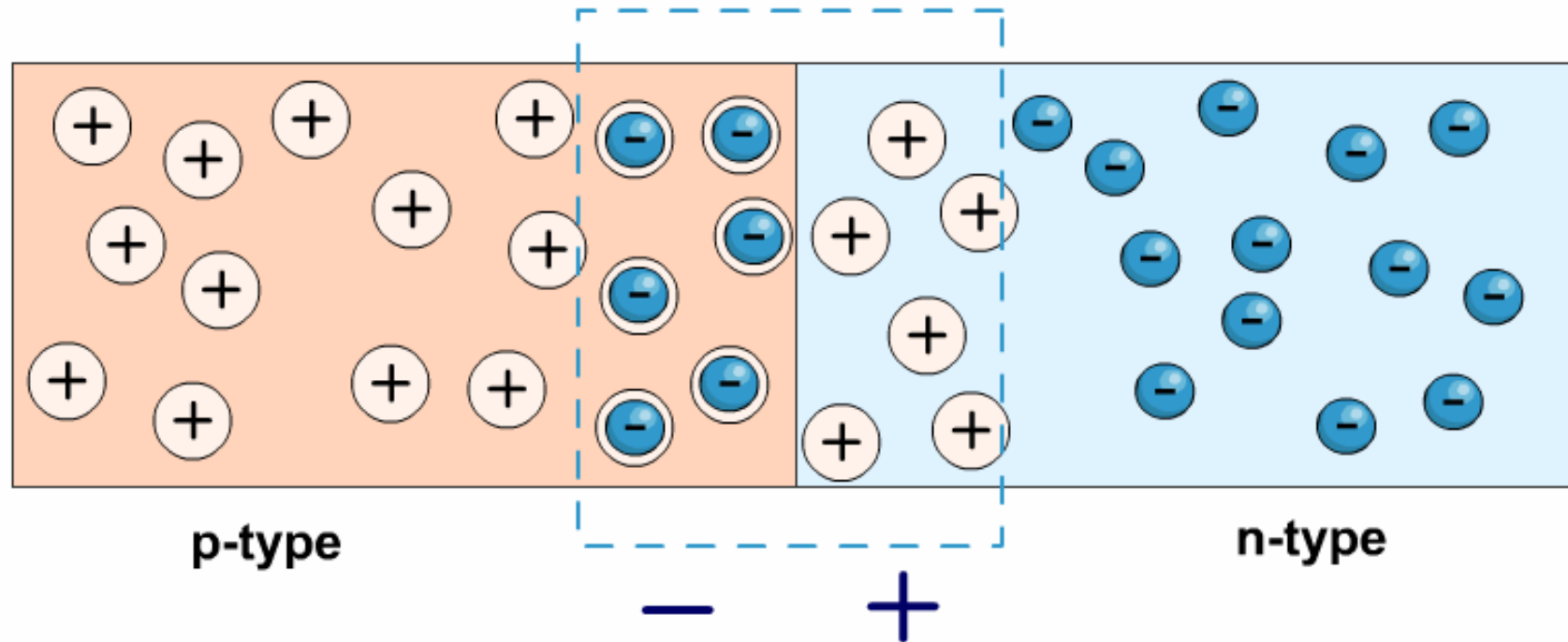
1. Diffusion current



2. Depletion Region

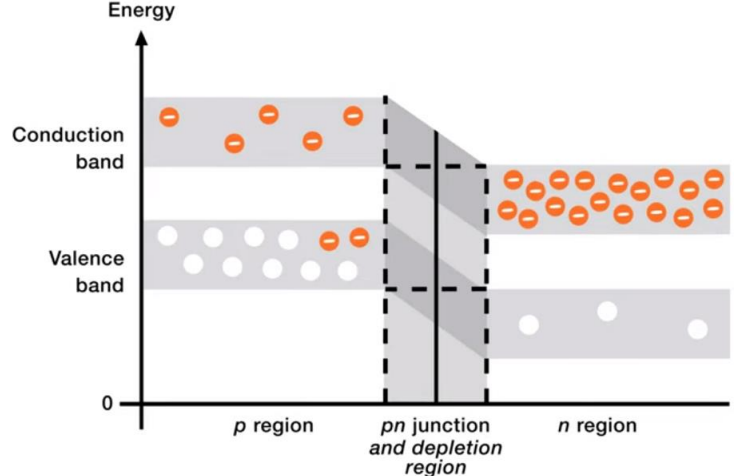
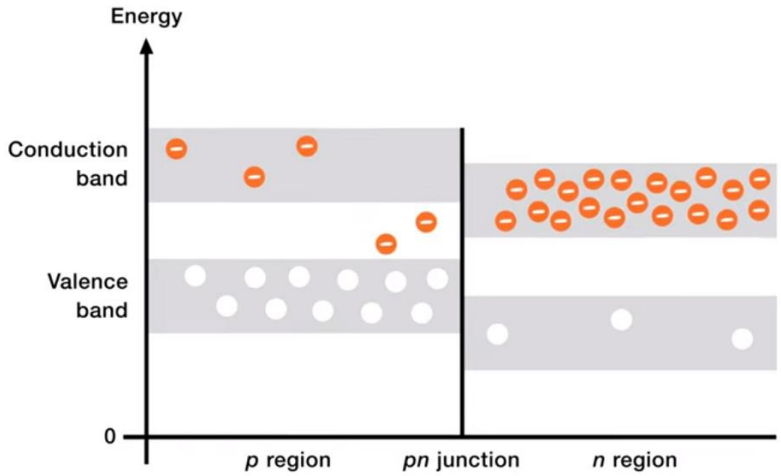
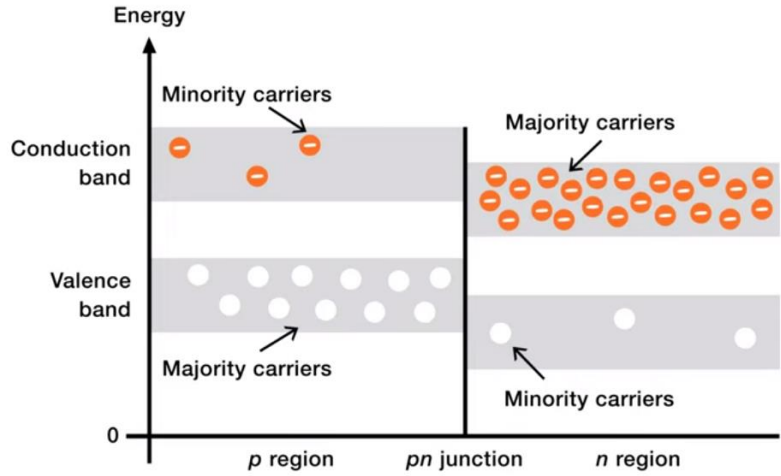
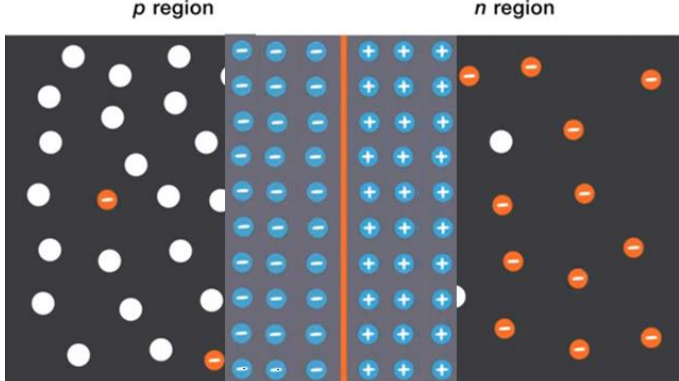
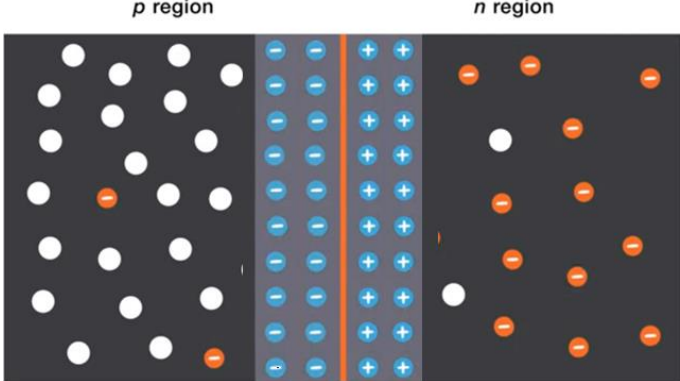
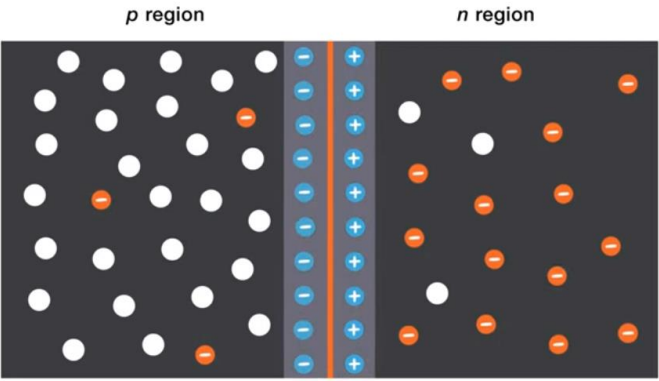


Summary

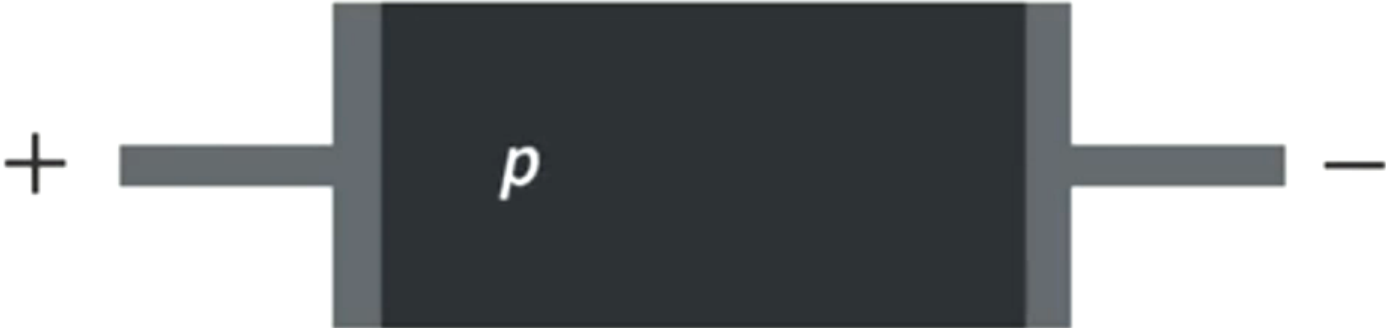


- Semiconductors n-type and p-type are brought together
- Electrons and holes migrate across the junction
- The depletion layer is formed
- A p.d. is set up across the depletion layer

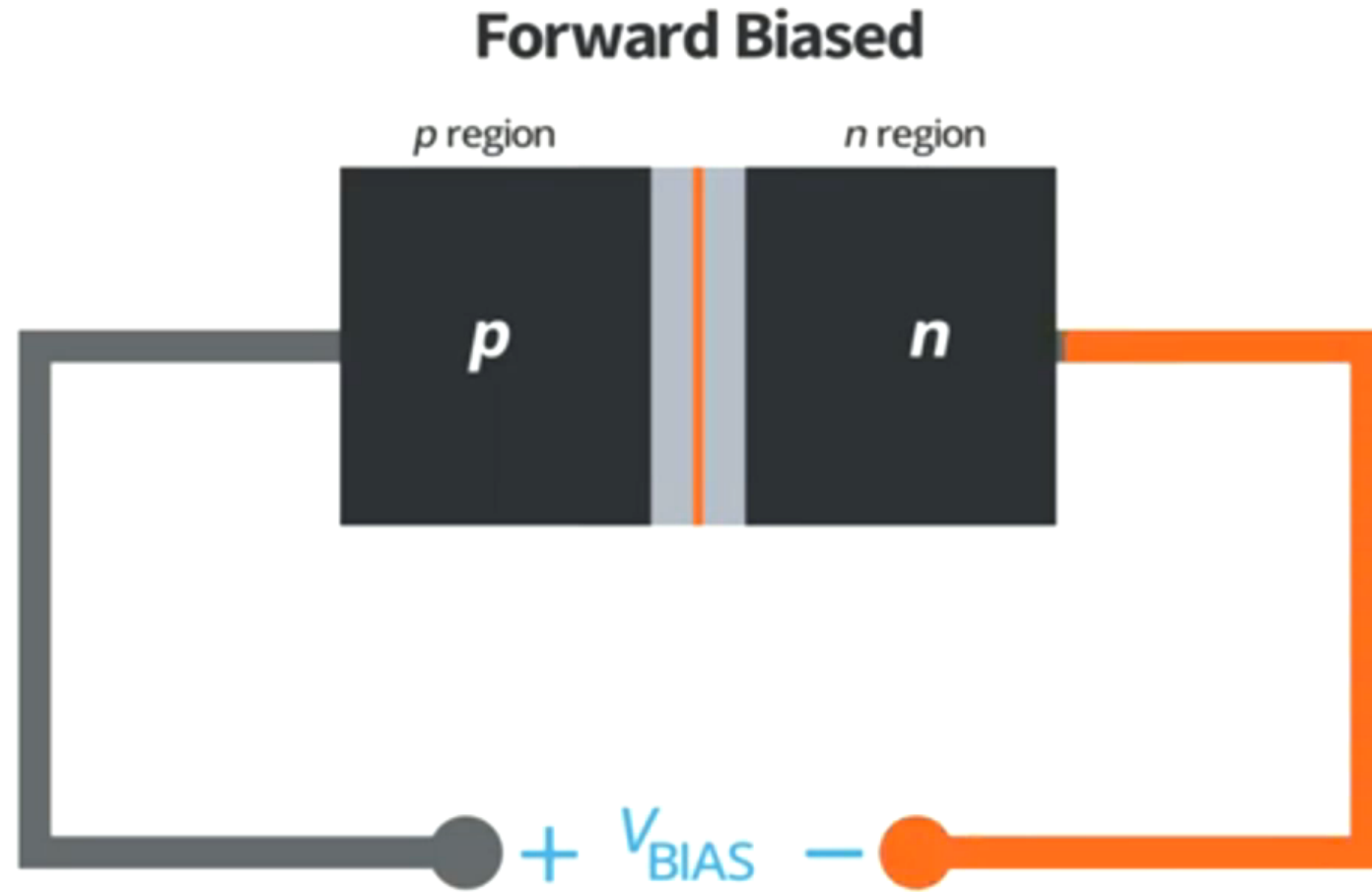
Unbiased PN Junction



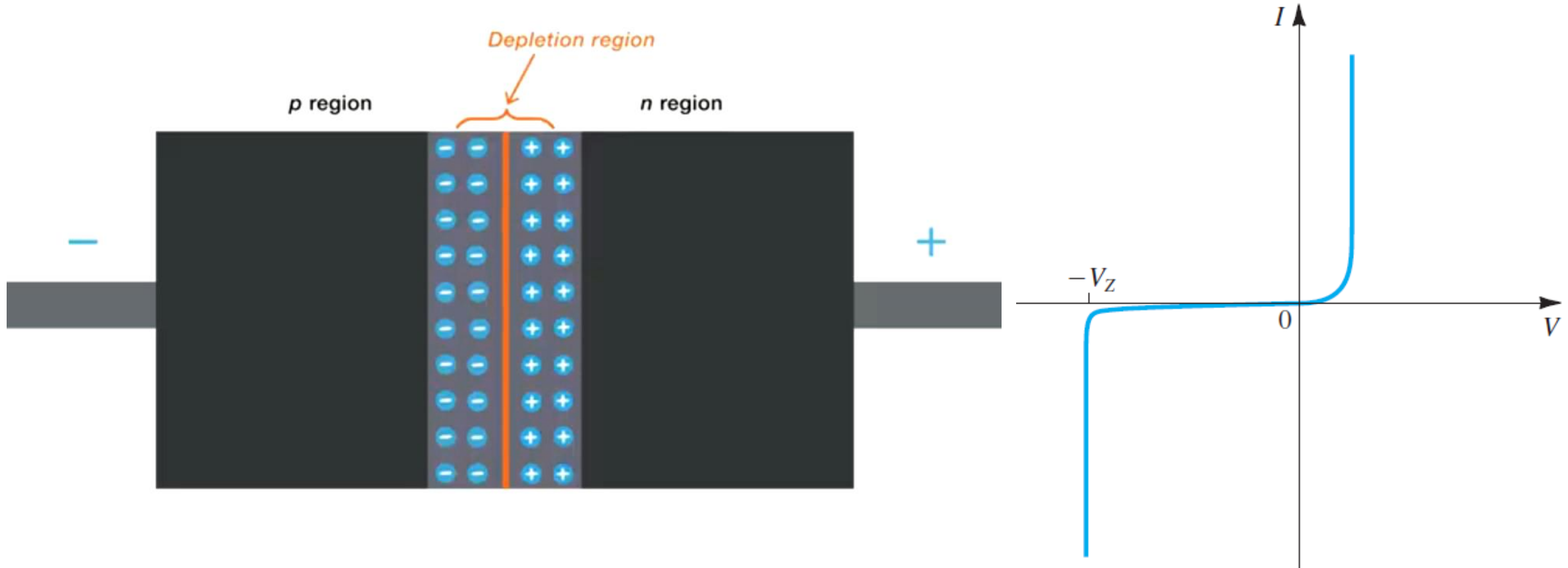
Biased PN Junction (forward bias)



Biased PN Junction (Reverse bias)

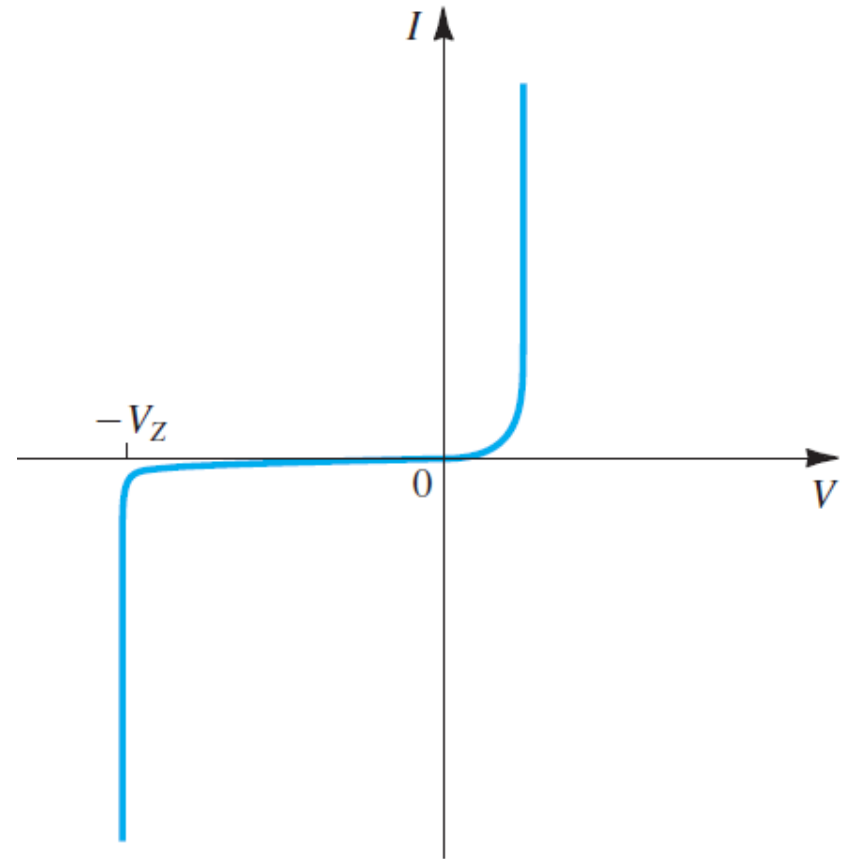


Biased PN Junction (Reverse bias)



Reverse Breakdown

The phenomenon that occurs at $V = V_Z$ is known as **junction breakdown**. It is not a destructive phenomenon. That is, the *pn* junction can be repeatedly operated in the breakdown region without a permanent effect on its characteristics.



End