Examiner: Dr. Mustafa M. Shiple

Subject: Advanced Microprocessor /(EEC 209)

Term: Feb - May 2016/2017

Score: 10 Marks Exam Time:30 min

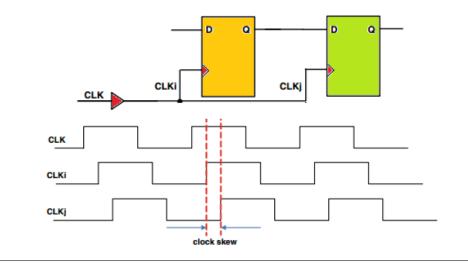
## ANSWER THE FOLLOWING QUESTIONS:

1. Briefly discuss the clock skew?

[3 marks ]  $[A_q, A_u, B_k]$ 

**Solution:** Q1. **Clock skew** is a phenomenon in synchronous circuits in which the clock signal arrives at different components at different times. Due to:

- Wire-interconnect length
- Temperature variations
- Capacitive coupling
- Material imperfections and differences in input capacitance on the clock inputs



2. Evaluate next equation  $Y = ABC + B(\bar{C} + \bar{A})$  against glitches.

[3 marks ]  $\left[B_a,A_d,A_q\right]$ 

Solution:		
buges	A,C	
ABC	at input A	Hazard
A00	0	No
A01	0	No
A10	1	No
A11	$A + \bar{A}$	Static 1
	at input C	
00C	0	No
01C	1	No
10C	0	No
11C	$C + \bar{C}$	Static 1

[Total Marks is 10]

Signature of Examiner:

The hazards are shown in the next figure

3. Redesign the previous equation to avoid glitches if existed.

[4 marks]  $[C_o, A_m]$ 

Solution: 
$$(A)$$

to avoid glitches Y = B