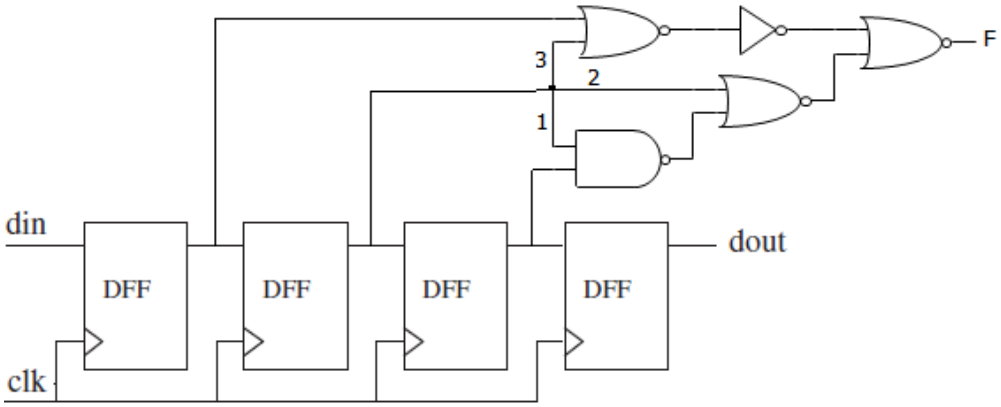
*Higher Technological Institute/ 10^{th} of Ramadan City
Department of Electrical & Computers Engineering
Quiz (2)

Examiner : Dr. Mustafa M. Shiple
Subject: Advanced Microprocessor /(EEC 209)
Score: 10 Marks

Term: Feb / May 2017
Exam Time:60 min

ANSWER THE FOLLOWING QUESTIONS:

1. Consider the next Figure. [5 marks] $[B_a, A_d, A_q]$



(a) Write a VHDL code that realizes the previous circuit.

Solution:

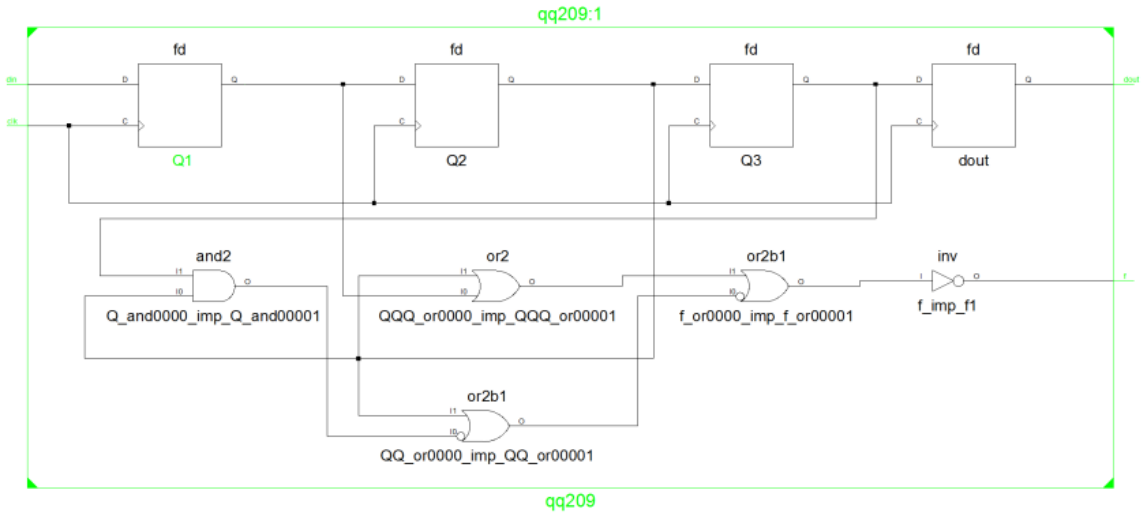
```
entity qq209 is
  Port ( din : in  STD_LOGIC;
       clk : in  STD_LOGIC;
       f : out  STD_LOGIC;
       dout : out  STD_LOGIC);
end qq209;

architecture Behavioral of qq209 is
signal Q1,Q2,Q3,Q,QQ,QQQ : std_logic;
begin

  DFF1: process (clk , din)
  Begin
    if rising_edge(clk)then
      Q1 <= din;
    end if;
  end process;

  DFF2: process (clk , din)
  Begin
    if rising_edge(clk)then
      Q2 <= Q1;
    end if;
  end process;

  DFF3: process (clk , din)
```

[Total Marks is 10]

Signature of Examiner:

Good Luck
Head of Dept.:

```
  Begin
    if rising_edge(clk)then
      Q3 <= Q2;
    end if;
  end process;

  DFF4: process (clk , din)
  Begin
    if rising_edge(clk)then
      dout<= Q3;
    end if;
  end process;

  Q<=(Q2 nand Q3);
  QQ<=(Q2  nor Q);
  QQQ<=not(Q1 nor Q2);
  F<= (QQQ)nor QQ;
end Behavioral;
```



2. Consider the next VHDL code: [5 marks] $[C_o, A_m]$

   (a) Synthesize the next code, and Draw the circuit.

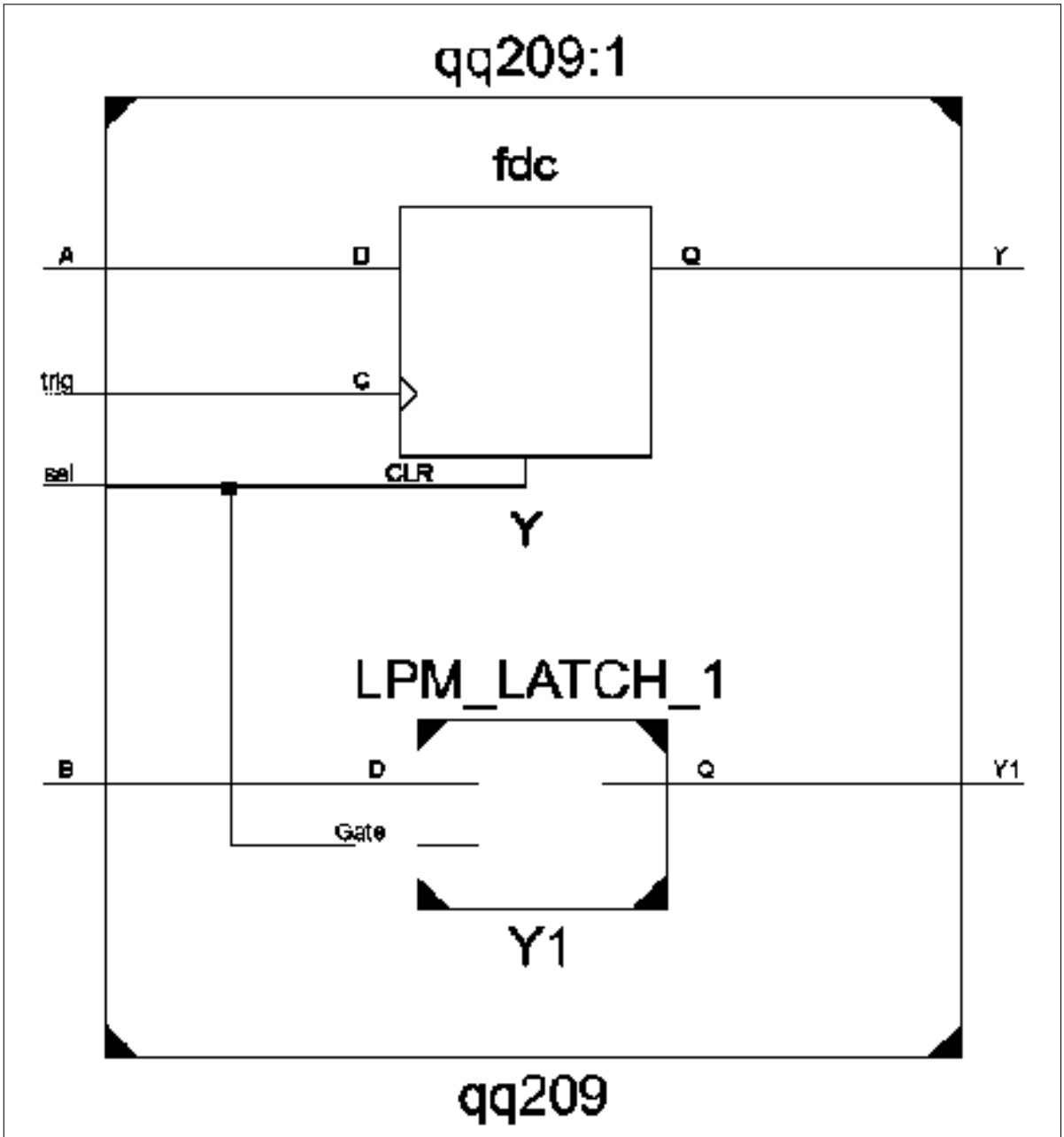
   (b) Compile the next code, and complete the missing data.

```


architecture ......... of QQ209 is

begin
Process1:   process (sel,    ,    )
```

```
7  begin
8    if sel = '1' then
9      Y<='0';
10   elsif rising_edge(trig) then
11     Y <= A;
12   end if;
13 end process;
14
15 Process2: process (sel, B)
16 begin
17   if sel = '1' then
18     Y <= B;
19   end if;
20 end process
21
22 end Behavioral;
```

Solution:

- Process 1 : symptoms and tokens describe DFF :
  - "Asynchronous reset" is named "sel".
  - The "clock" is named "trig" and activating by rising edge.
  - input = A
  - output = Y
- Process 2 : symptoms and tokens describe latch :
  - incomplete "if" statement .
  - The "latch" is named "sel" and activating by high level.
  - input = B
  - output = Y
- The output of two processes is identical (multiple driver). Consequently, it must one of them be changed.




```
1
2  entity qq209 is
3    Port ( trig,sel,A,B : in  STD_LOGIC;
4         Y,Y1 : out  STD_LOGIC);
5  end qq209;
6
7  architecture Behavioral of qq209 is
8  begin
9
```

```
  Process1: process (trig , sel, A)
  Begin
    if sel='1' then
      Y<='0';
    elsif rising_edge(trig)then
      Y<=A;
    end if;
  end process;

  process2: process (sel , B)
  Begin
    if sel='1' then
      Y1<=B;
    end if;
  end process;

end Behavioral;
```