



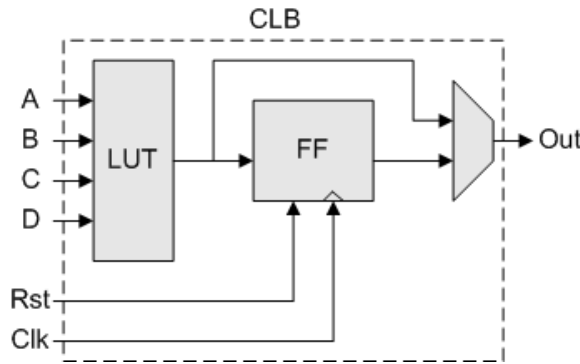
Examiner : Dr. Mustafa M. Shiple
 Subject: Shaping Circuits /(EEC 209)
 Score: 30 Marks

Term: Feb - May 2017
 Exam Time:60 min

ANSWER THE FOLLOWING QUESTIONS:

1. Briefly discuss the following items [10 marks] [A_u, B_k]
- (a) FPGA Architecture and sub-blocks
 - (b) 6T Cell SRAM.
 - (c) Metastability, Setup Time, Hold Time.

Solution:



(a) PSM: Programmable Switch Matrices, responsible for connecting the different CLBs. CLB: Configurable Logic Block , responsible for accommodating the logic circuits that are required either asynchronously or asynchronously. IO Block: input/output blocks, responsible for dealing with i/o signals including timing issues and protection circuits

(b)



The structure of a 6 transistor SRAM cell, storing one bit of information, can be seen in Figure.

The access transistors and the word and bit lines, WL and BL, are used to read and write from or to the cell.

To write information the data is imposed on the bit line and the inverse data on the inverse bit line, \overline{BL} . Then the access transistors are turned on by setting the word line to high.

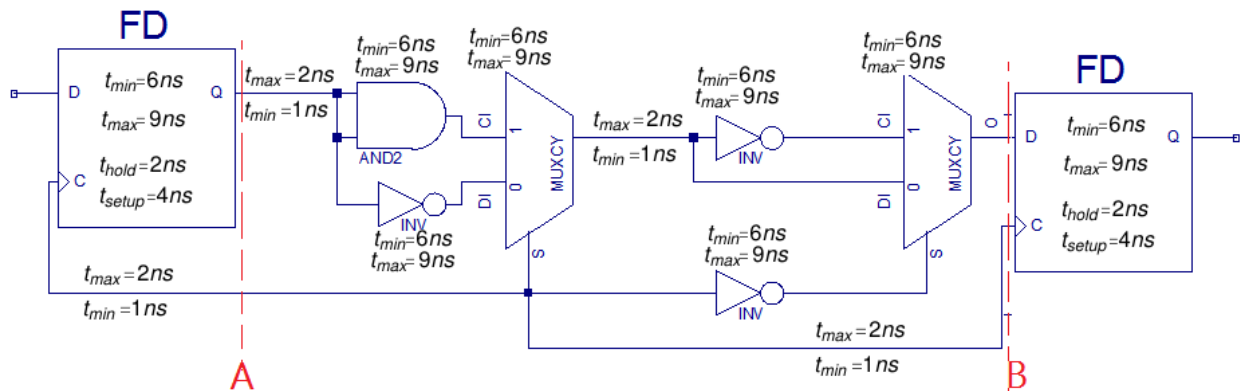
[Total Marks is 30]

For reading the word line is turned on to activate the access transistors while the information is sensed at the bit lines.

(c) Metastability: Result of violation of setup and hold times of a flip flop. Setup Time: The time required for data input to remain stable prior to arrival of clock pulse. Hold Time: The time required for data input to remain stable after the arrival of clock pulse.

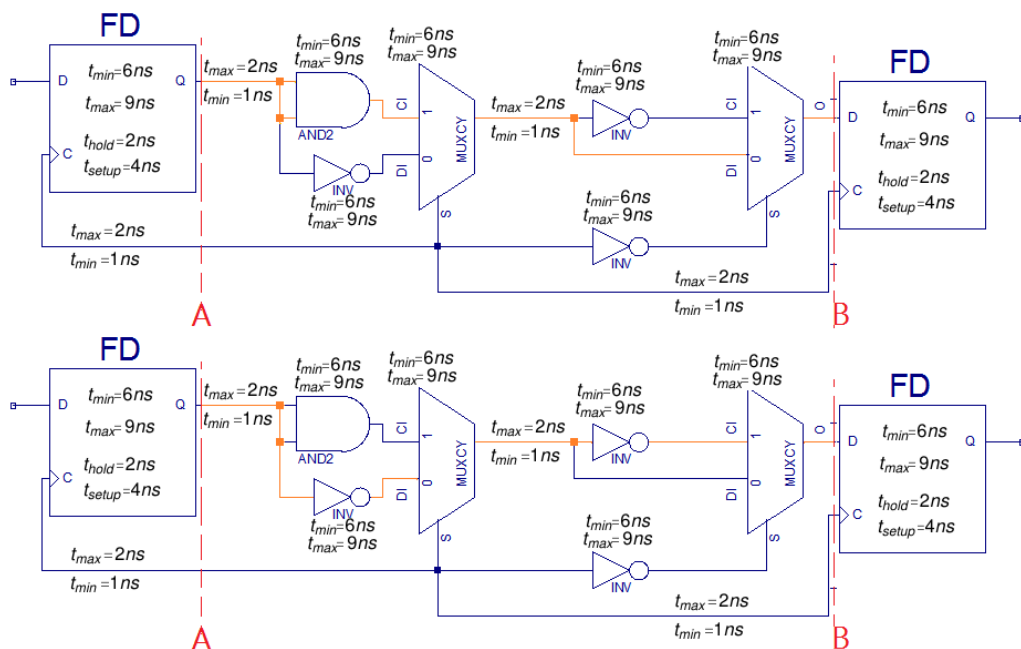
2. Calculate setup/hold violations

[6 marks] [C_o, A_m]



Solution:

(a)



There are two cases: 1) when S='1', 2)when S='0'.

- Case S='1':

$$Data_Path(max) = FD_{max} + path_{max} + AND_{max} + mux_{max} + path_{max} + mux_{max} + FD_{setup}$$

$$Data_Path(max) = 9 + 2 + 9 + 9 + 2 + 9 + 4 = 44ns$$

$$clk_Path(min) = path_{min} + path_{min} + clk_period$$

$$clk_Path(min) = 1 + 1 + 15 = 17ns$$

$\therefore clk_Path < Data_Path$ by 27 (setup violation)

$$Data_Path(min) = FD_{min} + path_{min} + AND_{min} + mux_{min} + path_{min} + mux_{min}$$

$$Data_Path(min) = 6 + 1 + 6 + 6 + 1 + 6 = 26ns$$

$$clk_Path(max) = path_{max} + path_{max} + FD_{hold}$$

$$clk_Path(max) = 2 + 2 + 2 = 6ns$$

$\therefore clk_Path < Data_Path$ by 20ns (no hold violation)

- Case S='0':

$$Data_Path(max) = FD_{max} + path_{max} + INV_{max} + mux_{max} + path_{max} + INV_{max} + mux_{max} + FD_{setup}$$

$$Data_Path(max) = 9 + 2 + 9 + 9 + 2 + 9 + 9 + 4 = 53ns$$

$$clk_Path(min) = path_{min} + path_{min} + clk_period$$

$$clk_Path(min) = 1 + 1 + 15 = 17ns$$

$\therefore clk_Path < Data_Path$ by 36ns (setup violation)

$$Data_Path(min) = FD_{min} + path_{min} + gate_{min} + mux_{min} + path_{min} + mux_{min}$$

$$Data_Path(min) = 6 + 1 + 6 + 6 + 1 + 6 + 6 = 32ns$$

$$clk_Path(max) = path_{max} + path_{max} + FD_{hold}$$

$$clk_Path(max) = 2 + 2 + 2 = 6ns$$

$\therefore clk_Path < Data_Path$ by 26 (no hold violation)

From the above analysis the maximum setup violation is 36ns and no hold violation. Therefore, the proposed solution is to add the violation time to clock period to be $15+36=51$ ns that means the maximum frequency will be reduced to be $\frac{1}{51n} = 19.6GHz$

3. Write a VHDL code that realizes the previous circuit which is bounded by dashed lines A,B.(Hint: make the width of S generic input) [10 marks] [B_k, C_o, A_m]

Solution:

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1 entity MT209 is
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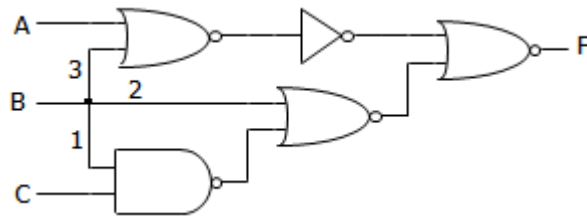
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2 Generic (width: integer :=0);
3 port( S:in std_logic_vector(width downto 0);
4       A:in std_logic;
5       B:out std_logic);
6 end MT209;
7
8 architecture Behavioral of MT209 is
9
10 begin
11
12     B <= not(A) when S="1" else (A and A) when S="0" else
13         (A and A) when S="1" else not(A);
14 end Behavioral;

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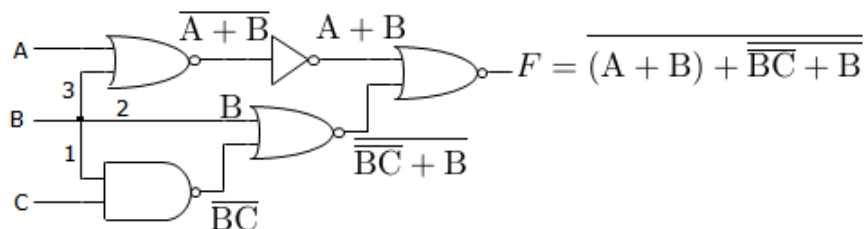
4. Evaluate the next circuit against glitches, resolve hazards if existed.

[4 marks] [A_d, A_q]



Solution: General rules :
 1- No for Distributive Law.
 2- OK for DeMorgan Law.

$$3-F = \overline{(A + B) + \overline{\overline{BC} + B}}$$



4-simplify without using Distributive Law. $F = \overline{B} \cdot \overline{A} \cdot (\overline{BC} + B)$

5-Dynamic @ $A = 0, C = 1 \Rightarrow \overline{B} \cdot (\overline{B} + B)$

6-The circuit could be resolved by synchronous systems.