

8085 Interrupts

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Microprocessor Architecture, 2019

بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

فِي الْحَقِّ وَالْبَاطِلِ
وَالْمَعْرُوفِ وَالْمَنْكُورِ
وَالْمُبِينِ

Introduction to interrupts

Definitions

- ① **At home** - how do you know when someone wants to talk to you on the telephone?
- A. Periodically pick up the phone and see if someone's there This is known as **polling**.
 - B. Wait for the phone to ring and then answer it, This is **interrupt-driven**

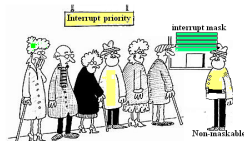
Interrupt

is a process where an external device can get the attention of the microprocessor.

- The process starts from the I/O device
- The process is asynchronous.

Neglecting ..

- Interrupts can sometimes be ignored (or masked)
 - ① Good for when the CPU is doing something more important
 - ② When the interrupt mask is set, interrupts are hidden (masked) and ignored
- Non-maskable interrupts cannot be ignored (NMI's take precedence)
- Interrupts may be prioritized



Servicing Interrupts and Exceptions

- When an exception occurs
 - CPU saves current state
 - PC, Flag Register
 - Global interrupts disabled
 - CPU saves current state
 - PC, Flag Register
 - Global interrupts disabled
 - Jump to interrupt service routine (ISR)
 - Execute routine
 - RETI - return from interrupt
 - Restore state
 - Flag Register (re-enables global interrupts)
 - Return to user program (restore PC)

Interrupt Vector Table (IVT)

Hardware interrupts of 8085

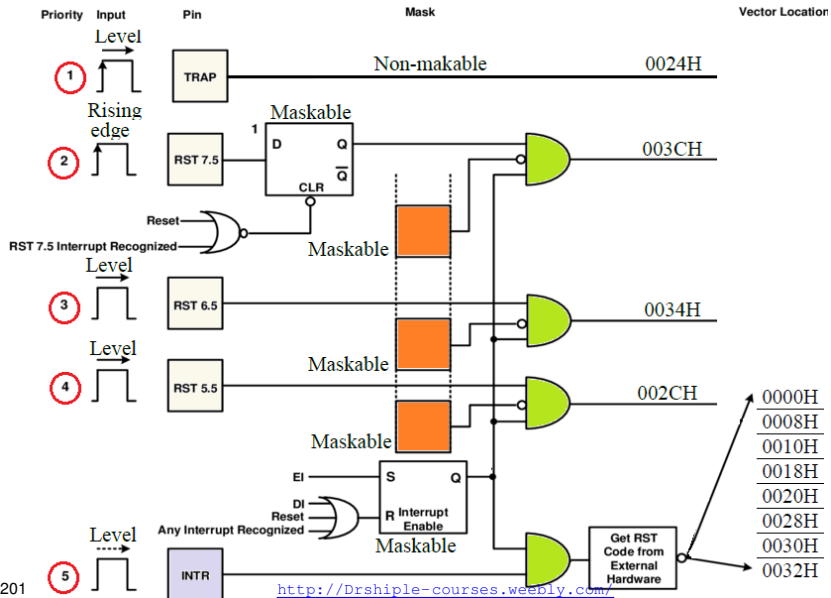
vector

Interrupt	Interrupt vector address	Maskable or non-maskable	Edge or level triggered	priority
TRAP	0024H	Non-maskable	Level	1
RST 7.5	003CH	Maskable	Rising edge	2
RST 6.5	0034H	Maskable	Level	3
RST 5.5	002CH	Maskable	Level	4
INTR	Decided by hardware	Maskable	Level	5

non-vector

Instruction	Machine hex code	Interrupt Vector Address
RST 0	C7	0000H
RST 1	CF	0008H
RST 2	D7	0010H
RST 3	DF	0018H
RST 4	E7	0020H
RST 5	EF	0028H
RST 6	F7	0030H
RST 7	FF	0032H

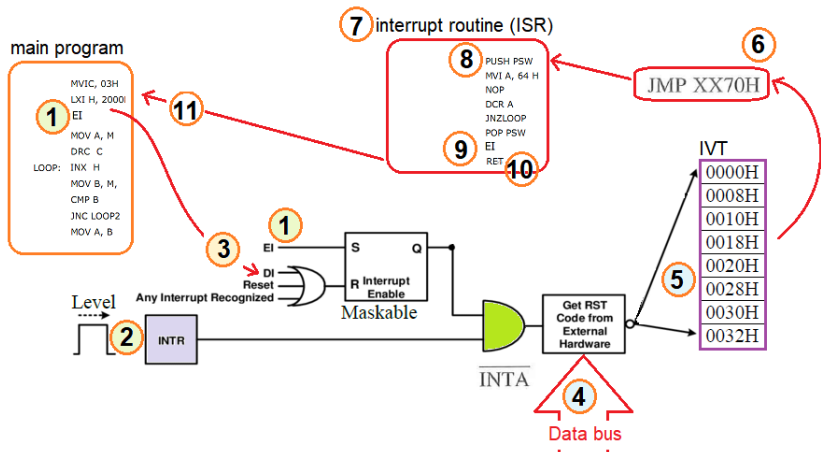
Interrupt summary



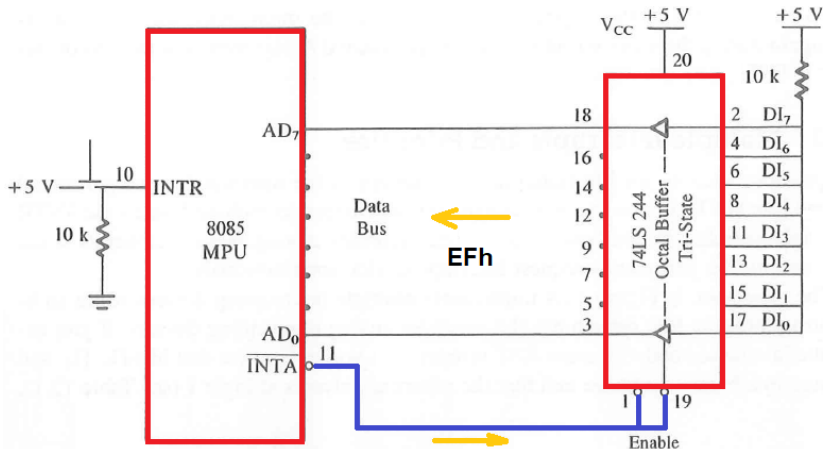
Interrupt assembly instructions

Instructions		Operation	Flag	Description
Mnemonics	Arguments			
SIM		mask=A	—	Set Interrupt Mask
RIM		A=mask	—	Read Interrupt Mas
DI			—	Disable Interrupts
EI			—	Enable Interrupts
RST	z	-[SP]=PC,PC=z	—	Restart (3X7)

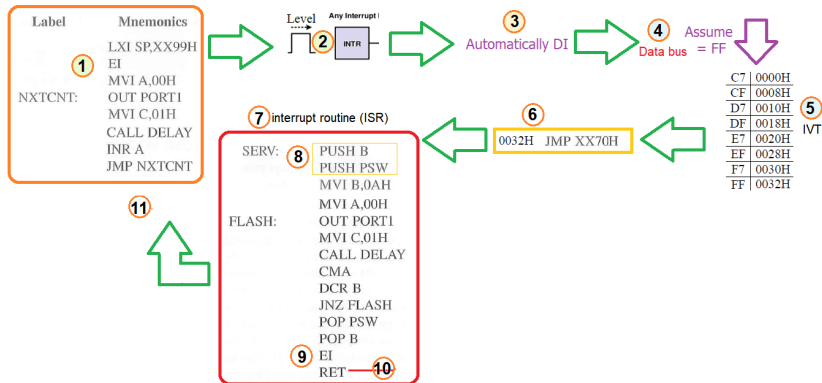
Interrupt life cycle



Interrupt life cycle



Interrupt life cycle



Classification of Interrupts

- Hardware (called Interrupts or Resets)
 - Reset
 - User-defined interrupt
 - Timer operations
 - CPU operations monitor failure
- Software
 - Reset
 - User-defined interrupt
 - Timer operations
 - CPU operations monitor failure