Memory Interface

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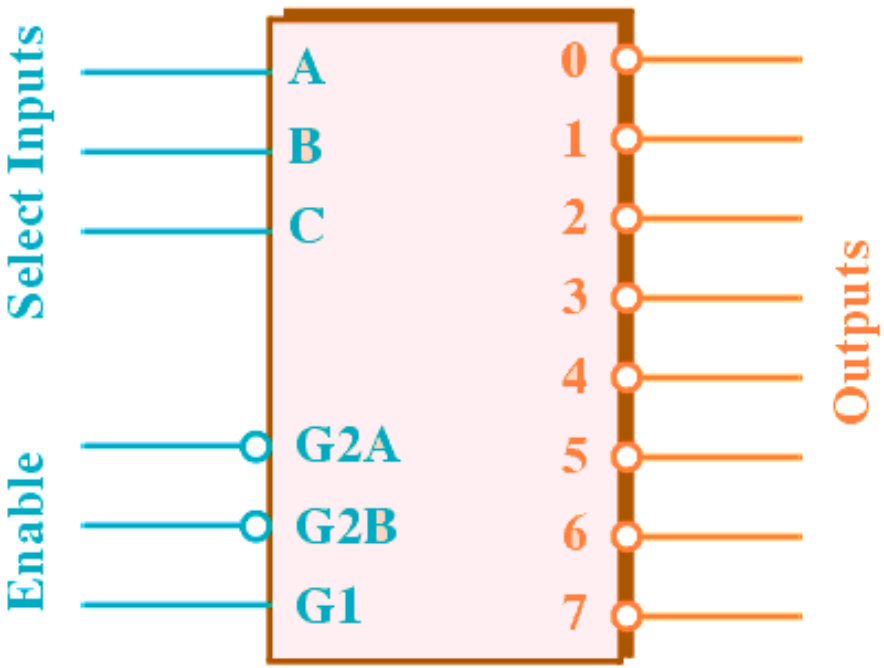
Microprocessor Architecture, 2019


بسم الله الرحمن الرحيم


وقل رب زدني علما

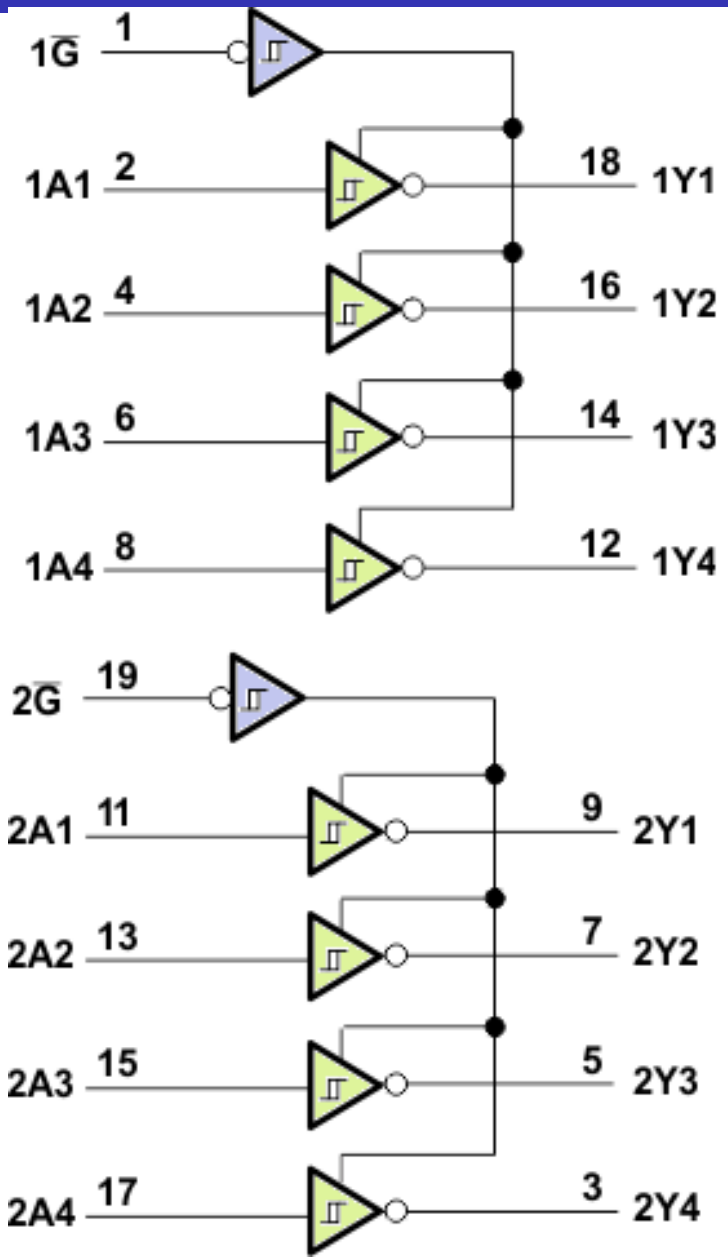
Introduction to decoders

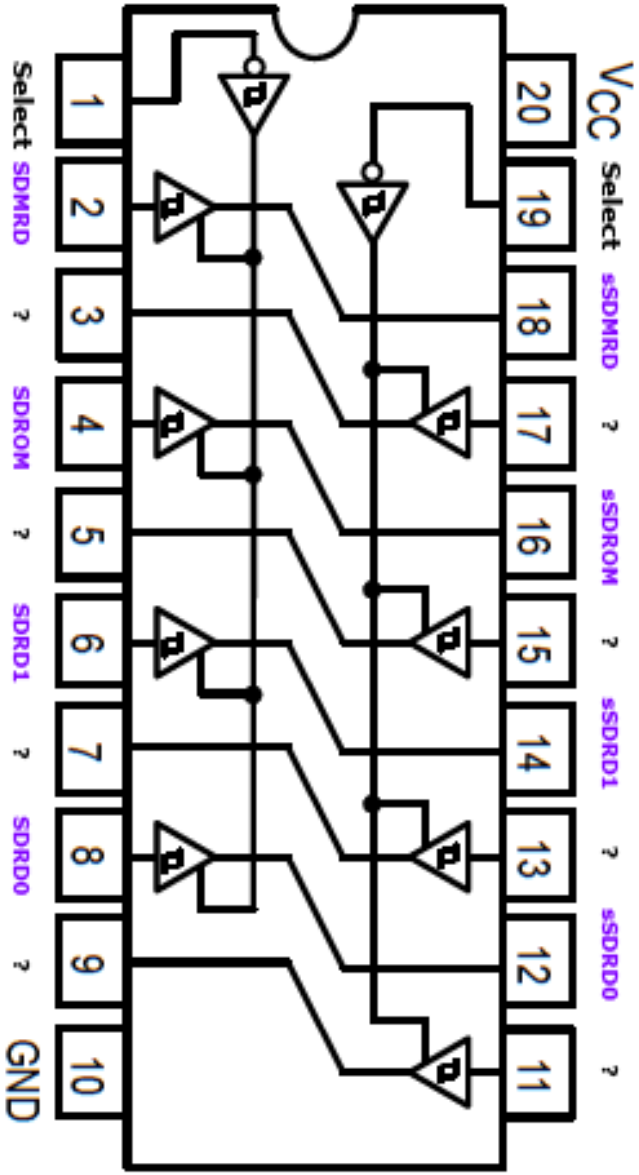
1-OF-8 Decoder/Demultiplexer (74ls138)



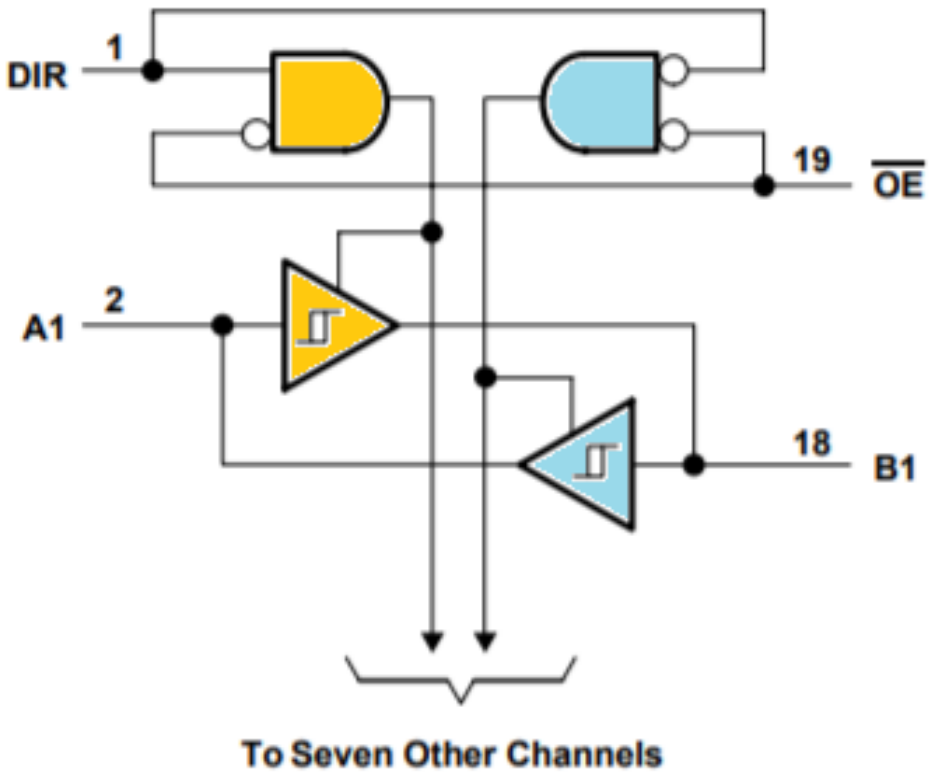
Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5		
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

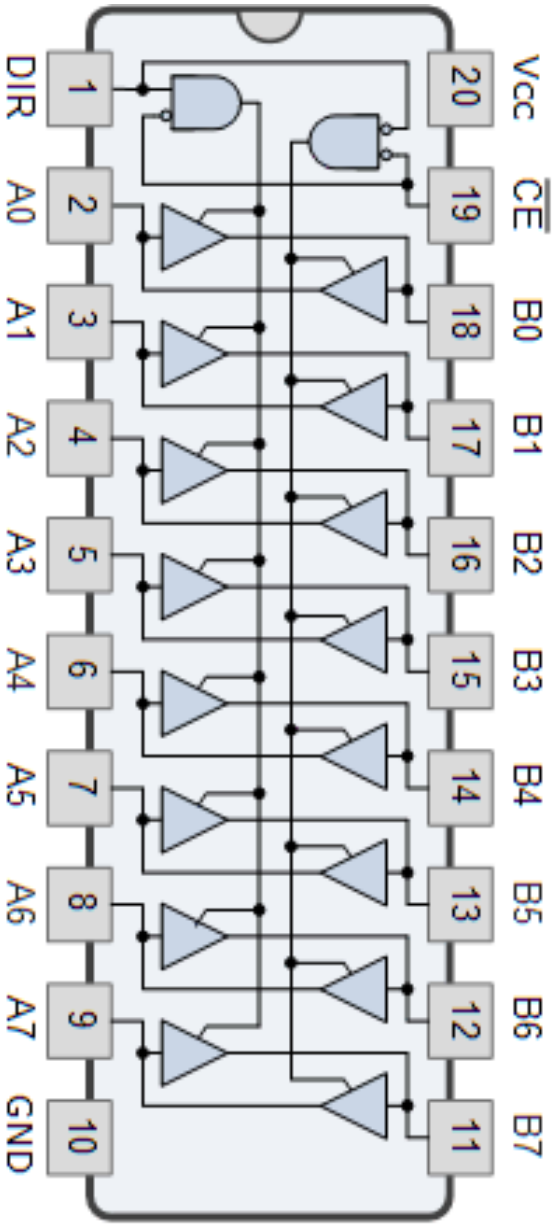
Octal 3-STATE Buffer/Line Driver/Line Receiver (74ls244)



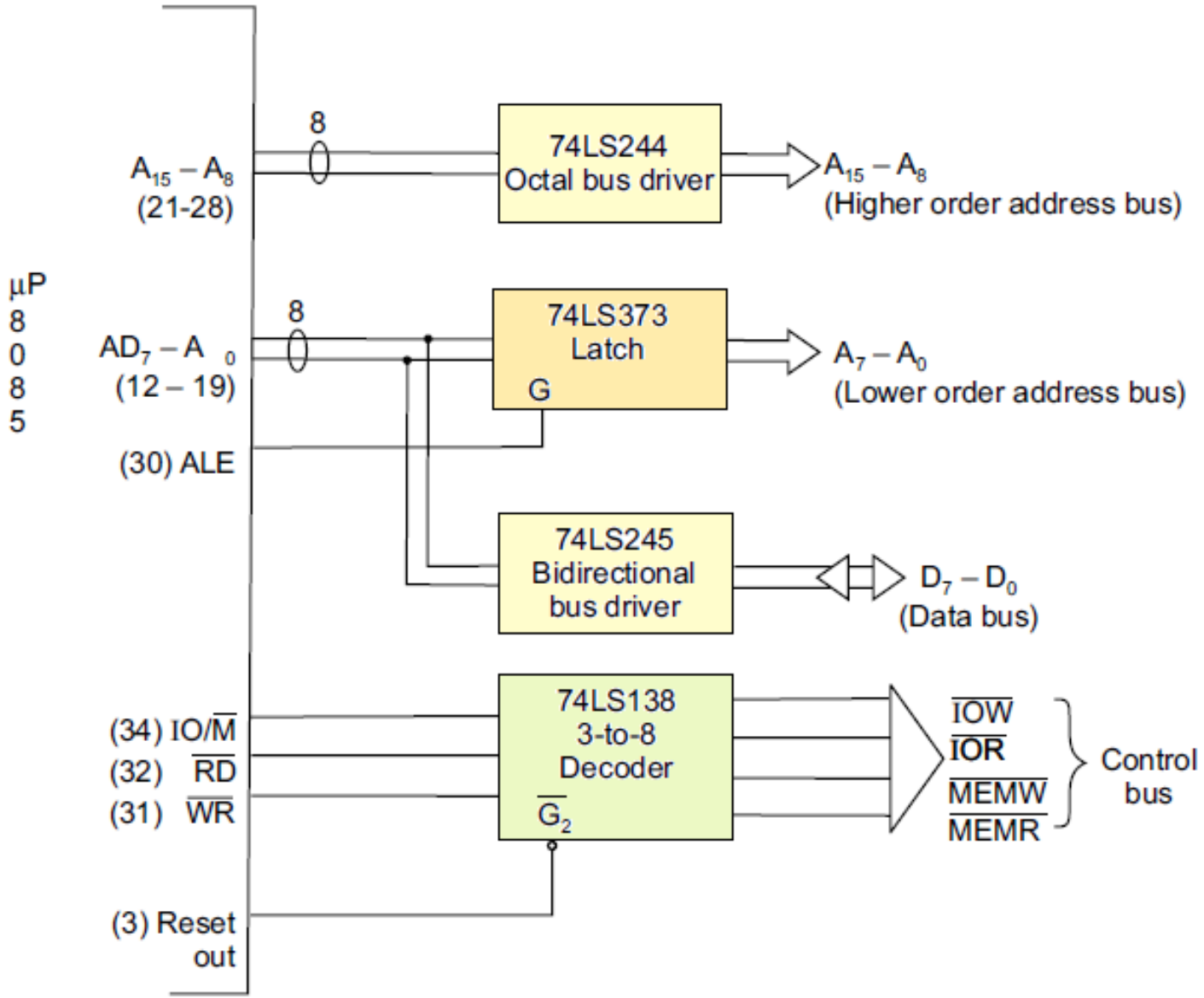


3-STATE Octal Bus Transceiver (74ls245)



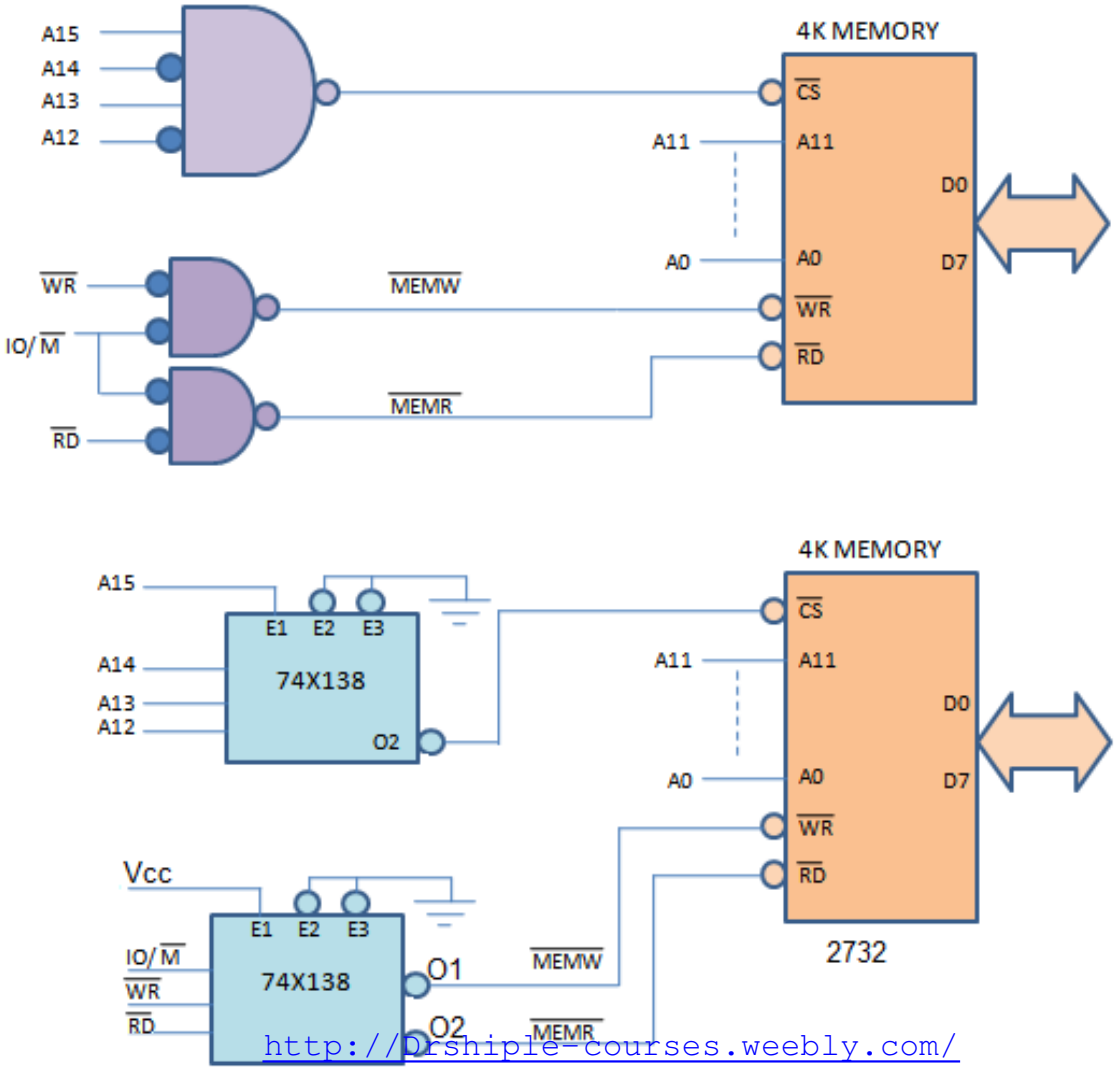


General 8085 Scheme



Memory interface

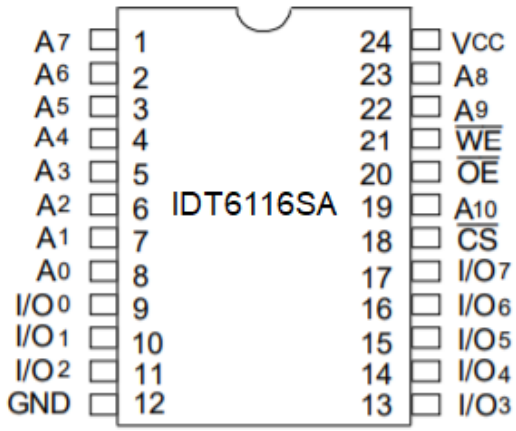
- 2K RAM : 11 address bus : A0 to A10
- 4K ROM : 12 address bus : A0 to A11



ROM/RAM Chips

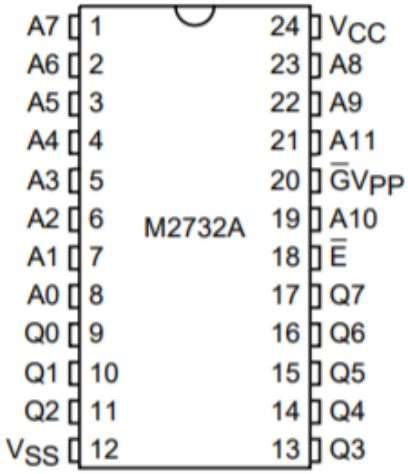
CMOS Static RAM (2K x 8-Bit)
NMOS 32K (4K x 8) UV EPROM

Pin Configurations



3089 drw 02

Pin Configurations



Pin Description

Name	Description
A_0 - A_{10}	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

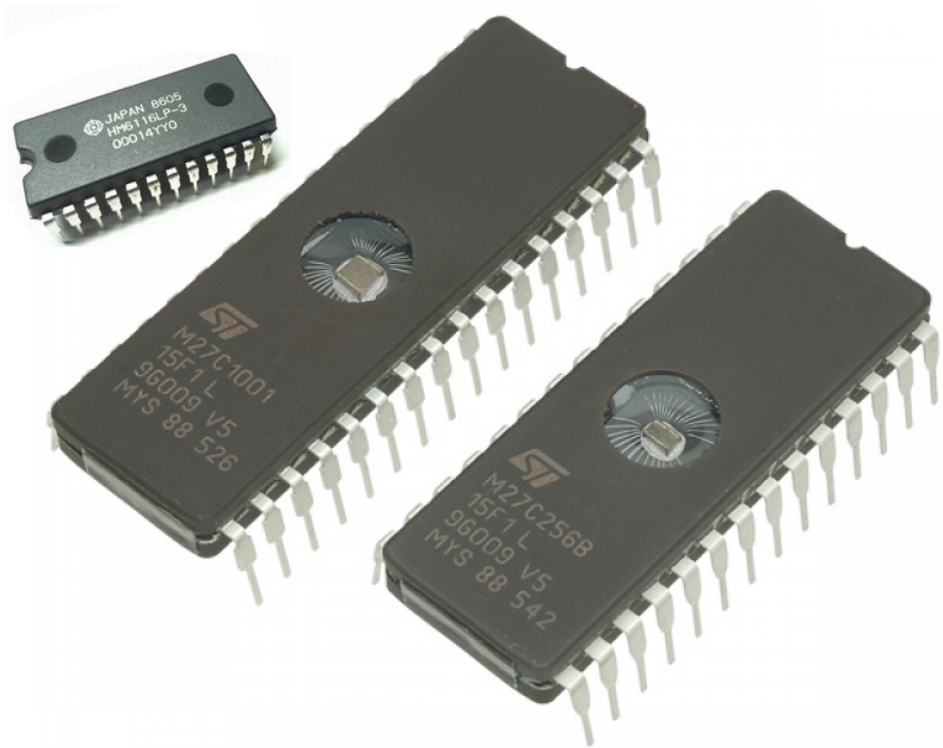
Pin Description

A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}V_{PP}$	Output Enable / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

ROM/RAM Chips

RAM Memory		
#	Chip No.	Size
1	2114	1k $\times$ 4bits
2	6116	2k $\times$ 8bits
3	6264	8k $\times$ 8bits

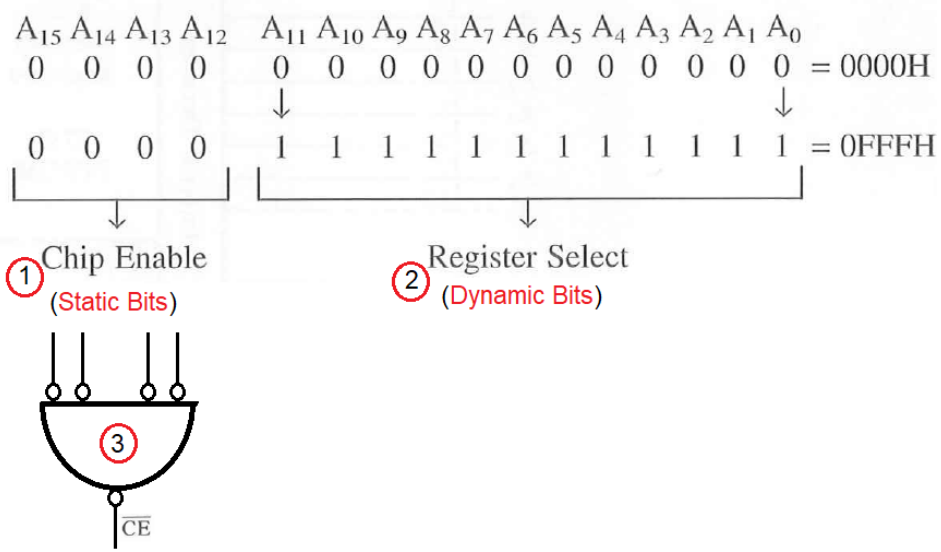
ROM Memory		
#	Chip No.	Size
1	2708	1k $\times$ 8bits
2	2716	2k $\times$ 8bits
3	2732	4k $\times$ 8bits
4	2764	8k $\times$ 8bits
5	27128	16k $\times$ 8bits
6	27256	32k $\times$ 8bits



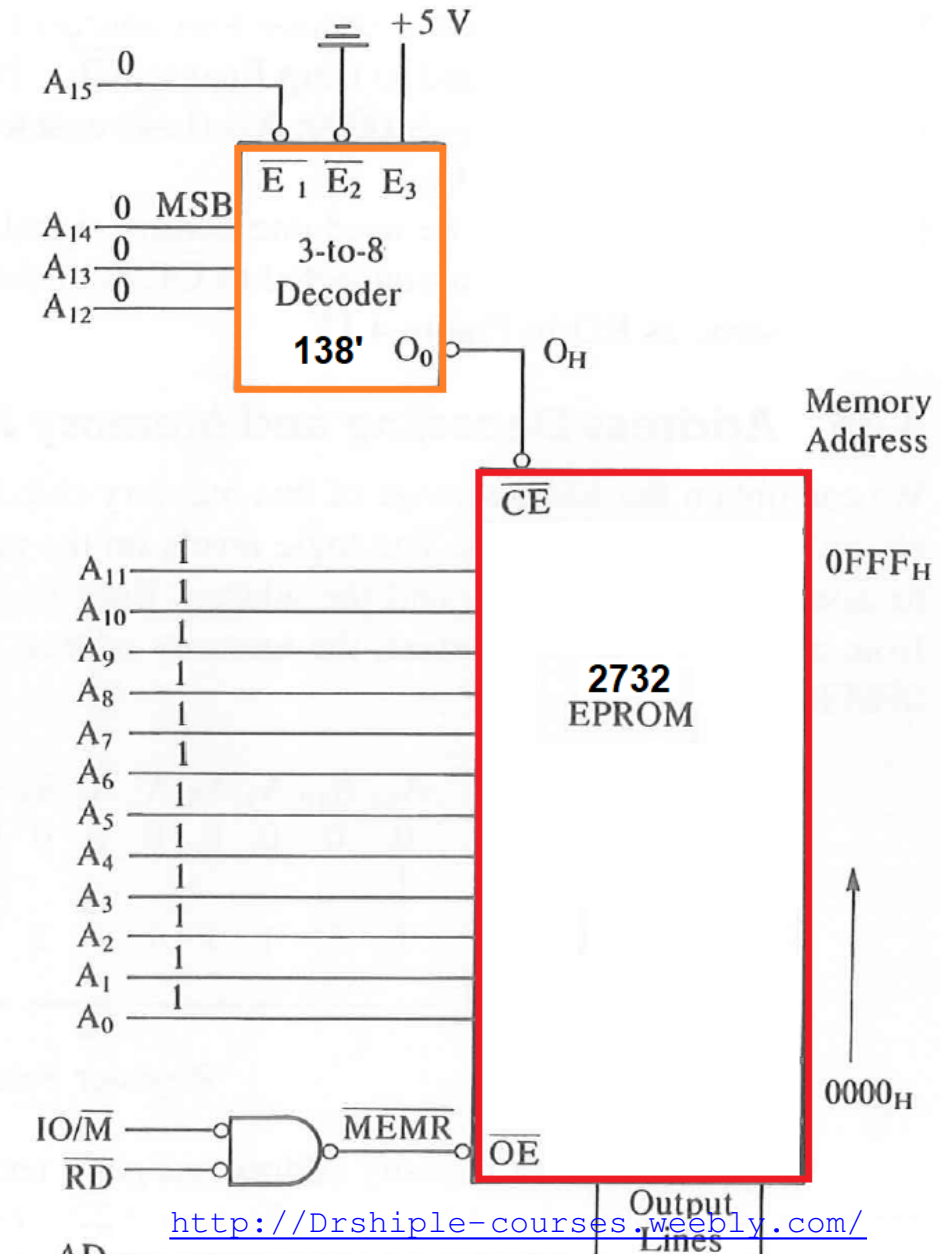
Exercise 1

Design the decoder circuit for ROM memory its address range is 0000 to FFFF?

1. Determine static bits Most significant 4 bits.
2. Determine dynamic bits:exclude.
3. Design according to static bits.



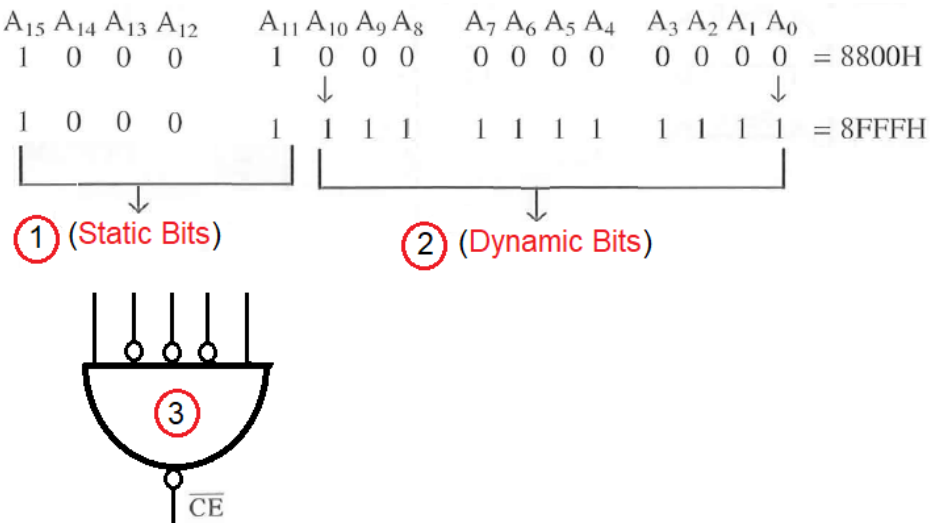
Exercise 1: 138 decoder solution



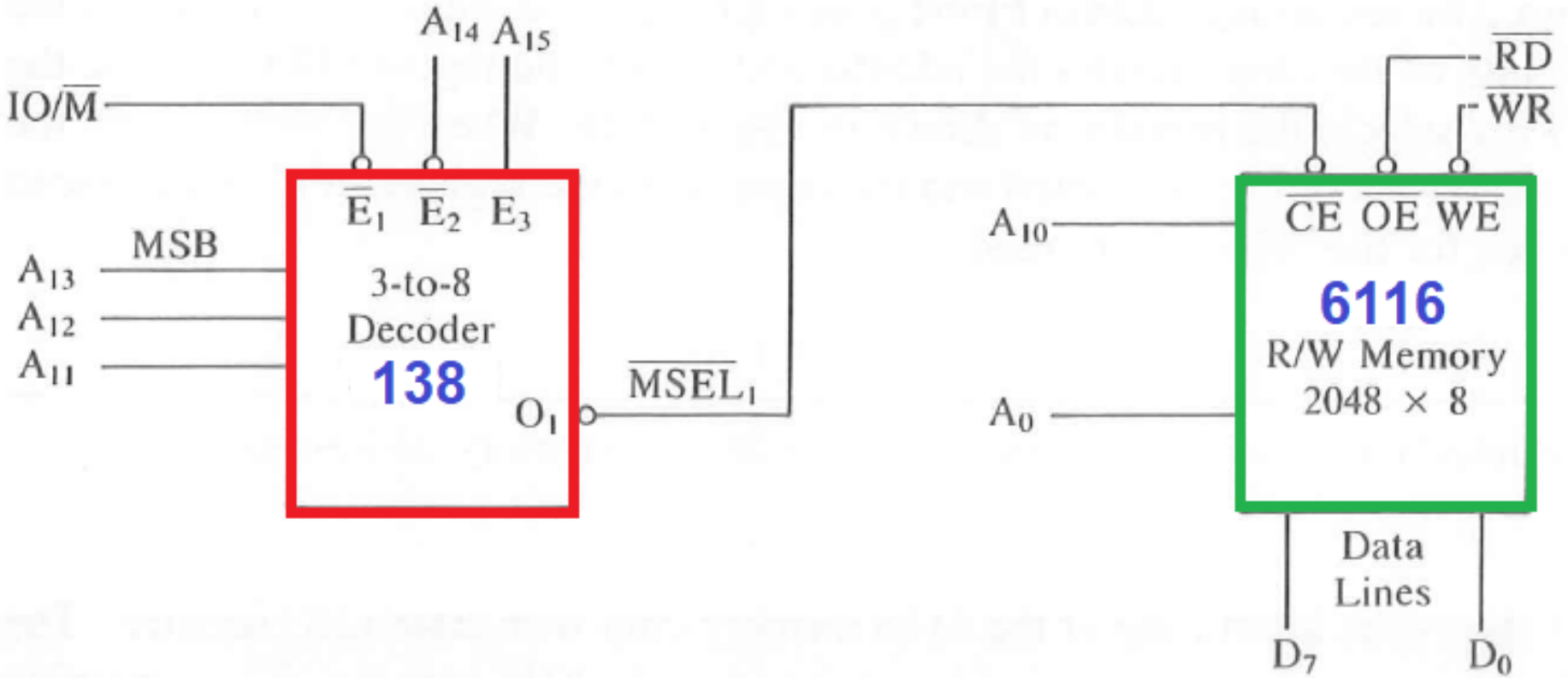
Exercise 2

Design the decoder circuit for ROM memory its address range is 8800 to 8FFF?

1. Determine static bits Most significant 4 bits.
2. Determine dynamic bits:exclude.
3. Design according to static bits.



Exercise 2: 138 decoder solution



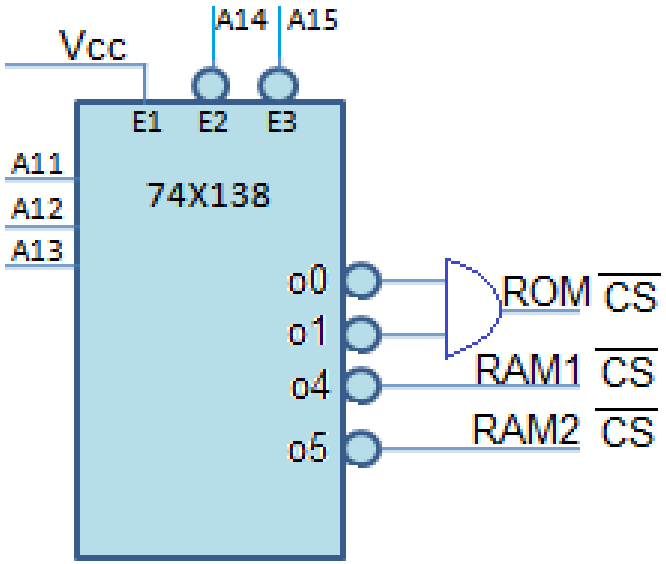
Exercise 2

Design the decoder circuit for ROM memory its address range is 8800 to 8FFF? Solution:

1. Subtract range to find memory size=7FF

Exercise 2

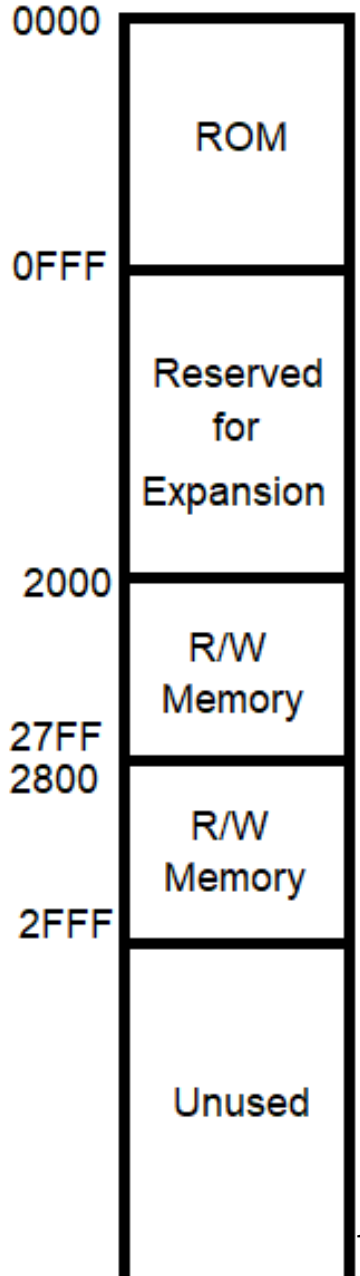
1. Determine static bits:
   ROM vs. RAM $\Rightarrow$ Most significant 4 bits.
   bit no: 13 discriminate
2. Determine static bits:
   RAM vs. RAM $\Rightarrow$ Most significant 5 bits.
   bit no: 11 discriminate



0000 0000 0000 0000
0000 1111 1111 1111

0010 0000 0000 0000
0010 0111 1111 1111

0010 1000 0000 0000
0010 1111 1111 1111



Exercise 3

Design an interfacing circuit for memory to meet the following specifications:

1. 2764 (8k x 8bit): EPROM address range starts from 0000h and additional 4K memory should be available for future use.
2. 6116 (2k x 8bit): CMOS R/W memory.

Exercise 3

2764 (4k x 8bit):

1. Size = 8K=111 1111 1111 11=FFF
2. End address =1FFF+0000=1FFF

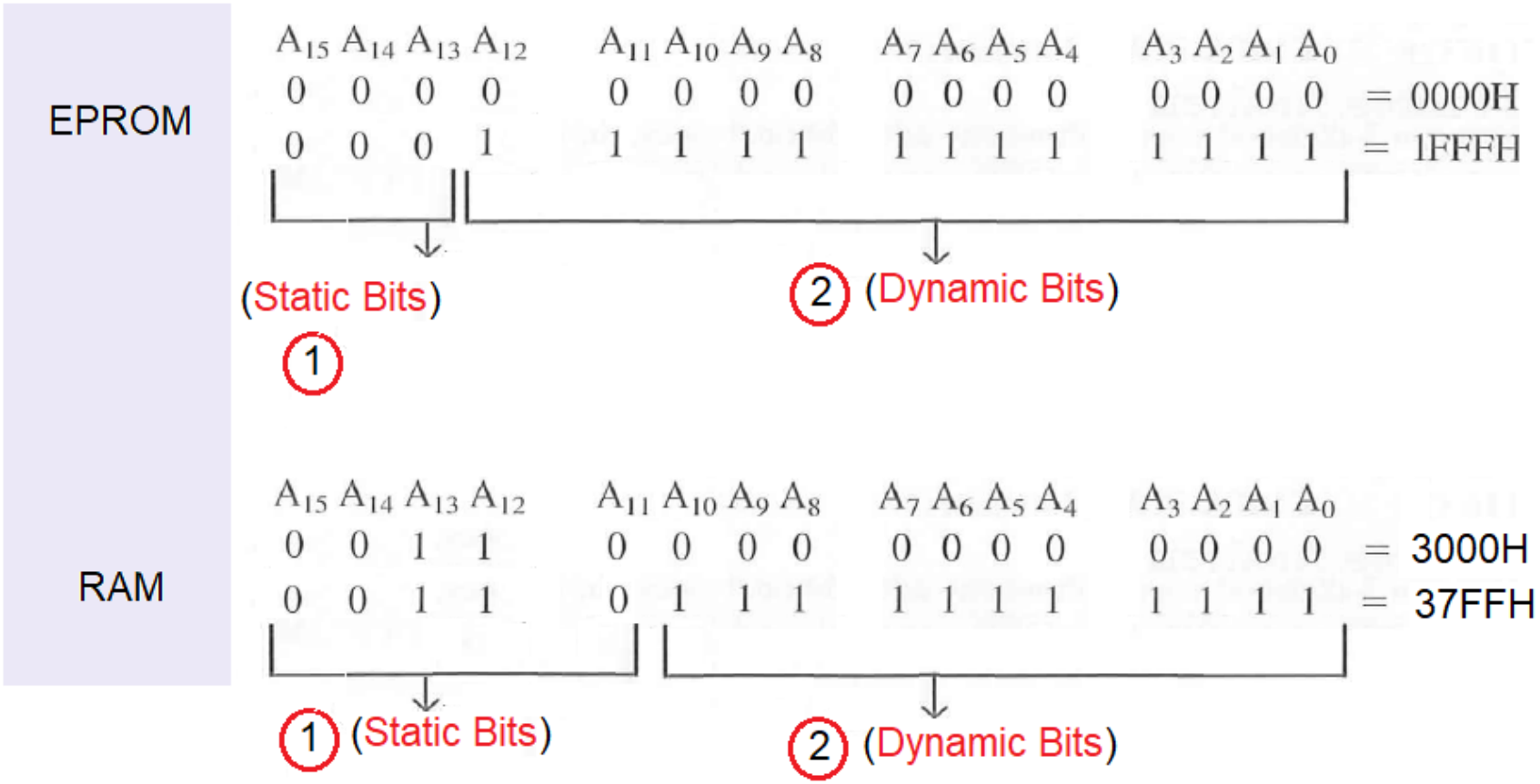
2732 (4k x 8bit) reserved:

1. Size = 4K=11 1111 1111 11=FFF
2. Start address = 1FFF+1=2000
3. End address = FFF+2000=2FFF .

6116 (2k x 8bit)

1. Size = 4K=1 1111 1111 11=7FF
2. Start address = 2FFF+1=3000
3. End address = 7FF+3000=37FF .

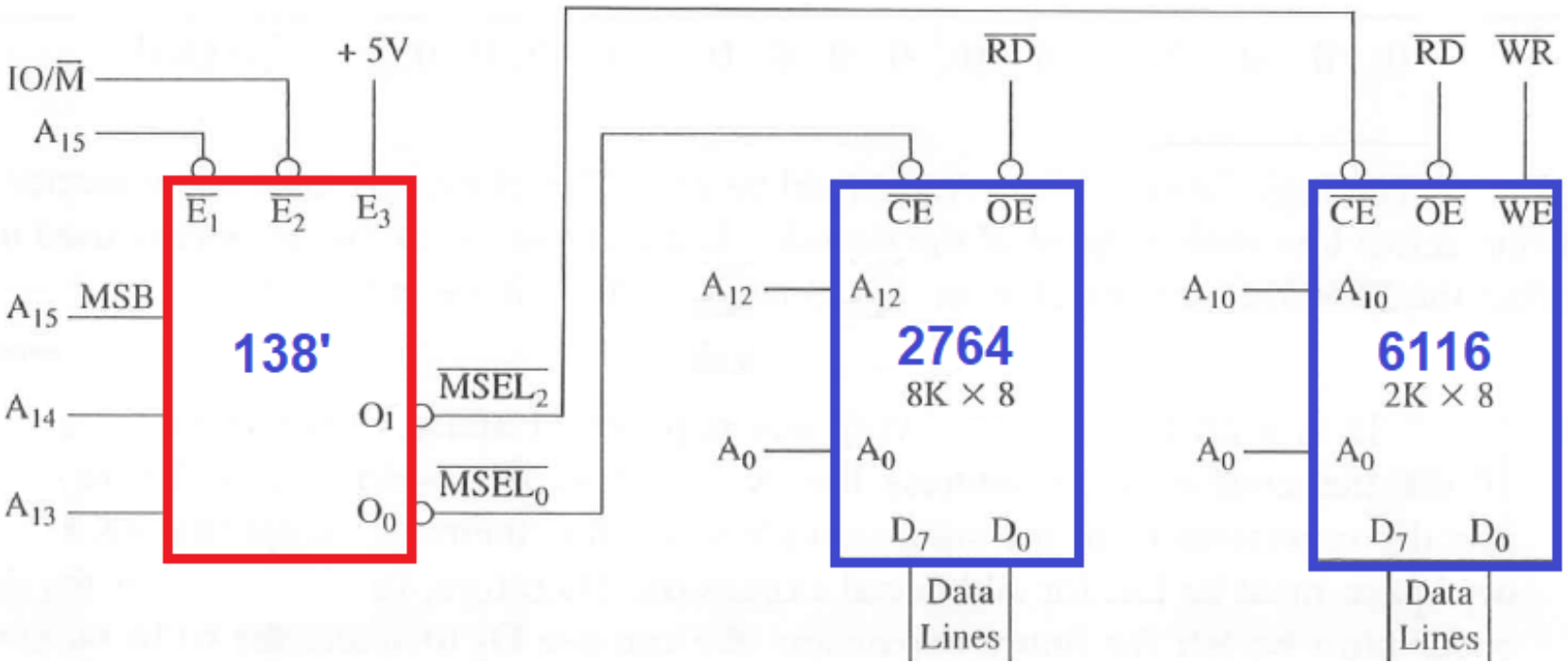
Exercise 3



it is safe to discriminate according to A_{15} , A_{14} , A_{13}

So EPROM=000 RAM= 001

Exercise 3

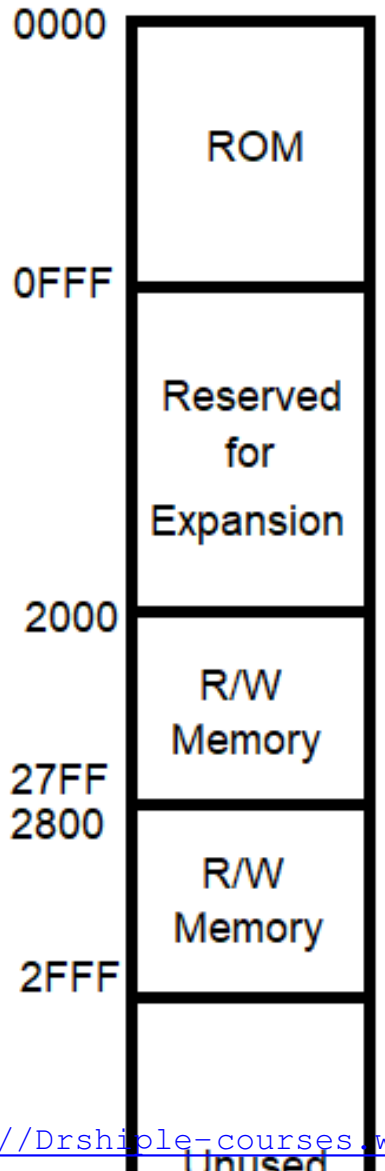


it is safe to discriminate according to A_{15} , A_{14} , A_{13}

So EPROM=000 RAM= 001

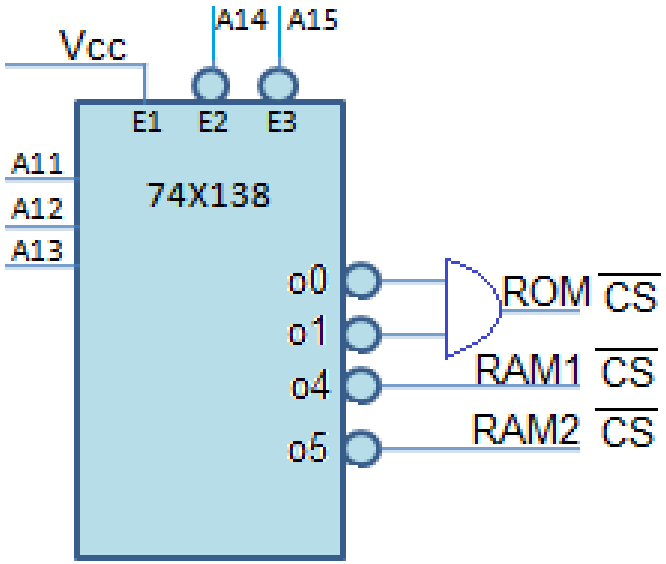
Exercise 4

Design the decoder circuit for shown memory structure?



Exercise 4

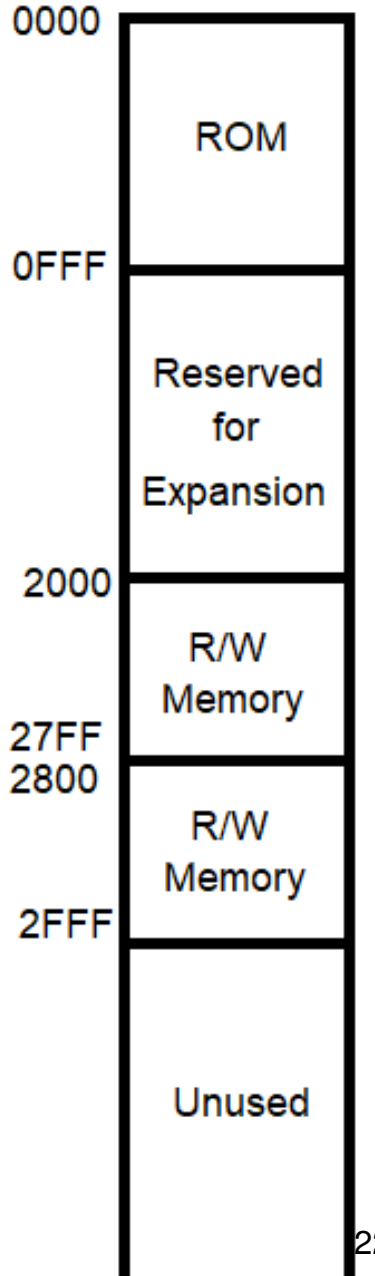
1. Determine static bits:
   ROM vs. RAM $\Rightarrow$ Most significant 4 bits.
   bit no: 13 discriminate
2. Determine static bits:
   RAM vs. RAM $\Rightarrow$ Most significant 5 bits.
   bit no: 11 discriminate



0000 0000 0000 0000
0000 1111 1111 1111

0010 0000 0000 0000
0010 0111 1111 1111

0010 1000 0000 0000
0010 1111 1111 1111



Exercise 4

Draw the memory map of next system