The 8085 Pinout and Timing Analysis

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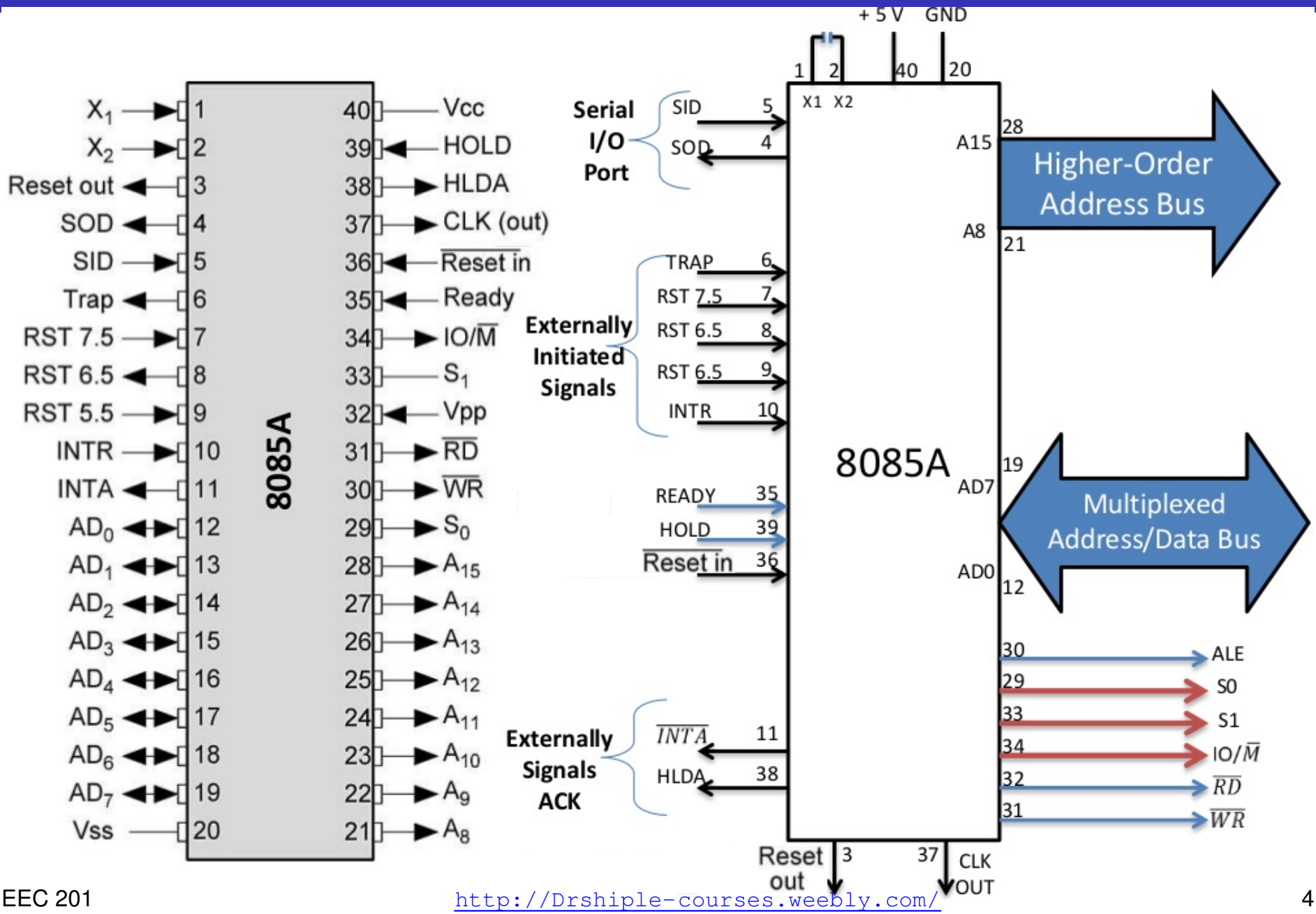
Microprocessor Architecture, 2019


بسم الله الرحمن الرحيم


وقل رب زدني علما

Introduction to Microprocessors

8085 Pinout


8085A
X1 1
X2 2
Reset out 3
SOD 4
SID 5
Trap 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
Vss 20
40 Vcc
39 HOLD
38 HLDA
37 CLK (out)
36 Reset in
35 Ready
34 IO/M
33 S1
32 Vpp
31 RD
30 WR
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8
+5 V
GND
1
2
40
20
X1 X2
Serial I/O Port
SID 5
SOD 4
A15 28
Higher-Order Address Bus
A8 21
Externally Initiated Signals
TRAP 6
RST 7.5 7
RST 6.5 8
RST 6.5 9
INTR 10
8085A
READY 35
HOLD 39
Reset in 36
AD7 19
Multiplexed Address/Data Bus
AD0 12
30 ALE
29 S0
33 S1
34 IO/M
32 RD
31 WR
Externally Signals ACK
INTA 11
HLDA 38
Reset out 3
37 CLK OUT

Power Supply and clock frequency

- V_{CC}, V_{SS}: +5 and GND signals
- X_1, X_2: Crystal inputs. internally the frequency is divide by **two**. therefore to run microprocessor on 3MHz , A 6MHz crystal should be connected.
- CLK: output signal to drive another devices.

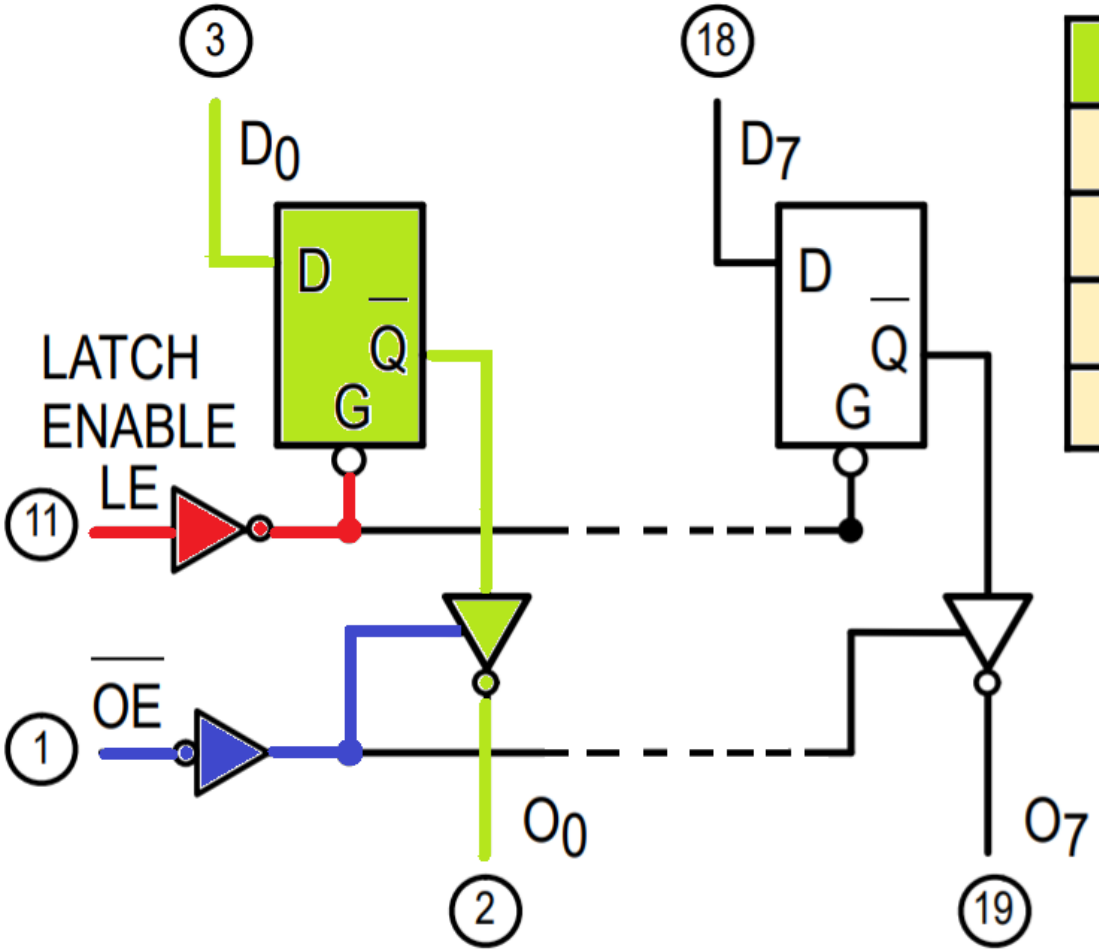
Control Signals

- **ALE:** The address latch enable output is used to demultiplex the address/data bus.
- **$\overline{\text{RD}}$:** This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available on the data bus.
- **$\overline{\text{WR}}$:** This signal indicates that the data on the data bus is to be written into a selected memory or IO location.
- **IO/$\overline{\text{M}}$:** This signal is used to differentiate between IO and Memory operations, i.e. when it is high indicates IO operation and when it is low then it indicates memory operation.
- **S1, and S0 Status inputs:** These signals are used to identify the type of current operation.

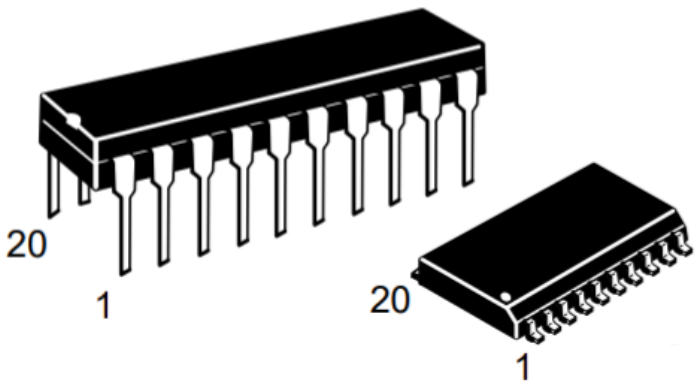
Control Signals (S_0 and S_1)

$IO/\overline{M}$	S1	S0	Status
Z	0	0	Halt
Z	x	x	Hold
Z	x	x	Reset
0	0	1	Memory write
0	1	0	Memory read
0	1	1	Opcode fetch
1	0	1	I/O Write
1	1	0	I/O Read
1	1	1	Interrupt acknowledgment

D-Latch 74ls373



D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z*

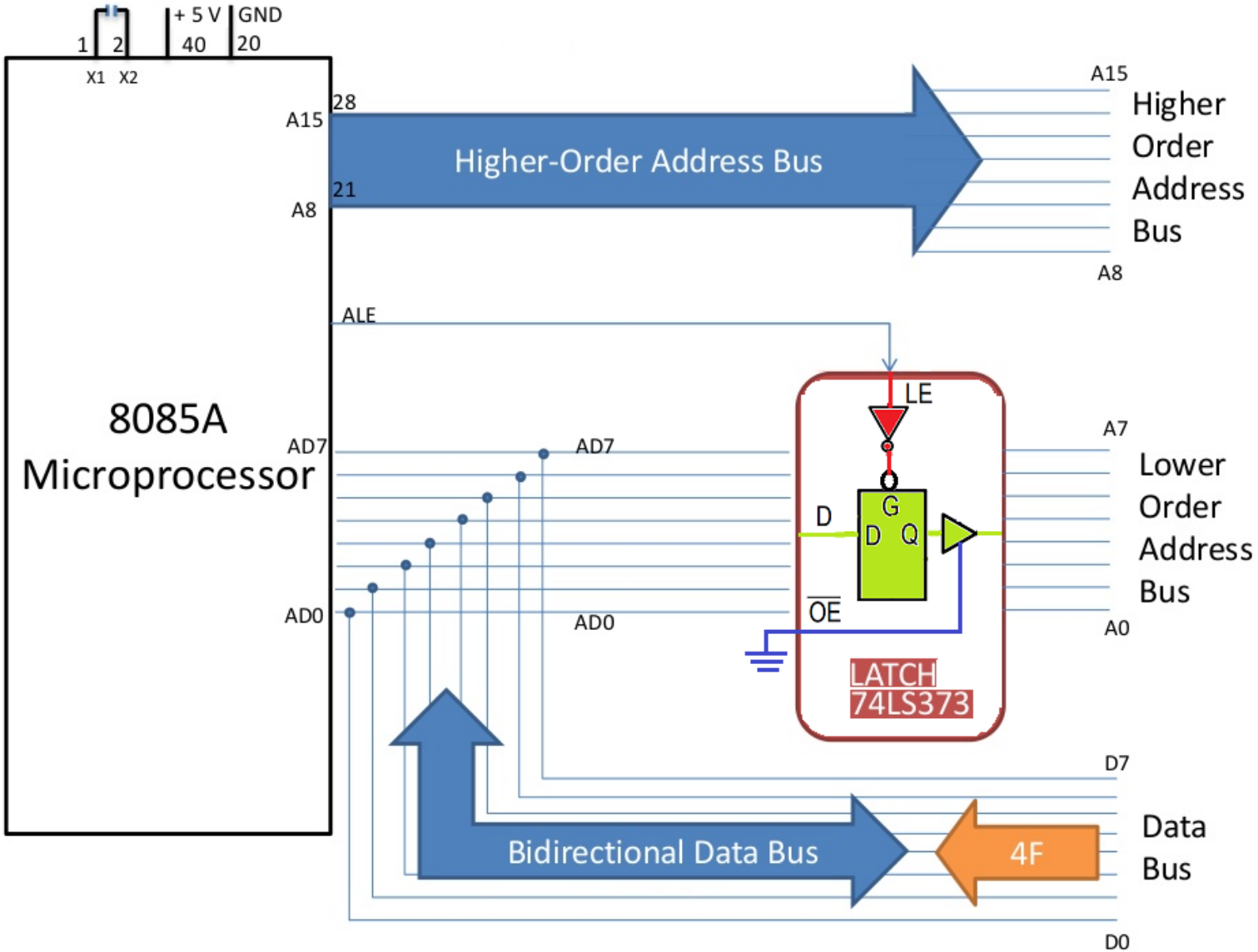


OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

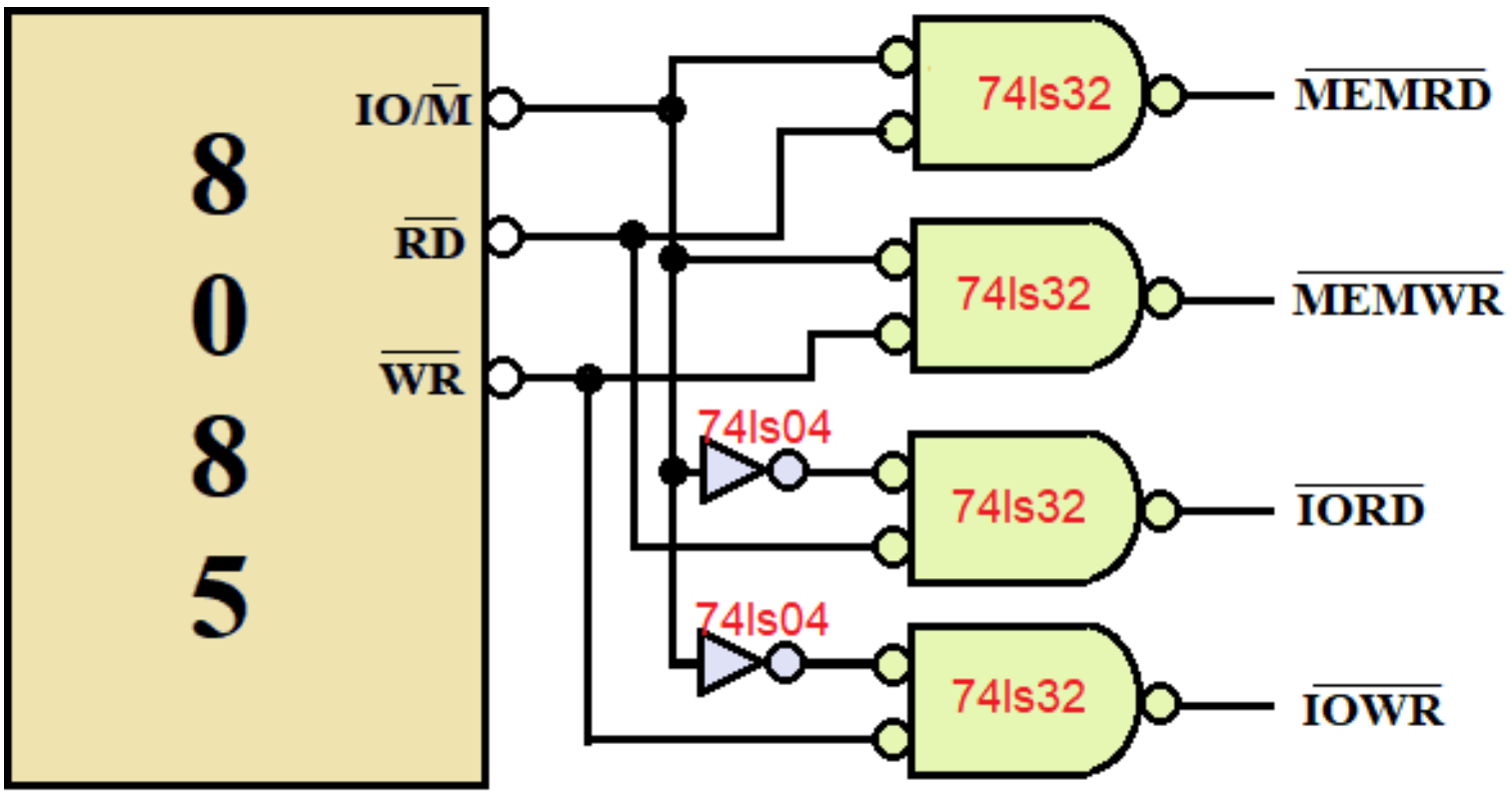
74 series families

- The 74LS (Low-power Schottky) family uses TTL (Transistor Transistor Logic) circuitry which is fast but requires more power.
- The 74HC family has High-speed CMOS circuitry, combining the speed of TTL with low power consumption of the 4000 series. Note that 74HC inputs cannot be reliably driven by 74LS outputs because the voltage ranges used for logic 0 are not quite compatible.
- The 74HCT family is a special version of 74HC with 74LS TTL-compatible inputs so 74HCT can be safely mixed with 74LS in the same system. The minor disadvantage of 74HCT is a lower immunity to noise.
- For most new projects the 74HC family is the best choice.

Bus Demultiplexing



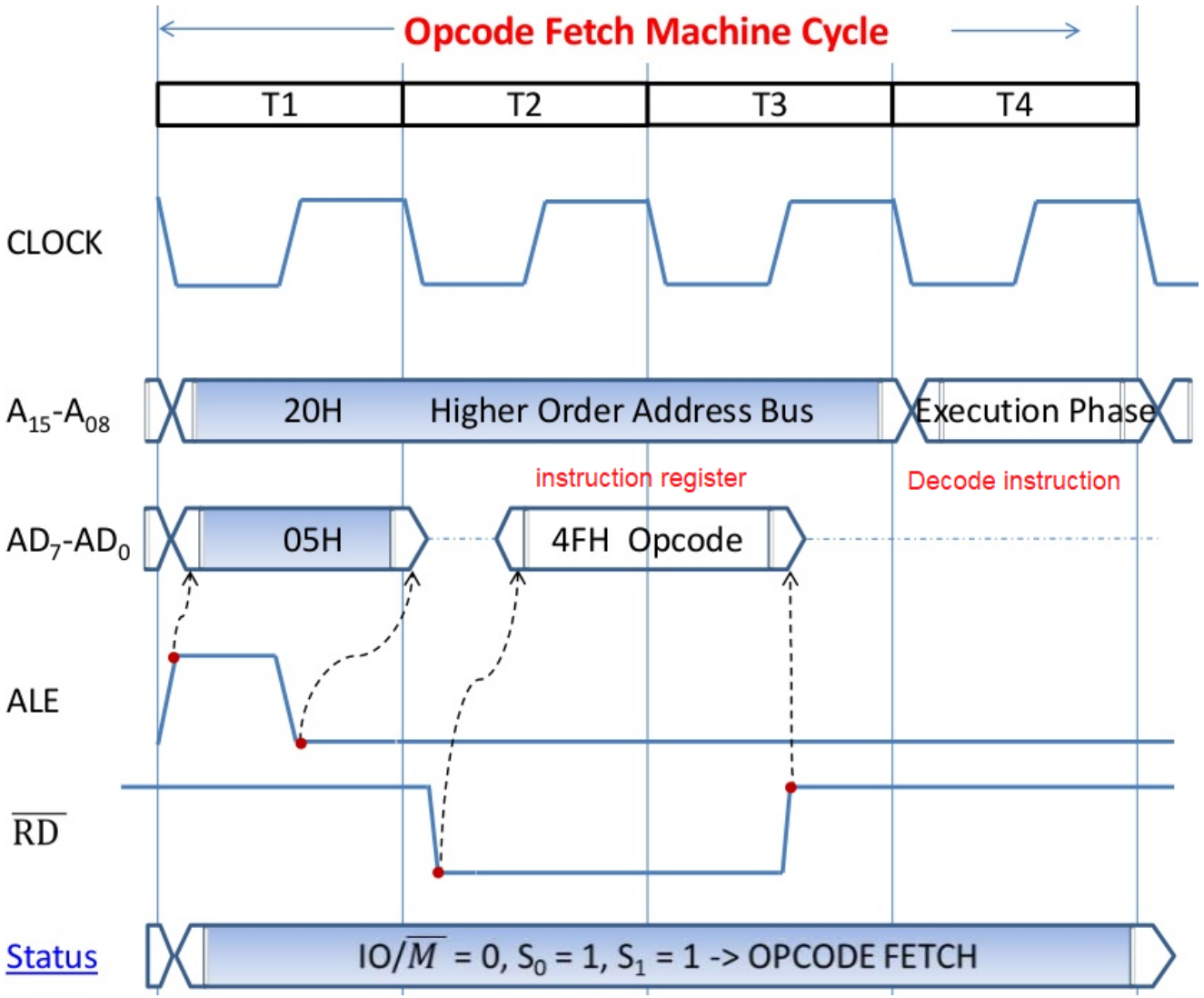
RD/WR Control circuit



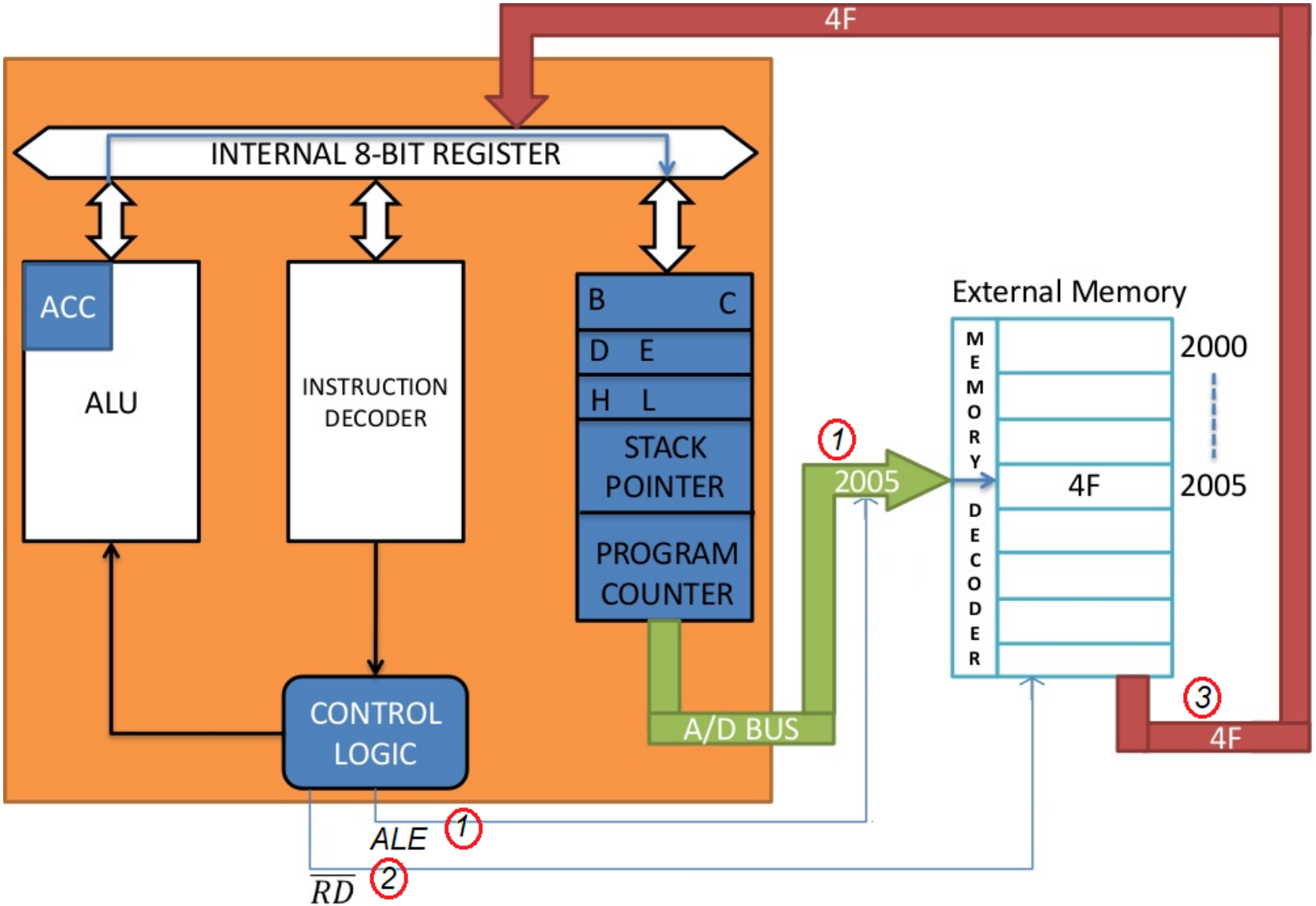
Example: Opcode Fetching

Fetch opcode:
{MOV C, A }
HEX:4Fh,
Mem add.: 2005h

fetch machine cycle called: M1
#T states= 4 states
fetching: T1,T2,T3
Decoding:T4



Timing of 8085



Timing of 8085

Machine Cycle

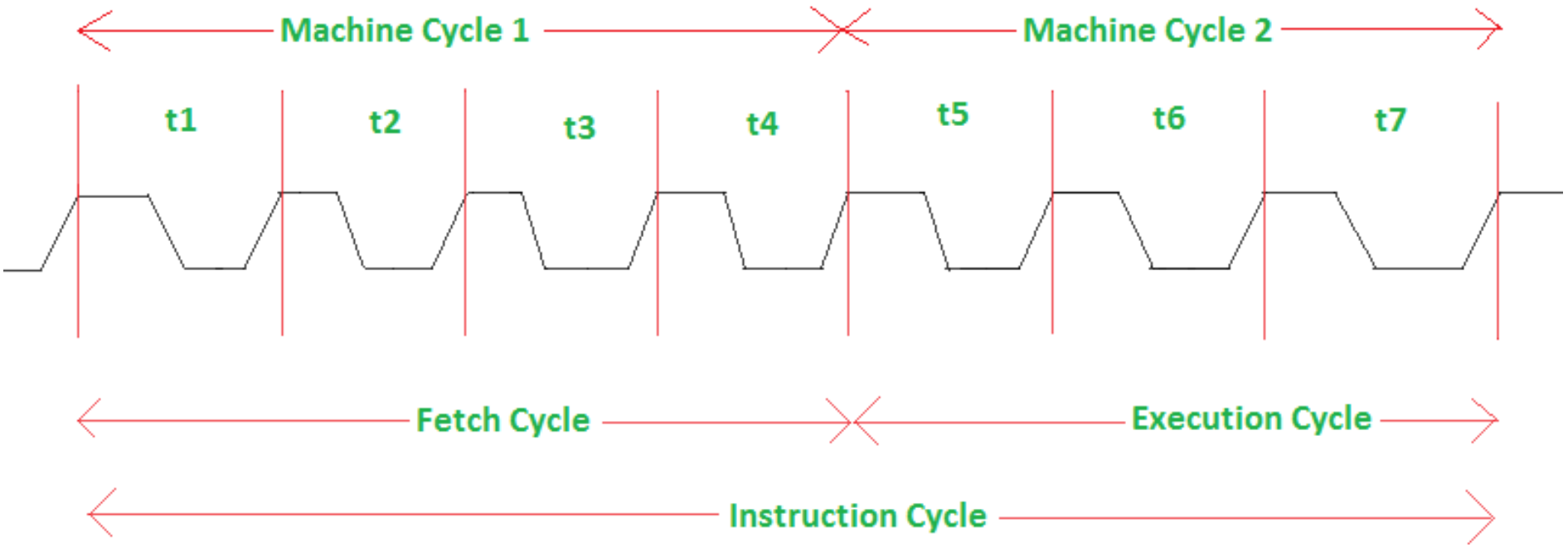
The time required by the microprocessor to complete an operation of accessing memory or input/output devices (consistes of three to six T-states)

- **Fetch Cycle:** needs machine cycle.
- **Execution cycle :** needs machine cycle.

Timing of 8085

T-state

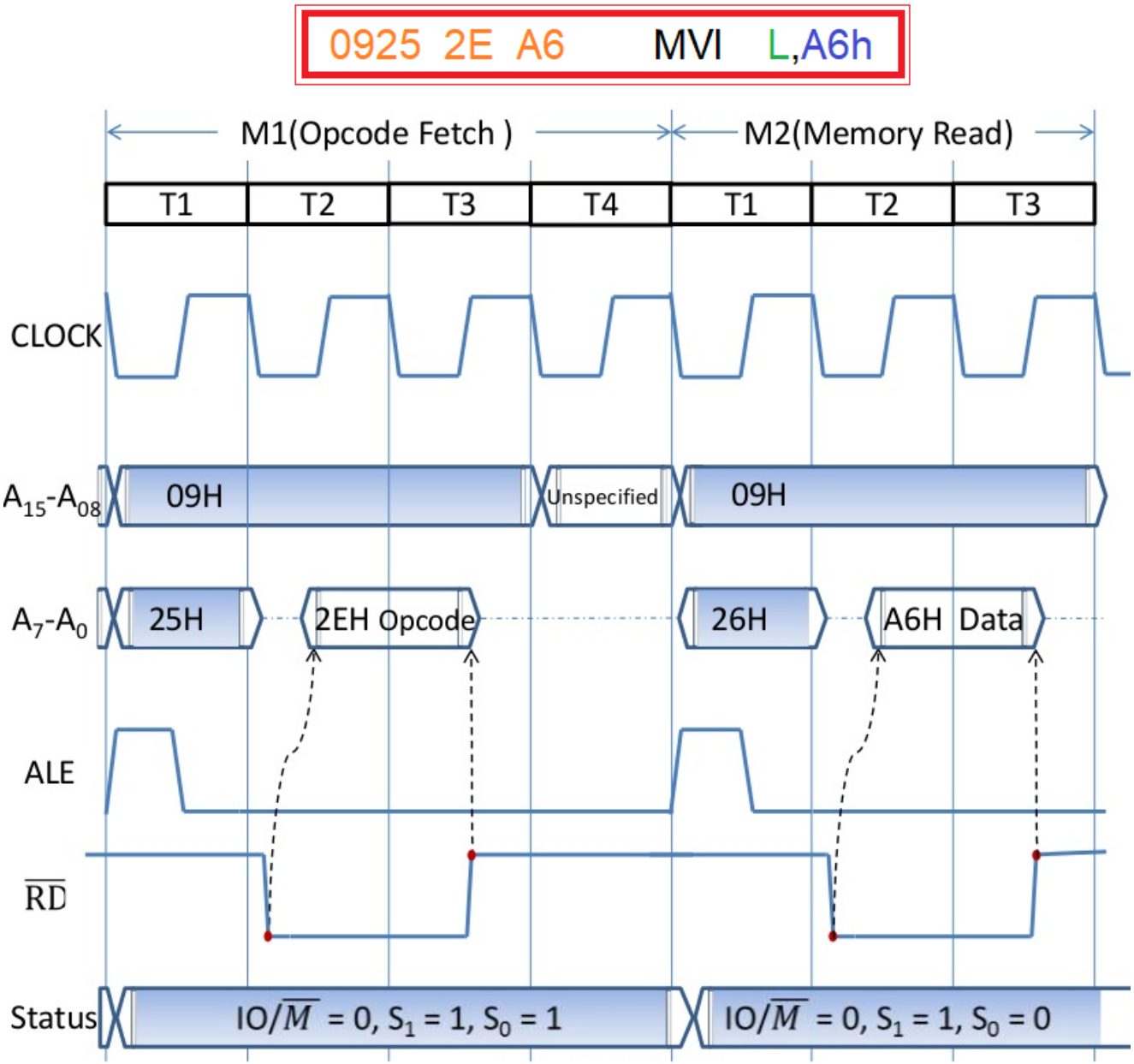
One time period of frequency of microprocessor. A t-state is measured from the falling edge of one clock pulse to the falling edge of the next clock pulse.



8085 Machine Cycle:

1. Opcode fetch machine cycle (4T)
2. Memory read machine cycle (3 T)
3. Memory write machine cycle (3 T)
4. I/O read machine cycle (3 T)
5. I/O write machine cycle (3 T)
6. Interrupt acknowledge machine cycle (3 T)
7. Bus idle machine cycle (6 T)

Ex:2 bytes


0925 2E A6 MVI L,A6h
M1(Opcode Fetch)
M2(Memory Read)
T1
T2
T3
T4
T1
T2
T3
CLOCK
A15-A08
09H
Unspecified
09H
A7-A0
25H
2EH Opcode
26H
A6H Data
ALE
RD
Status
IO/M = 0, S1 = 1, S0 = 1
IO/M = 0, S1 = 1, S0 = 0

Ex:2 bytes (Opcode Fetch Machine Cycle)

OPFMC: $IO/\overline{M} = 0$, $S_1 = 1$, $S_0 = 1$
T_1: AD_0–$AD_7 \leftarrow PC_0$–PC_7; A_8–$A_{15} \leftarrow PC_8$–PC_{15}; ALE
T_2: PC = PC + 1; $\overline{RD} = 0$; BDB ← M (AB)
T_3: $\overline{RD} = 1$; IR ← BDB
T_4: MVI r, data F/F is set

OPFMC:

During T_1 state the address from the PC (Program Counter) is transferred to the address bus and ALE signal is made active.

During T_2 state, the PC is incremented by one and $\overline{RD}$ signal is made low. The contents of memory whose address is available on the address bus are loaded into the bi-directional data bus.

During T_3 state, the $\overline{RD}$ signal is made high. During this process, the contents of the BDB are read into the internal bus and thus into the instruction register.

During T_4 state, the microprocessor makes the MVI r, data F/F set indicate so it requires another machine cycle i.e., MRDMC to complete the instruction cycle.

PC: Program Counter IR: instruction Register BDB: Bidirectional Data Bus AB: Address Bus

Ex:2 bytes (Memory Read Machine Cycle)

MRDMC: IO/$\overline{M}$ = 0, S_1 = 1, S_0 = 0
T_1: AD_0–AD_7 ← PCL; A_8–A_{15} ← PCH; ALE
T_2: PC ← PC+1; $\overline{RD}$ = 0; BDB ← M (PC)
T_3: $\overline{RD}$ = 1; r ← (BDB)

MRDMC:
During T_1 state of this machine cycle, the content of PC register is loaded on to the address bus. ALE signal is made active.

During T_2 state, the $\overline{RD}$ signal is made low and the data from the memory pointed by the address on the address bus is loaded into the BDB. The PC is incremented as the contents of PC are sent to get the next byte of the instruction.

During T_3 state, the $\overline{RD}$ signal is made high and the data from the BDB is transferred into the register mentioned in the instruction.

Ex: MVI M,85h

OPFMC: $IO/\overline{M} = 0,\ S_1 = 1,\ S_0 = 1$

T_1: A_{15}–$A_8 \leftarrow$ (PCH); AD_7–$AD_0 \leftarrow$ (PCL); ALE

T_2: PC $\leftarrow$ PC + 1; $\overline{RD} = 0$; BDB $\leftarrow$ M (AB)

T_3: $\overline{RD} = 1$; IR $\leftarrow$ BDB

T_4: MVI M F/F is set to 1

MRDMC: $IO/\overline{M} = 0,\ S_1 = 1,\ S_0 = 0$

T_1: AD_0–$AD_7 \leftarrow$ PCL; A_8–$A_{15} \leftarrow$ PCH; ALE

T_2: PC $\leftarrow$ PC + 1; $\overline{RD} = 0$; BDB $\leftarrow$ M (AB)

T_3: $\overline{RD} = 1$; Z $\leftarrow$ (BDB)

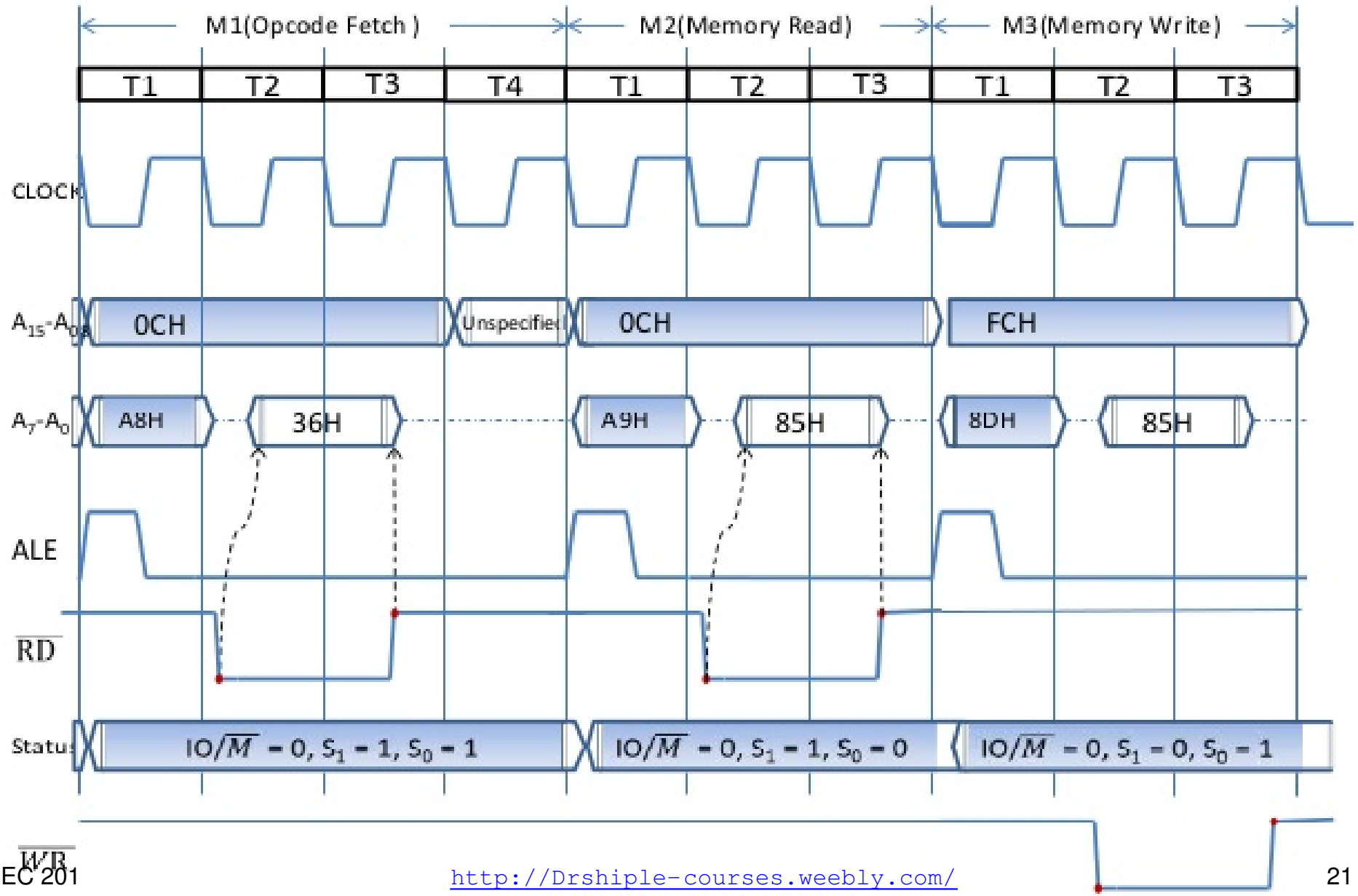
MWRMC: $IO/\overline{M} = 0\ S_1 = 0,\ S_0 = 1$

T_1: A_{15}–$A_8 \leftarrow$ (H); AD_7–$AD_0 \leftarrow$ (L); ALE

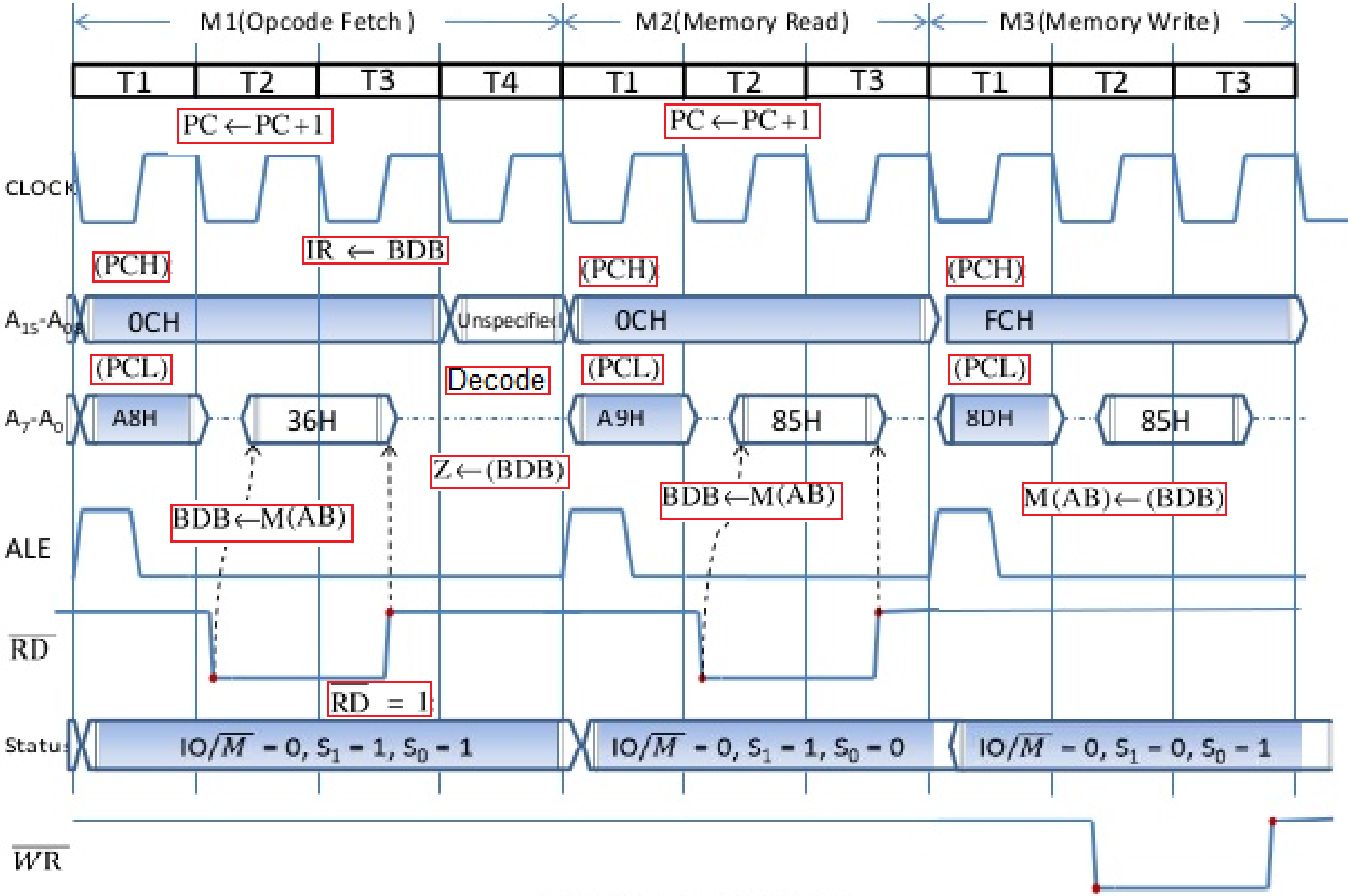
T_2: $\overline{WR} = 0$; $(AD_7$–$AD_{0)}) \leftarrow$ Z;

T_3: $\overline{WR} = 1$; M (AB) $\leftarrow$ (BDB)

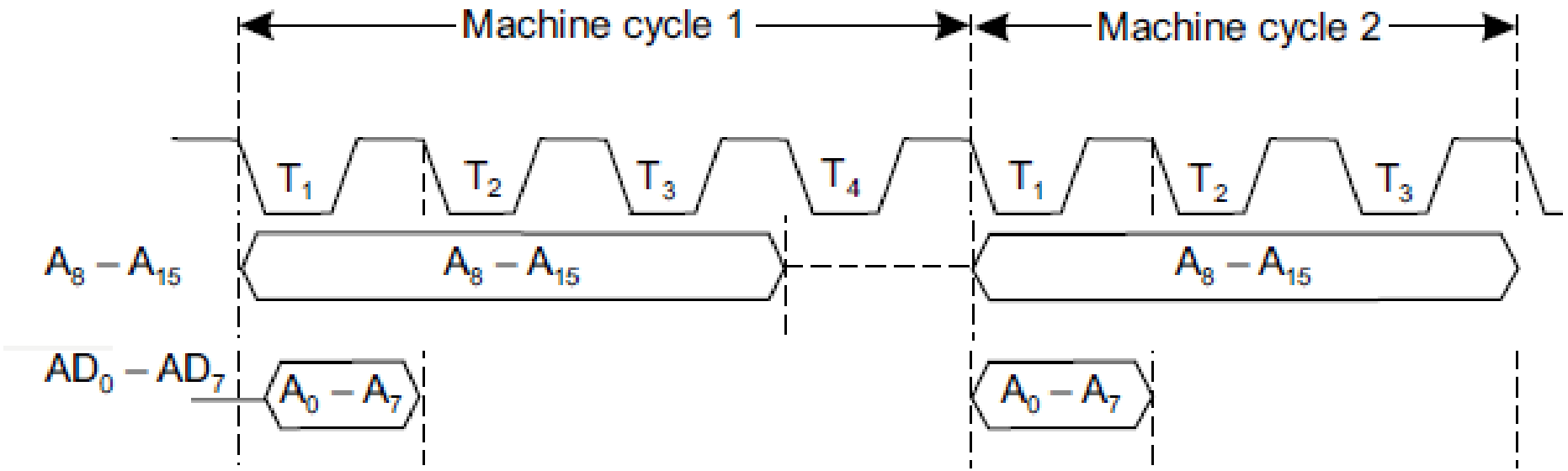
Ex: MVI M,85h


M1(Opcode Fetch)
M2(Memory Read)
M3(Memory Write)
T1
T2
T3
T4
T1
T2
T3
T1
T2
T3
CLOCK
A_{15}-A_8
0CH
Unspecified
0CH
FCH
A_7-A_0
A8H
36H
A9H
85H
8DH
85H
ALE
RD
Status
IO/M = 0, S1 = 1, S0 = 1
IO/M = 0, S1 = 1, S0 = 0
IO/M = 0, S1 = 0, S0 = 1
WR

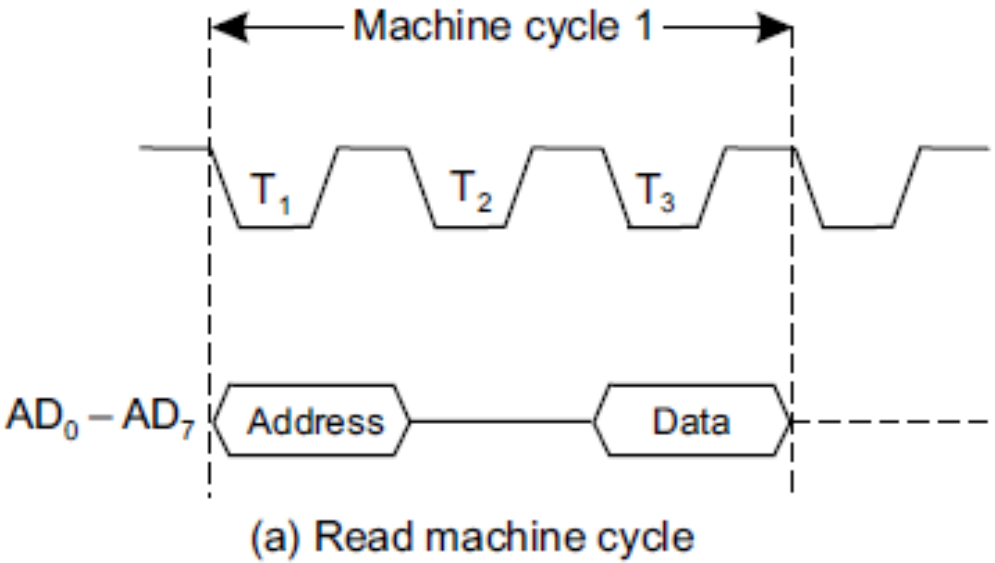
Ex: MVI M,85h


M1(Opcode Fetch)
M2(Memory Read)
M3 (Memory Write)
T1
T2
T3
T4
T1
T2
T3
T1
T2
T3
PC ← PC + 1
PC ← PC + 1
CLOCK
IR ← BDB
(PCH)
(PCH)
(PCH)
A15-A8
0CH
Unspecified
0CH
FCH
(PCL)
Decode
(PCL)
(PCL)
A7-A0
A8H
36H
A9H
85H
8DH
85H
Z ← (BDB)
BDB ← M(AB)
BDB ← M(AB)
M(AB) ← (BDB)
ALE
RD
RD = 1
Status
IO/M = 0, S1 = 1, S0 = 1
IO/M = 0, S1 = 1, S0 = 0
IO/M = 0, S1 = 0, S0 = 1
WR

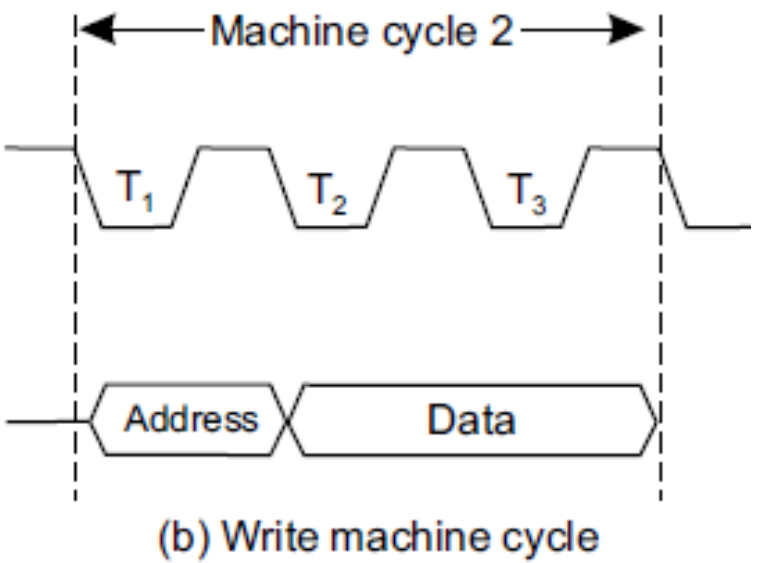
Note: address bus during the machine cycles



Note: address bus during the machine cycles



(a) Read machine cycle



(b) Write machine cycle

Excercise 1:

Draw the timing diagram of next instruction

INR M ;M=M+1

Memory map:

Address	Mnemonics	Code
4105	INR M	34h
4250		12h

Register map:

Register	Value
A	34h
H	42h
L	50h

Excercise 1:

Draw the timing diagram of next instruction

INR M ;M=M+1

Memory map:

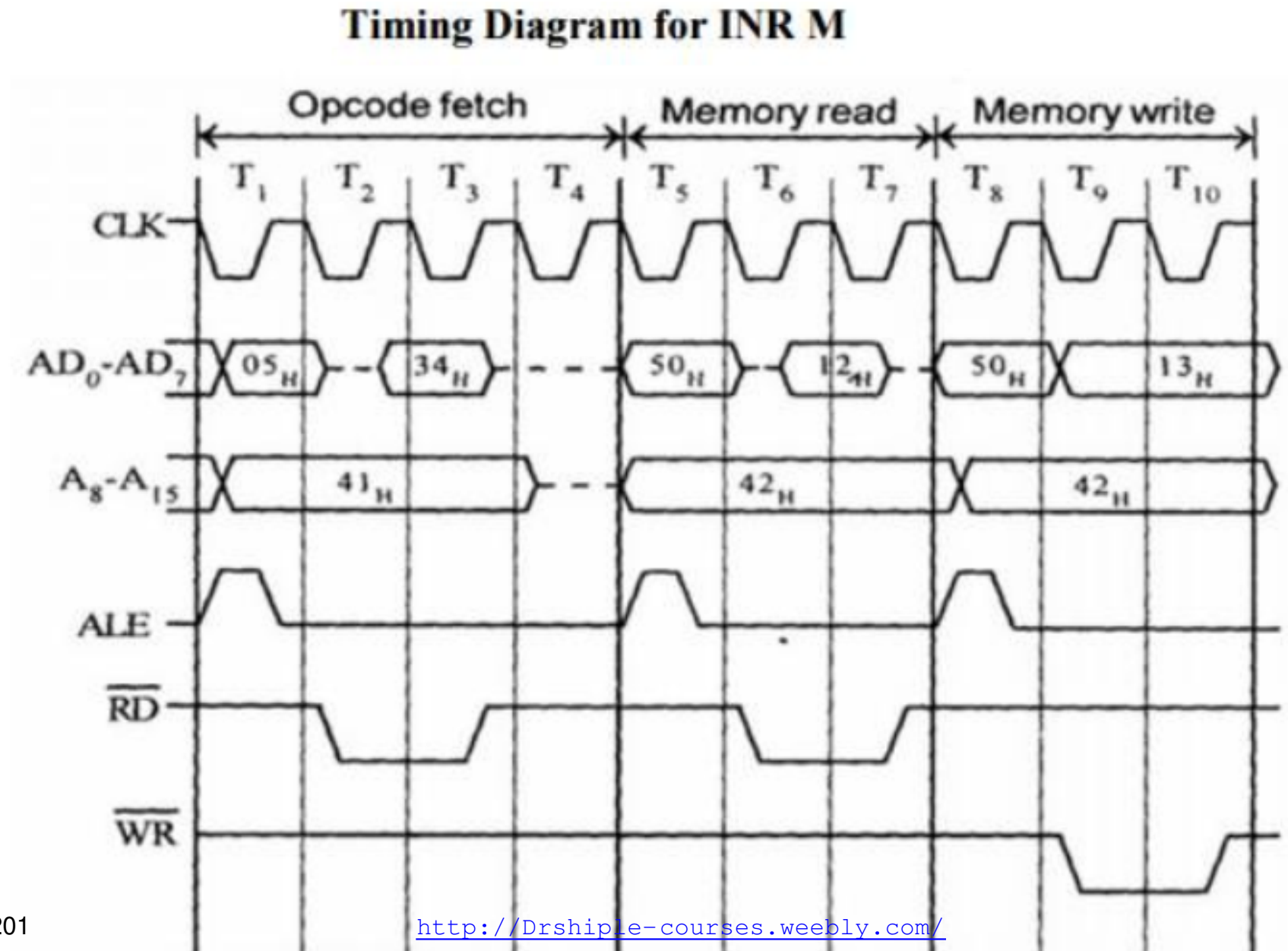
Address	Mnemonics	Code
4105	INR M	34h
4250		12h

Register map:

Register	Value
A	34h
H	42h
L	50h

1. Fetching the Opcode 34H from the memory 4105H. (OPFMC cycle).
2. Let the memory address (M) be 4250H. (MRDMC cycle).
3. Increment the memory content from 12H to 13H. (MWRMC machine cycle).

Excercise 1:


Timing Diagram for INR M
Opcode fetch
Memory read
Memory write
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CLK
AD0-AD7
05H
34H
50H
12H
50H
13H
A8-A15
41H
42H
42H
ALE
RD
WR

Excercise 2:

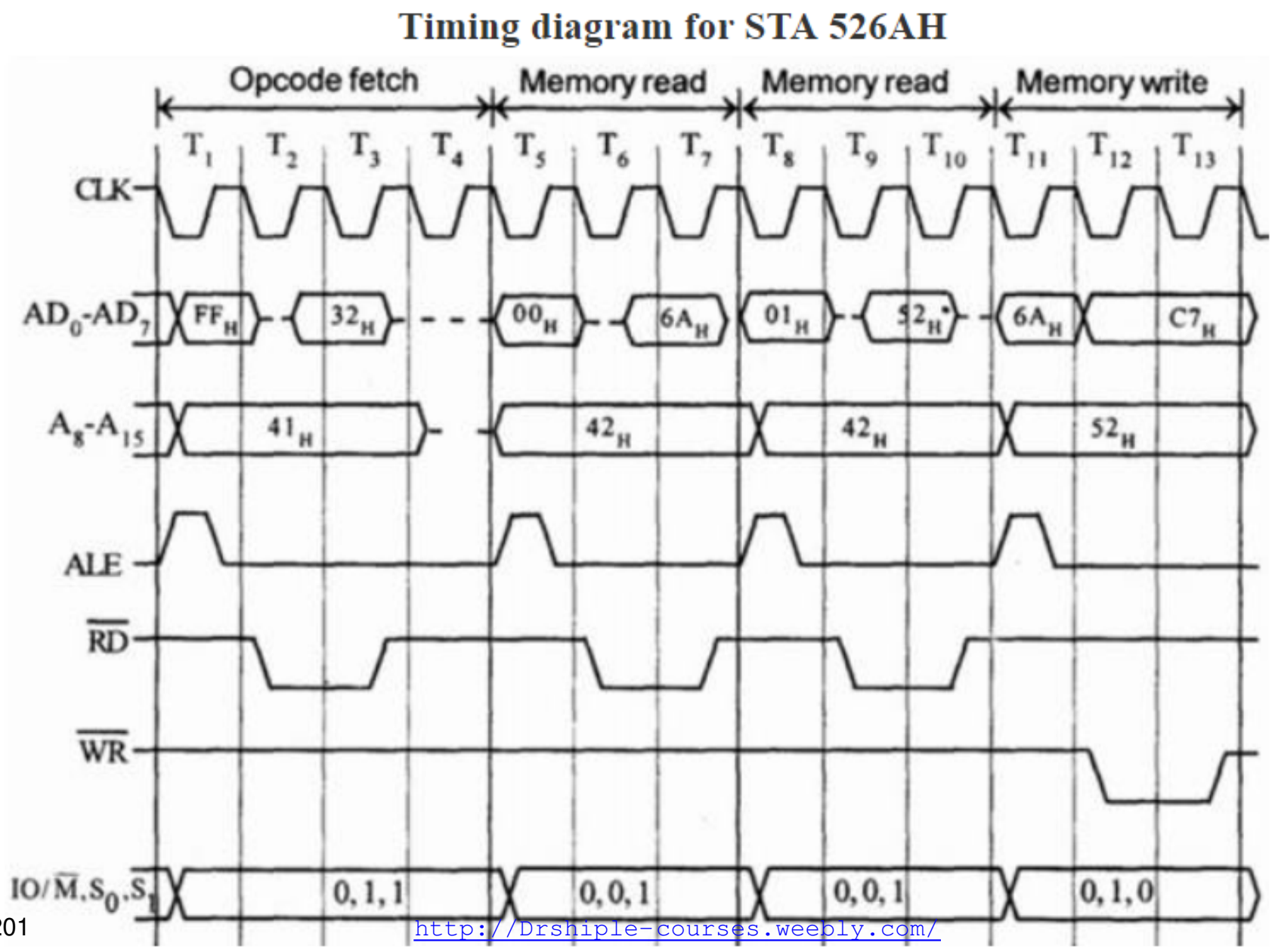
Draw the timing diagram of next instruction

STA 526Ah ;[a]=A

Memory map:

Address	Mnemonics	Code
41FF	STA 526Ah	32h
4200		6Ah
4201		52h

Excercise 2:


Timing diagram for STA 526AH
Opcode fetch
Memory read
Memory read
Memory write
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
CLK
AD0-AD7
FFH
32H
00H
6AH
01H
52H
6AH
C7H
A8-A15
41H
42H
42H
52H
ALE
RD
WR
IO/M, S0, S1
0, 1, 1
0, 0, 1
0, 0, 1
0, 1, 0

Five machine cycles

Micro RTL: SHLD ADDR

OPFMC: IO/$\overline{M}$ = 0, S_1 = 1, S_0 = 1

T_1: A_{15}–A_8 ← (PCH); AD_7–AD_0 ← (PCL); ALE

T_2: PC ← PC + 1; $\overline{RD}$ = 0; BDB ← M (AB)

T_3: $\overline{RD}$ = 1; IR ← BDB

T_4: SHLD ADDR FF = 1

MRDMC: IO/$\overline{M}$ = 0, S_1 = 1, S_0 = 0

T_1: AD_0–AD_7 ← PCL; A_8–A_{15} ← PCH; ALE

T_2: PC ← PC + 1; $\overline{RD}$ = 0; BDB ← M (AB)

T_3: $\overline{RD}$ = 1; Z ← (BDB)

MRDMC: IO/$\overline{M}$ = 0, S_1 = 1, S_0 = 0

T_1: AD_0–AD_7 ← PCL; A_8–A_{15} ← PCH; ALE

T_2: PC ← PC + 1; $\overline{RD}$ = 0; BDB ← M (AB)

T_3: $\overline{RD}$ = 1; W ← (BDB)

MWRMC: IO/$\overline{M}$ = 0, S_1 = 0, S_0 = 1

T_1: AD_0–AD_7 ← Z; A_8–A_{15} ← W; ALE

T_2: $\overline{WR}$ = 0; BDB ← (L)

T_3: $\overline{WR}$ = 1; M (AB) ← BDB

MWRMC: IO/$\overline{M}$ = 0, S_1 = 0, S_0 = 1

T_1: AD_0–AD_7 ← Z + 1; A_8–A_{15} ← W; ALE

T_2: $\overline{WR}$ = 0; BDB ← (H)