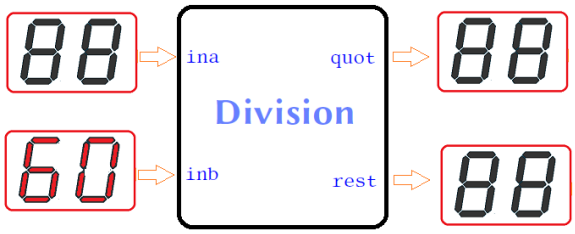
Examiner : Dr. Mustafa M. Shiple
Subject: Selected Topics in Electronics /(ECE 569)
Score: 5 Marks

Term: Spring 2018
Exam Time:20 min

ANSWER THE FOLLOWING QUESTIONS:

1. Write a VHDL code to implement a minute-to-hours converter, that accepts two digits and results in the binary equivalent value.

Solution:



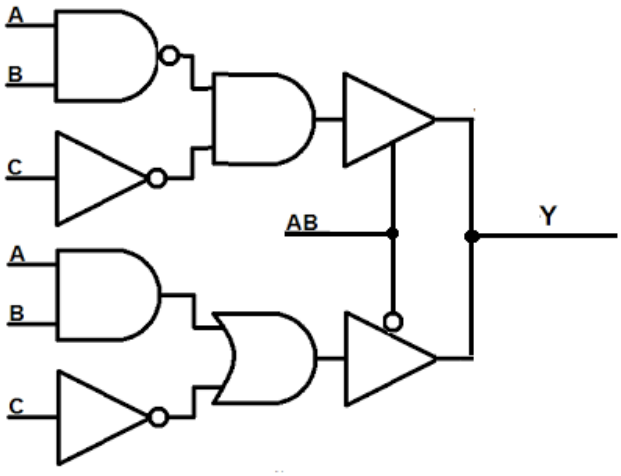

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.numeric_STD.ALL;
4
5  entity div_binary is
6          Port (ina, inb : in std_logic_vector (15 downto 0);
7          quot, rest:  out std_logic_vector (15 downto 0);
8  end div_binary;
9
10 architecture Behavioral of div_binary is
11 begin
12         process (ina, inb)
13         variable temp1: std_logic_vector (30 downto 0):=(others
               =>'0');
14         variable temp2: std_logic_vector (30 downto 0):=(others
               =>'0');
15         begin
16                 temp1(15 downto 0):=ina;
17                 temp2(30 downto 15) :=inb;
18                 for i in 15 downto 0 loop
19                         if (temp1>temp2 ) then
20                                 quot(i):= '1';
21                                 temp1:=std_logic_vector(unsigned(
                                       temp1)-unsigned(temp2));
22                         else quot(i):= '0';
23                         end if;
24                         temp2:='0'&temp2(30 downto 1);
25                 end loop;
26                 rest <= temp1;
27         end process;
28 end Behavioral;
```

[Total Marks is 5]

Signature of Examiner:

Good Luck
Head of Dept.:

2. Write a VHDL entity code that realizes the shown circuit.



Solution:

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  ---------------------------------------------------
4  ENTITY vhdl1 IS
5  PORT ( a,b,c,ab  : IN STD_LOGIC;
6  y : out STD_logic);
7  END vhdl1;
8  ---------------------------------------------------
9  ARCHITECTURE example OF vhdl1 IS
10 SIGNAL and_out,or_out : STD_logic;
11 BEGIN
12 and_out<= (a nand b) and not c;
13 or_out<= (a and b) or not c;
14 y_temp<='z' when ab='1' else and_out;
15 y_temp2<='z' when ab='0' else or_out;
16 -- Multiple driver
17 y<= y_temp or y_temp2;
18
19 END example;
20 ---------------------------------------------------
```