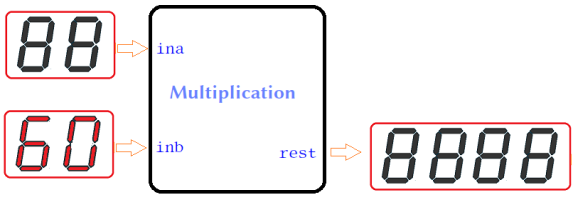
Examiner : Dr. Mustafa M. Shiple
Subject: Selected Topics in Electronics /(ECE 569)
Score: 5 Marks

Term: Spring 2018
Exam Time:20 min

ANSWER THE FOLLOWING QUESTIONS:

1. Write a VHDL code to implement a minute-to-seconds converter, that accepts two digits and results in the binary equivalent value.

Solution:




```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.numeric_STD.ALL;
4
5  entity div_binary is
6  Port (ina, inb : in std_logic_vector (15 downto 0);
7   result:  out std_logic_vector (30 downto 0);
8  end div_binary;
9
10 architecture Behavioral of div_binary is
11 begin
12 process (ina, inb)
13 variable acc: std_logic_vector (30 downto 0):=(others
       =>'0');
14 variable temp: std_logic_vector (30 downto 0):=(others
       =>'0');
15 begin
16  acc := (others => '0');
17 temp := "0000" & ina ;
18 for j in 0 to 3 loop
19 if (inb(j)='1') then
20 c(0):='0';
21 for i in 0 to 7 loop
22 sum(i) <= acc(i) xor temp(i) xor c(i);
23 c(i+1):=(acc(i)and temp(i))or(acc(i)and c(i))or(c(i)and
       temp(i));
24 end loop;
25 acc :=sum;
26 end if;
27 temp:= temp(6 downto 0) & '0';
28 end loop;
29 result <= acc;
```

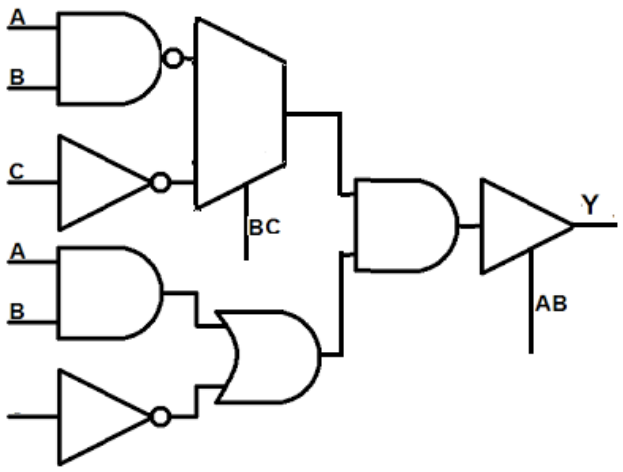
[Total Marks is 5]

Signature of Examiner:

Good Luck
Head of Dept.:

```
30          end process;
31          end Behavioral;
```

2. Write a VHDL entity code that realizes the shown circuit.



Solution:

```
1           LIBRARY ieee;
2       USE ieee.std_logic_1164.all;
3       ---------------------------------------------
4       ENTITY vhdl1 IS
5       PORT ( a,b,c,ab   : IN STD_LOGIC;
6       y : out STD_logic);
7       END vhdl1;
8       ---------------------------------------------
9       ARCHITECTURE example OF vhdl1 IS
10      SIGNAL or_out,mux_out : STD_logic;
11      BEGIN
12      mux_out<= (a nand b) when bc='0' else not c;
13      or_out<= (a and b) or not c;
14
15      y<= 'z' when ab='1' else (mux_out and or_out);
16
17      END example;
```