Examiner : Dr. Mustafa M. Shiple
Subject: Selected Topics in Electronics /(ECE 569)
Score: 5 Marks

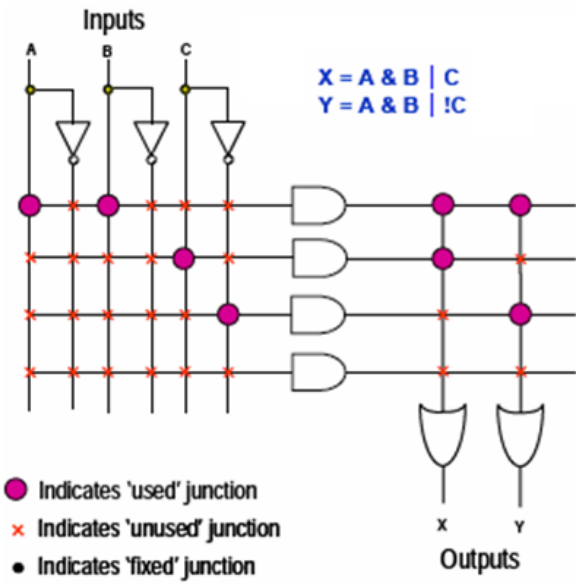
Term: Spring 2018
Exam Time:20 min

**ANSWER THE FOLLOWING QUESTIONS:**

1. Briefly discuss pros and cons of simple PAL

**Solution:**

- Any combination of ANDs/ORs
- High Input-to-output delay (or propagation delay)
- Wafer geometries of $10\mu m$ technology




2. Consider the next VHDL code:
   (a) Check and correct syntax errors.
   (b) Synthesize the next code, and Draw the circuit.

```
1  LIBRARY ieee;
2  USE ieee.std_logic_6411.all;
3  ---------------------------------------------
4  ENTITY freq IS
5                  PORT ( IN1; IN2; IN3; AND  : IN STD LOGIC;
6                  Data : out STD LOGIC Vector(7 downto 0));
7  END freq;
8  ---------------------------------------------
9  ARCHITECTURE example OF freq IS
10 SIGNAL count1 : STD LOGIC Vector(7 downto 0);
11 BEGIN
12  count1(7)<= not count1(6);
```

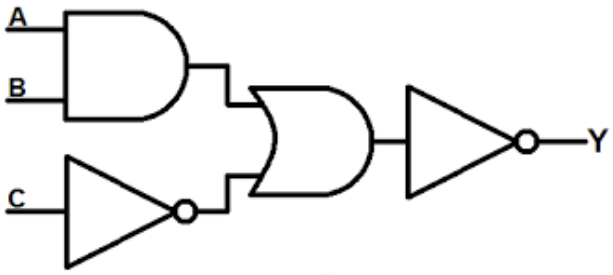
[Total Marks is 5]

```
13    count1(6)<= not count1(5);
14    count1(5)<= not count1(3);
15    count1(4)<= not IN1;
16    count1(3)<= in3 or AND;
17    count1(2)<= in3 and in2;
18    count1(1)<=count1(2);
19    count1(1)<=count1(0);
20    Data <= count1;
21  END Freq;
22  ------------------------------------------------
```

**Solution:**

```
1  LIBRARY ieee;          <- VHDL Use Clause error at Vhdl1.vhd(2): design library "ieee" does not contain primary unit "std_logic_6411"
2   USE ieee.std_logic_6411.all;
3   ----------------------------------------
                           <- VHDL syntax error at Vhdl1.vhd(5) near text ";";  expecting ":", or ","
4  ENTITY freq  IS          <- VHDL syntax error at Vhdl1.vhd(5) near text "AND";  expecting an identifier
5         PORT ( IN1; IN2; IN3; AND  : IN STD LOGIC;  VHDL error at Vhdl1.vhd(5): object "LOGIC" is used but not declared
6         Data : out STD_LOGIC_Vector(7 downto 0));
7  END freq;                <- VHDL syntax error at Vhdl1.vhd(6) near text "Vector";  expecting ";", or ")"
8  ----------------------------------------
9  ARCHITECTURE example OF  freq  IS
10 SIGNAL count1 : STD LOGIC Vector(7 downto 0);
11 BEGIN             VHDL syntax error at Vhdl1.vhd(10) near text "Vector";  expecting ";", or ":=", or "bus", or "register"
12  count1(7)<= not count1(6);
13  count1(6)<= not count1(5);
14  count1(5)<= not count1(3);
15  count1(4)<= not IN1;
16  count1(3)<= in3 or AND;
17  count1(2)<= in3 and in2;
18  count1(1)<=count1(2);  } Can't resolve multiple constant drivers for net "count1[1]" at Vhdl1.vhd(19)
19  count1(1)<=count1(0);  }
20  Data <= count1;
21 END Freq;
        <- VHDL syntax error at Vhdl1.vhd(21): name used in construct must match previously specified name "example"
```

3. Write a VHDL entity code that realizes the shown circuit.




**Solution:**

```
1                  LIBRARY ieee;
2                  USE ieee.std_logic_1164.all;
3                  ------------------------------------------------
```

```
4   ENTITY vhdl1 IS
5   PORT ( a,b,c   : IN STD_LOGIC;
6   y : out STD_logic);
7   END vhdl1;
8   ------------------------------------------------------
9   ARCHITECTURE example OF vhdl1 IS
10  SIGNAL and_out,or_out : STD_logic;
11  BEGIN
12  and_out<= a and b;
13  or_out<= and_out or not c;
14  y<= not or_out;
15
16  END example;
17  ------------------------------------------------------
```