Examiner : Dr. Mustafa M. Shiple
Subject: Selected Topics in Electronics /(ECE 569)
Score: 5 Marks

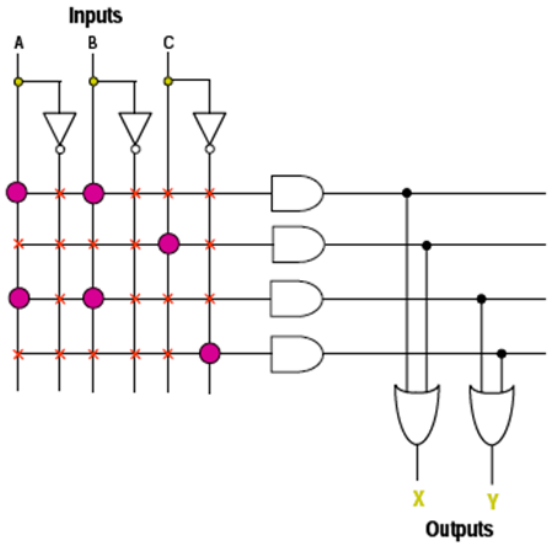
Term: Spring 2018
Exam Time:20 min

ANSWER THE FOLLOWING QUESTIONS:

1. Briefly discuss pros and cons of single PAL

Solution:

- t_{PD} being better
- Less complex software
- Output plan is fixed
- Medium logic density available to user



2. Consider the next VHDL code:
   (a) Check and correct syntax errors.
   (b) Synthesize the next code, and Draw the circuit.

```
1  LIBRARY ieee;
2  USE ieee.std_logic_6411.all;
3  ---------------------------------------------
4  ENTITY freq IS
5  PORT ( IN 1, IN 2, IN 3  : IN STD LOGIC;
6  Data : out STD LOGIC Vector(7 down 0));
7  END freq;
8  ---------------------------------------------
9  ARCHITECTURE freq OF example IS
10 SIGNAL count1 : STD LOGIC Vector(0 to 7);
11 BEGIN
```

[Total Marks is 5]

Signature of Examiner:

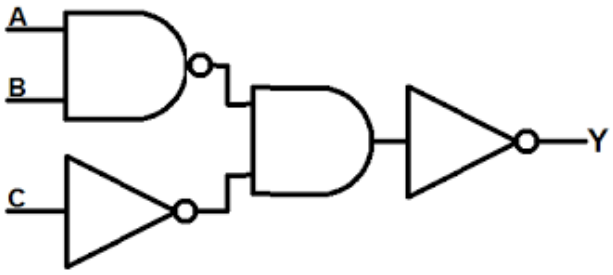
Good Luck
Head of Dept.:

```
count1(7)<= not count1(6);
count1(6)<= not count1(5);
count1(5)<= not count1(3);
count1(4)<= not IN 1;
count1(3)<= in 3 or in 1;
count1(2)<= in 3 and in 2;
count1(1)<=count1(2);
count1(1)<=count1(0);
Data <= count1;
END example;
```

Solution:

```
LIBRARY ieee;
 USE ieee.std_logic_1164.all;
 ----------------------------------------
                    VHDL syntax error at Vhdl1.vhd(5) near text "IN";  expecting an identifier ("in" is a reserved keyword)
 ENTITY vhdl1 IS                                VHDL error at Vhdl1.vhd(5): object "LOGIC" is used but not declared
        PORT ( IN 1, IN 2, IN 3  : IN STD LOGIC;
        Data : out STD LOGIC Vector(7 down 0));
 END vhdl1;                                     VHDL syntax error at Vhdl1.vhd(6) near text "0";  expecting ")", or ","
                           VHDL syntax error at Vhdl1.vhd(6) near text "Vector";  expecting ";", or ")"
 ----------------------------------------
 ARCHITECTURE vhdl1 OF example IS
SIGNAL count1 : STD LOGIC Vector(0 to 7);
BEGIN
count1(7)<= not count1(6);
count1(6)<= not count1(5);
count1(5)<= not count1(3);
count1(4)<= not IN 1;
count1(3)<= in 3 or in 1;
count1(2)<= in 3 and in 2;
count1(1)<=count1(2);
count1(1)<=count1(0);  Can't resolve multiple constant drivers for net "count1[1]" at Vhdl1.vhd(19)
Data <= count1;
END example;
          VHDL syntax error at Vhdl1.vhd(21): name used in construct must match previously specified name "vhdl1"
```

3. Write a VHDL entity code that realizes the shown circuit.



Solution:

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
```

```
3  ----------------------------------------------------------
4  ENTITY vhdl1 IS
5  PORT ( a,b,c  : IN STD_LOGIC;
6  y : out STD_logic);
7  END vhdl1;
8  ----------------------------------------------------------
9  ARCHITECTURE example OF vhdl1 IS
10 SIGNAL nand_out,and_out : STD_logic;
11 BEGIN
12 nand_out<= a nand b;
13 and_out<= nand_out and not c;
14 y<= not and_out;
15
16 END example;
17 ----------------------------------------------------------
```