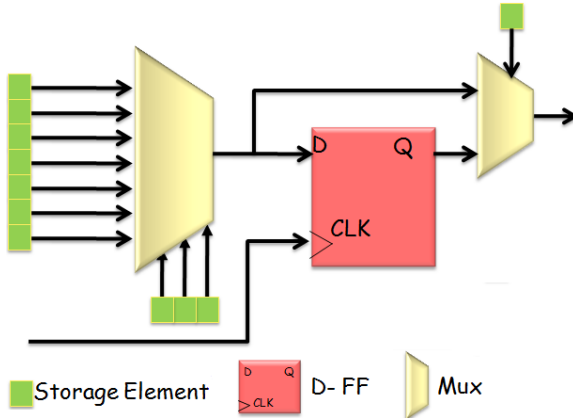


**ANSWER THE FOLLOWING QUESTIONS:**

1. Briefly discuss pros and cons of CLB.

**Solution:** CLB:Configurable Logic Block

- based on configurable multiplexer.
- contains D'FF for synchronous systems.



The diagram illustrates the internal structure of a Configurable Logic Block (CLB). It features a first multiplexer (Mux) on the left that takes multiple inputs from a vertical stack of green storage elements. The output of this Mux is connected to the D input of a D-type flip-flop (D-FF). The clock input (CLK) of the D-FF is also connected to the output of the first Mux. The Q output of the D-FF is connected to a second multiplexer on the right, which also receives an input from a single green storage element. The final output of the CLB is the output of this second Mux. A legend at the bottom identifies the components: a green square for 'Storage Element', a red square with 'D', 'Q', and 'CLK' for 'D- FF', and a yellow trapezoid for 'Mux'.

2. Consider the next VHDL code:

(a) Synthesize the next code, and Draw the circuit.

```

1      LIBRARY ieee;
2      USE ieee.std.logic.1164.all;
3
4      ENTITY freq IS
5      PORT ( IN1$, IN_2, IN3$ ; IN STD.LOGIC;
6      Data ; out STD.LOGIC.Vector(7 downto 0));
7      END freq;
8
9      ARCHITECTURE freq OF example IS
10     SIGNAL count1 : STD.LOGIC.Vector(0 to 7);
11
12
13     count1(7)<= not count1(6);
14     count1(6)<= not count1(5);
15     count1(5)<= not count1(3);
16     count1(4)<= not IN1$;
17     count1(3)<= IN3$ or IN1$;
18     count1(2)<= IN3$ and IN_2;
19     count1(1)<=count1(2);

```

[Total Marks is 5]

```

20     count1(1)<=count1(0);
21     Data <= count1;
22     END example;
23

```

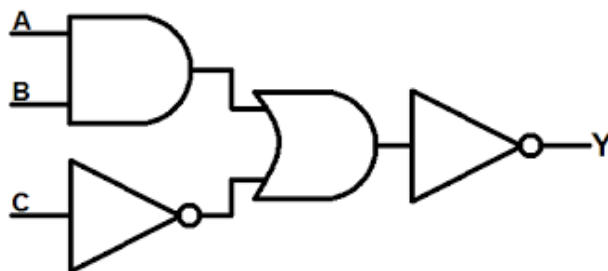
**Solution:**

```

1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  -----
4  ENTITY vhd11 IS          VHDL syntax error at Vhd11.vhd(5) near text $
                           VHDL syntax error at Vhd11.vhd(5) near text ";"; expecting ":", or ",",
5      PORT ( IN1$, IN_2, IN3$ ; IN STD.LOGIC;
6          Data ; out STD.LOGIC.Vector(7 downto 0));
7  END vhd11;
8  -----
9  ARCHITECTURE example OF vhd11 IS
10 SIGNAL count1 : STD.LOGIC.Vector(0 to 7);
11
12 VHDL syntax error at Vhd11.vhd(13) near text "count1"; expecting "begin", or a declaration statement
13     count1(7)<= not count1(6);
14     count1(6)<= not count1(5);
15     count1(5)<= not count1(3);
16     count1(4)<= not IN1$;
17     count1(3)<= IN3$ or IN1$;
18     count1(2)<= IN3$ and IN_2;
19     count1(1)<=count1(2);
20     count1(1)<=count1(0);  Can't resolve multiple constant drivers for net "count1[1]" at Vhd11.vhd(19)
21     Data <= count1;
22 END example;

```

3. Write a VHDL entity code that realizes the shown circuit.



**Solution:**

```

1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  -----
4  ENTITY vhd11 IS
5  PORT ( a,b,c : IN STD.LOGIC;
6        y : out STD_logic);
7  END vhd11;

```

8  
9  
10  
11  
12  
13  
14  
15  
16  
17

```
-----  
ARCHITECTURE example OF vhd11 IS  
SIGNAL and_out , or_out : STD_logic;  
BEGIN  
and_out<= a and b;  
or_out<= and_out or not c;  
y<= not or_out;  
  
END example;  
-----
```